Subthreshold and Near-Threshold Techniques for Ultra-Low Power CMOS Design

by

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Abstract

The miniaturisation of electronic circuits allows the potential for new applications, such as smart-dust or the Internet of Things. However, the design of batteries has not improved at the same rate as CMOS technology, so circuits need to be designed for improved energy efficiency to enable new form factors and applications.

To address these issues, the use of subthreshold and near-threshold supply voltages is proposed. Throughout this thesis, the nature of what makes a design suitable for subthreshold use is examined. This work starts at the gate level, where the effects of transistor geometry and valency are examined. The levels of abstraction are progressively increased until high level architectures are considered, where quasi-delay-insensitive and globally-asynchronous locally-synchronous designs are argued as suitable for designing reliable systems. To assist in this, a methodology for partitioning systems into separate timing domains is proposed, and applied to published designs.

The underlying theme throughout the exploration of subthreshold technology is the effects and mitigation of process and environmental variation, to which designs are increasingly susceptible as the supply voltage is lowered. This vulnerability affects all levels of design, from the widths of individual transistor to the choice of overall architectures, where a fundamental issue is the ability to determine when a unit of work has been performed.

Not all applications respond well to the scaling of supply voltage. To address this, an alternative approach is considered where the system spends much of its lifetime in a powered-down state, being woken at appropriate intervals by a wakeup timer. As power consumption is a function of frequency, this timer seeks to achieve energy efficiency by maximising the period of oscillation. Despite the higher supply voltages considered, the themes of environmental and process variation continue, as the wakeup timers examined share similarities to subthreshold designs. Two of the proposed timers have been fabricated and are compared to simulated results and other published work.

Statement of Originality

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