Aspects of Designing a High Speed Analog To Digital Converter

M.S. Hsu postgraduate student

Thesis submitted for the degree of

Master of Engineering Science

in

The University of Adelaide

(Department of Electrical and Electronic Engineering)

10 September 1992

Contents

This work contains no material which has been accepted for the award of any other degree or diploma in any university or other tertiary institution and to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text.

I give consent to this copy of my thesis, when deposited in the University Library, being available for loan and photocopying.

SIGNED :.

DATE : Jan 28, 1993

Acknowledgements

I would like to express my gratitute to the people who made their contributions to the completion of this research. First of all I would like to thank my supervisor, Associate Professor Dr. K. Eshraghian for his guidance and overall support during my stay in this University. Andrew Beaumont-Smith is the second person I would like to thank. Without his help in facilitating the CAD system, the tutorials for using the software and correcting my english,finishing this thesis would have been much much later. My partner Dr. Bertrand Hochet of EPFL Switzerland has given me special assistance in this research during his six months stay here. Derek Abbott helped me to organise the structure of this thesis. Finally, the friendship and assistance which I have received from the colleagues and staff of the department have made my stay in the University much more enjoyable. I would like to thank them all.

Abstract

Analog to Digital Converters operating in the microwave frequency are needed in digital telecommunications, optical data transmission systems and real time signal processors. The fastest ADC reported using BiCMOS technology can operate at 650M samples per second and offers 8-bit resolution. The high power dissipation is the main drawback of using bipolar silicon technology. The progress of scaling silicon devices is limited by both the development of process technology and the fabrication equipment. Thus, a low power, high speed ADC using silicon technology is not possible at the present time. On the other hand, Gallium Arsenide technology is very promising for high frequency operation with lower power consumption. A Gallium Arsenide ADC operating at 2.2 GHz has been reported, however it only offers 5-bit resolution, which limits its use to a small number of applications. Designing a high speed and high accuracy ADC using GaAs involves many complex issues, the two major obstacles limiting the accuracy are offset and hysteresis. Therefore, the main objective in this research program is to address these important issues.

Among many existing techniques of ADC design, a subranging architecture is selected primarily for its simplicity and high speed potential. The problem of a long sampling time needed in a conventional "input voltage sampling" scheme is eliminated by the use of a "reference voltage sampling" approach. Moreover, a very simple feedback structure and input coupling capacitors are adapted to perform an offset-free conversion. In overcoming the hysteresis problems a "bootstrapping" technique is used to clamp the drain-to-source voltage of the transistors which are subject to hysteresis. This is normally performed by cascoding schemes for hysteresis reduction. An ADC aimed at 8-bit and 1 GHz with a 1V input range and low power consumption is designed. The optimum speed and accuracy

compromise is achieved by the choice of device parameters. The simulation results show that the design can reach 8-bit resolution at a rate of 700M samples per second, with 256mW power dissipation for the analog circuit. In addition, the use of small transistor sizes makes the entire ADC realisable on a 3mm by 3mm chip.