Aspects of Designing a High Speed Analog To Digital Converter

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Contents

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Abstract

Analog to Digital Converters operating in the microwave frequency are needed in digital telecommunications, optical data transmission systems and real time signal processors. The fastest ADC reported using BiCMOS technology can operate at 650M samples per second and offers 8-bit resolution. The high power dissipation is the main drawback of using bipolar silicon technology. The progress of scaling silicon devices is limited by both the development of process technology and the fabrication equipment. Thus, a low power, high speed ADC using silicon technology is not possible at the present time. On the other hand, Gallium Arsenide technology is very promising for high frequency operation with lower power consumption. A Gallium Arsenide ADC operating at 2.2 GHz has been reported, however it only offers 5-bit resolution, which limits its use to a small number of applications. Designing a high speed and high accuracy ADC using GaAs involves many complex issues, the two major obstacles limiting the accuracy are offset and hysteresis. Therefore, the main objective in this research program is to address these important issues.

Among many existing techniques of ADC design, a subranging architecture is selected primarily for its simplicity and high speed potential. The problem of a long sampling time needed in a conventional "input voltage sampling" scheme is eliminated by the use of a "reference voltage sampling" approach. Moreover, a very simple feedback structure and input coupling capacitors are adapted to perform an offset-free conversion. In overcoming the hysteresis problems a "bootstrapping" technique is used to clamp the drain-to-source voltage of the transistors which are subject to hysteresis. This is normally performed by cascoding schemes for hysteresis reduction. An ADC aimed at 8-bit and 1 GHz with a 1V input range and low power consumption is designed. The optimum speed and accuracy

compromise is achieved by the choice of device parameters. The simulation results show that the design can reach 8-bit resolution at a rate of 700M samples per second, with 256mW power dissipation for the analog circuit. In addition, the use of small transistor sizes makes the entire ADC realisable on a 3mm by 3mm chip.

Chapter 1

Introduction

Electrical signals are generally divided into two categories: digital and analog [TEMES]. Analog signals carry information by the use of current, voltage, charges and so on. It is a continuous function of the continuous time variable. For examples, audio amplifiers and RC filters are the circuits for analog signals. Digital signals are represented by a sequence of numbers, typically codes in the form of binary digits or bits. The information is in the form of discrete values at discrete time interval. The examples are computer CPUs and digital filters. Usually, different process technologies are needed to fabricate analog and digital ICs.

1.1 An introduction to Analog to Digital Converter

The analog to digital converter (ADC) is an essential link between digital and analog systems. It samples a continuous analog signal and converts it to digital data at discrete time interval. This function is illustrated in figure 1.1. Depending on the architecture

chosen and the techniques used in the design of an ADC, different configurations can be included in the circuit. Following subcircuits are normally used;

- a quantizer which consists from one to 2^N comparators to converter an analog signal to digital data.
- a reference voltage generator to create the voltage levels for the quantizer to compare to input signal.
- sample and hold circuit which is usually placed in front of the quantizer to provide static input voltage. It is also used in pipelined architecture to hold the voltage transferred from the previous stage.
- digital encoders to encode the digital data received from the quantizer to output digital word.
- logic and clock generators to provide control signals and internal clocks.
- multiplexer and subtractor to generate residual voltages for pipelined comparators.
- digital to analog converters to provide intermediate voltage for the quantizer.
- self calibration circuits to eliminate errors.

The performance of an ADC is assessed with following figures of merit.

- resolution or bit count, which is the bit number of the digital output.
- bandwidth of operation, this is defined by the unit gain frequency.

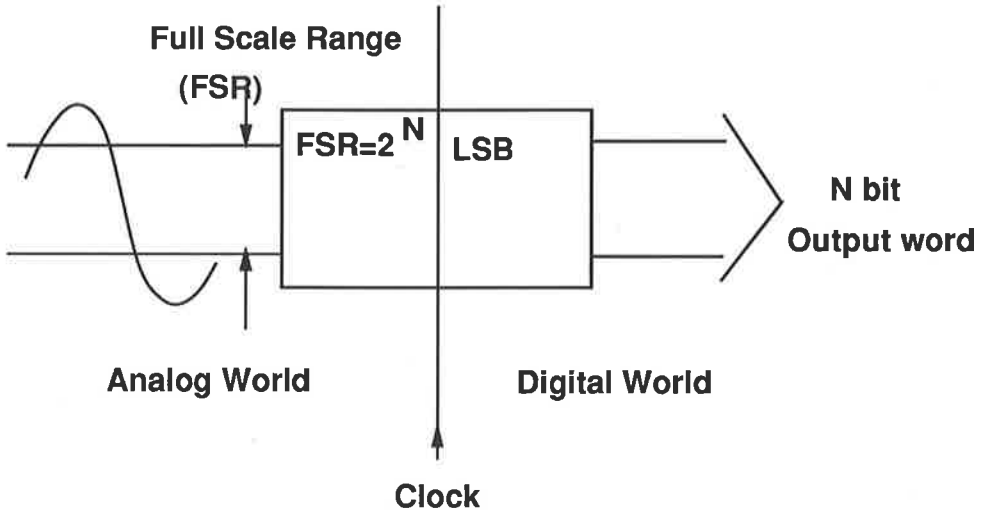


Figure 1.1: Basic A/D Converter

- power consumption, which is the product of the supplied power and the total current consumed.
- linearity, which is the measure of the difference between ideal conversion and the real.
- maximum sampling rate, which is the highest number of samples the input can detect in unit time.
- maximum input dynamic range, which is the input voltage range that the circuit can operate properly.

Based on the area of applications, various emphasis in the specifications are required. However, the most distinct items of the specification are resolution and sampling rate. Sampling rate can be expressed as "M samples per second (Ms/s)" or "MHz" or "M conversions per second". The resolution is expressed as "N output digital bits" or "1 LSB = nV" together with the full input scan range. Following the recent improvement

in the speed of digital signal processing, the demand for high speed ADCs also increases. In the application of low resolution ADCs, optical transmission links require a sampling rate from 2.4 GHz to 10 GHz. Satellite transmissions and logic analysers require ADCs with two to five bit resolution at one to two GHz rate. For medium resolution applications, nuclear instrumentation and wide input bandwidth oscilloscopy demand 4-6 bit resolution at 1-2 giga samples per second. General purpose ADC, identification radar systems and video systems require higher resolution (6-8 bit) at a rather lower rate (0.1-1 GHz)[LEP][NABER].

1.2 ADC architectures in silicon

Since the analog to digital converters (ADC) have been developed and used for a long time, the techniques used to design ADCs are very well established. Depending on the application, different types of ADC are chosen to fulfill the requirements of accuracy, speed or cost. In this chapter, five main types of ADC architectures will be discussed [HOES].

1.2.1 Flash converter

The most straight forward type of ADC, flash converters or parallel A/D converters, are commonly accepted as the architecture which consumes the least time in conversion. Figure 1.2 shows the structure of a N-Bit flash converter in which one comparator is used for each quantisation level. A comparison cycle can be completed in one step. That facilitates sampling rates of hundreds of mega samples per second possible. Mean while, both

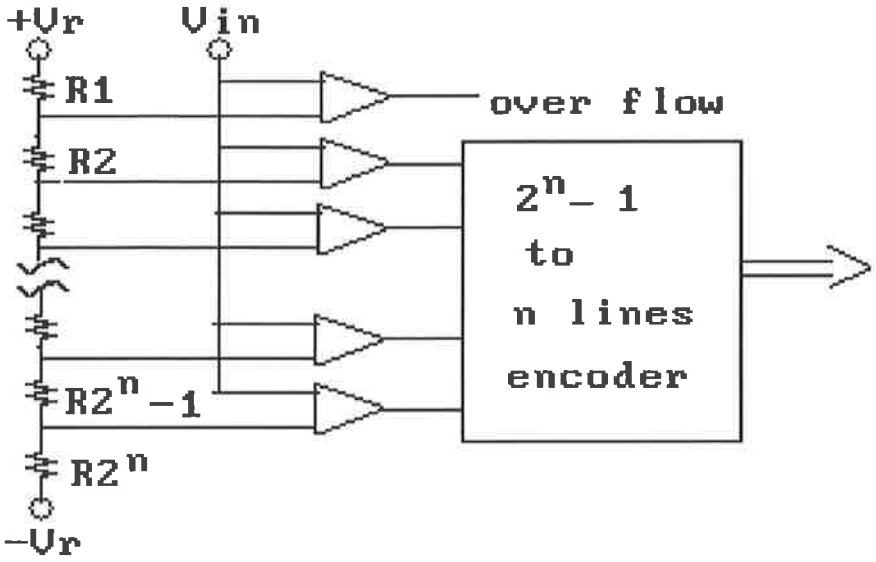


Figure 1.2: A flash converter

the analog and digital parts of the ADC are simple and straight forward. The possible errors result from the reference voltages and the comparators. However, this architecture requires 2^N comparators for its quantizer to carry out the comparisons and a large number of logic devices to encode the results at the comparators outputs. Therefore, the large input capacitance of the quantizer will cause more difficulties in designing a S/H circuit in front of it. Moreover, the over all power and area needed makes flash impractical for high speed and high accuracy applications.

1.2.2 Pipeline Converter

Other than flash converters, the Pipeline ADC is another alternative for very high speed applications. It takes one input sample in each clock period and continuously generates the results at the output N clock periods later. Once the pipeline is full (initial N clock latency) one conversion can be done each clock cycle. Fig 1.3 is a sample of pipeline ADC.

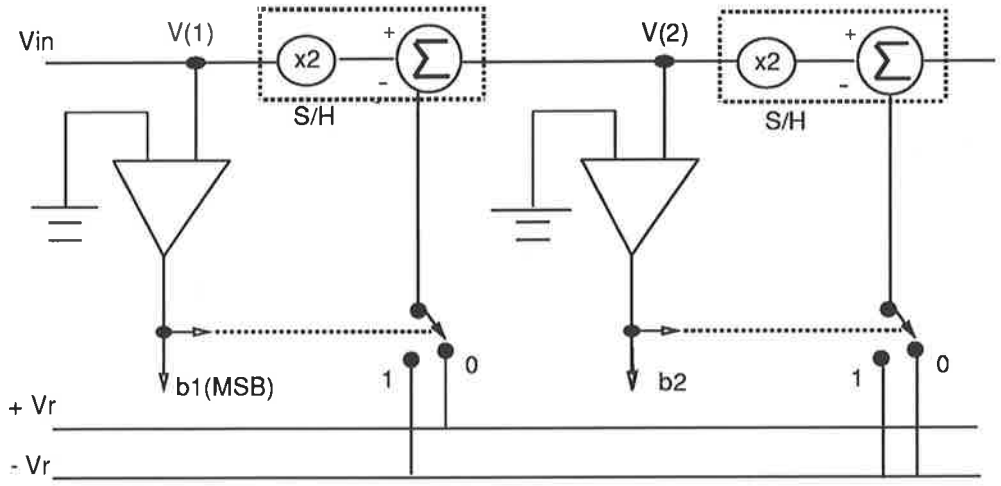


Figure 1.3: A pipeline analog to digital converter

In this architecture N comparators are used for a N-Bit conversion. In the first period V_{in} is sampled and compared with the level of the most significant bit (MSB). The result will be used to decide a positive or a negative reference voltage V_r sent to the second stage. Then V_{in} will be multiplied by two and summed to the $+V_r$ or $-V_r$ before the comparison for the second MSB.

At the same time the first comparator samples another input voltage and performs the comparison for the MSB of the new V_{in}. The process carries on until the least significant bit (LSB) is compared and the result of N logic bits can be obtained from the N comparators. The following equations express the operations mathematically.

$$V(1) = V_{in}$$

$$-V_r <= V_{in} <= +V_r$$

$$V(k+1) = 2V(k) + (-1)^{b_k} V_r$$

$$b_k = \begin{cases} 1 & \text{if } V(k) > 0 \\ 0 & \text{if } V(k) < 0 \end{cases}$$

$$V(N) = 2^{N-1}(V_{in} + \sum_{k=1}^{N-1}(-1)^{b_k}2^{-k}V_r)$$

In this circuit, N sample and holds (S/H) are needed for N comparison stages in addition to a large number of shift registers used to equalise the bit delays. Errors can be introduced from the multiplication and summing circuits, especially if the errors occur in the earlier stages they will be carried and amplified in the latter stages. This architecture is limited to medium accuracy applications.

1.2.3 Subranging ADC

The conversion using this type of architecture is also called serial-parallel conversion. It takes $2^{N/2}$ comparators and two clock periods to complete one comparison. In the first period, V_{in} is compared with the full range of the reference voltage which is divided into $2^{N/2}$ quantisation levels called coarse reference voltages, instead of 2^N levels in flash converters. The result is processed to determine the voltage range to be used in the second period where the voltage step between two coarse reference voltages in the first period is further divided into $2^{N/2}$ levels, those are called fine reference voltages.

Figure 1.4 shows the architecture of a subranging ADC in which a digital to analog converter (DAC) may be included to provide the chosen level from the result of the first comparison for the second comparison. A switch and resistor ladder combination can

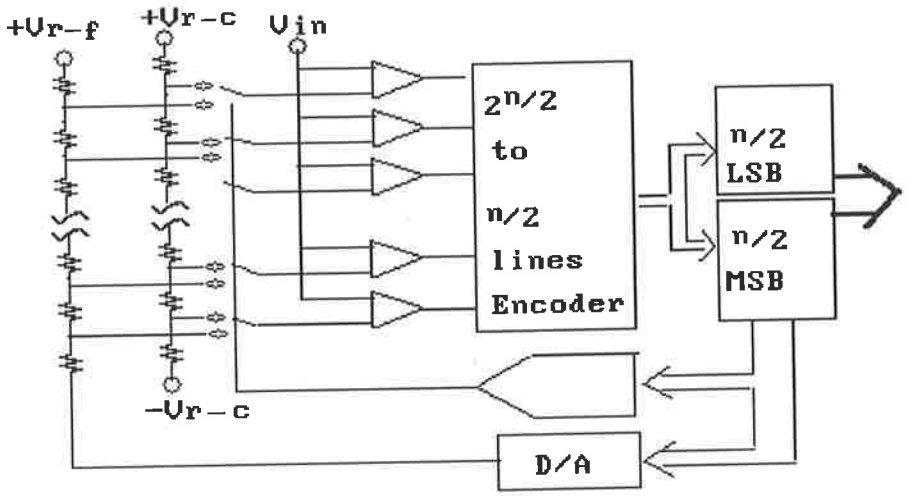


Figure 1.4: A subranging ADC

also serve the same purpose. This architecture uses less components than a full flash ADC and the control circuit is much simpler than that of a pipeline converter. The error sources of this circuit are limited to the reference voltages and the comparators. Thus, the applications for higher resolutions are possible.

Due to the small input capacitance the speed of a subranging converter is depends on the response of the comparators and the settling time of the fine reference voltages, whereas the large capacitive load is a draw back of flash converters. Subranging ADC is more promising in high speed applications, though it takes one more clock period.

1.2.4 Successive Approximation Converter

This kind of converter is one of the most commonly used ADC. It consists of a digital to analog converter (D/A) decoder which generates reference voltages to compare with the input voltage at the comparator, a reference voltage source and a programmer which sets and resets each bit of the D/A decoder. Figure 1.5 shows the structure of a successive

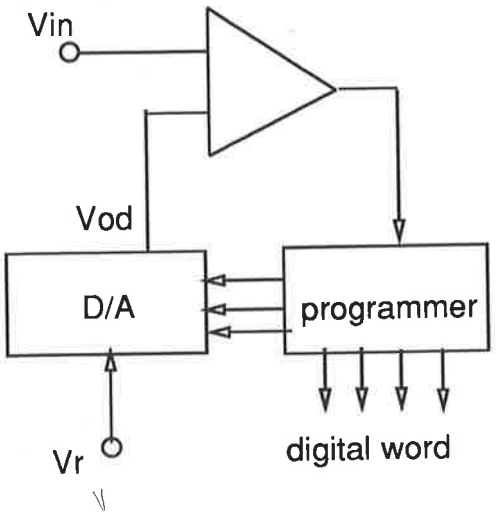


Figure 1.5: A successive-approximation converter

approximation converter. Conversion starts from the MSB and successively trys a '1' in each bit of D/A decoder. As each bit is tried, the output of the D/A decoder V_{od} is compared against the input V_{in}. If V_{in} is larger than V_{od}, the '1' remains in that bit, and a '1' is tried in the next bit. If V_{od} is larger than V_{in} at the Nth bit, the '1' is removed from that bit. At the end of the process the digital word in the programmer is equivalent to the sampled input voltage.

The conversion rate is limited by the successive trial of each bit. In addition, sufficient time must be allowed for the D/A decoder to reach its final value in each step, and enough time is also needed for the comparator to recover from its previous input. The accuracy of this type of ADC is a function of the quantising errors, accuracies of the D/A converter, voltage reference and the comparator. It can be used in low speed and medium accuracy applications.

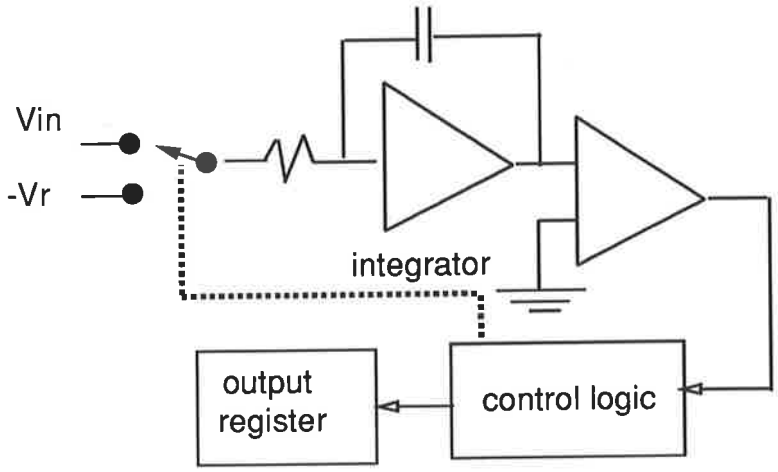


Figure 1.6: A dual slope converter

1.2.5 Dual Slope Converter

This architecture is used in low speed and high accuracy operations. Figure 1.6 depicts the simplicity of this type of converter. It consists of an integrator, a comparator, a voltage reference and logic. In the circuit the integrator is to integrate the input signal and enable the immunity to noise. Initially, the unknown analog input voltage is applied to the integrator input for a preset number of clock pulses P. Then, the integrator input is switched to a reference voltage of opposite sign. In a number of clock pulses M, the output voltage of the integrator falls to 0 volt. Thus, the input voltage V_{in} can be determined by

$$V_{in} = \frac{M}{P} V_r$$

If P is set to be equivalent to 2^N where N is the bit count of the converter, then V_r/P equals to 1 LSB. Thus the input voltage V_{in} can be expressed as a logic number M. The conversion process is extremely slow. However, the possible error sources are

ARCHITECTURE	DEVICE COUNT	COMPLEXITY	APPLICATIONS
Flash	large	low	high speed low accuracy
Pipeline	medium	high	high speed medium accuracy
Subranging	medium	medium	high speed medium accuracy
Successive-appro.	small	high	low speed medium accuracy
Dual Slope	small	low	low speed high accuracy

Table 1.1: The summary of ADC architectures

limited to only the voltage reference and the comparator, which means very high accuracy conversions can be achieved.

1.2.6 Summary of ADC architecture

The characteristics of above mentioned ADC architectures are summarised in table 1.1. The choice of the architecture depends on the application and its limitations. Normally, speed and accuracy are the major indicators of the performance of an ADC and very often characteristics move in opposite direction and compromises are required.

1.3 Efforts toward high speed and high accuracy ADC

In the past decade a lot of efforts have been conducted toward the development of high speed and high accuracy ADC with low power consumption using CMOS and bipolar process technologies. As discussed in the previous section, successive approximation con-

verter can be used to design very high accuracy ADC. A 12 bit and a 15 bit ADC have been reported by [LEE] using fold cascode comparator structure and by [PING] using MOS integrator and exchanging capacitors. However, they achieved only 8 KHz and 12 KHz respectively. For high frequency operation, flash, subranging and pipeline architectures are usually selected.

These architectures can be implemented using either CMOS for its low power consumption or bipolar for its high speed. In addition to the choice of the architecture, some factors must also be considered before a high performance ADC can be obtained. 1) low power consumption at high operating frequency; 2) reduced kickback to the input; 3)aperture uncertainty less than 30 ps; 4) prevention of missing codes at high sampling rate; 5) overcome clock jitter and glitches. [AKAZAWA][INOUE].

An 8 bit flash ADC using bipolar technology has been reported to achieve 400 MHz sampling rate [AKAZAWA]. In his design a quasi-gray-code technique is used to eliminate carry error, which is one of the major problem associated with flash converter, without the excess time taken to get an 8 bit output.

The use of bipolar falls short of the low power consumption which CMOS can achieve. [YOSH] points out in his paper that reducing the current used in a bipolar ADC by reducing the emitter size causes the circuit unable to reach the aimed 8 bit resolution. Instead, he uses small transistors with thick field oxide to reduce capacitance, his design reaches 8 bit resolution at 40 MHz with 1.2W power dissipation.

The following examples demonstrate that using CMOS enables low power consumption for high speed ADC. However, the large number of comparators and hence the input capacitance of flash architecture enhance the popularity of subranging ADC in high speed applications. A 10 bit 5 Ms/s CMOS two-step flash ADC has been reported [DOER]. This design introduces a sharing component scheme among the ADCs and DACs in the circuit to eliminate matching problems associated with classical two-step flash.

Differential structure is very often used in ADC design to cancel the problems of switch charge injection and common mode noise [PING][DOER]. A new chopped-type comparator with three input terminals and offset cancellation is introduced by [HOSO]. Using a set of cascade connected inverters and a feedback switch, his subranging and pipelined ADC reaches 7.4 bit resolution and 20 MHz.

In order to predict the performance of the circuits with shrunk devices [DENN] proposed a constant field scaling model. In which a reduction factor K is applied to all physical dimensions and supplied voltage. Improvements in speed, power and power speed product by the factors of K, K^2 and K^3 respectively are predicted.

[BERG] introduce a combined voltage and dimension scaling model based on the fact that voltage and dimensions are not usually scaled with the same factors. Two independent factor are used for physical dimensions and supplied voltage separately.

Scaling models have been effectively implemented in the actual fabrication of ICs for years. However, continuing this process far enough, limits will eventually be encountered

[SOLO] [HOEN] has studied the electrical limits including minimum energy for computing, electrical breakdown and punchthrough and wire and contact resistance.

There are different limits that exist for FET and bipolar devices. For FET, the built-in potential needs to be compensated by increasing channel doping, which will reduce the mobility of charge carriers. As voltage is reduced, the thermal energy KT/e gives the device an increasing soft turn-on [DENN]. The signal to noise ratio restricts the minimum supply voltage to 0.5V [SOLO].

For bipolar, the increasing contact resistance reduces small signal transconductance. Also, emission-limited transport is possible to happen due to the shrunk diffusion depth. Moreover, increasing current density aggravates the electron migration. When current density is retained and dimensions are reduced the speed will be reduced.

While silicon technology is facing the problems associated with its physic nature, GaAs is working its way into the market with the superior characteristics. In 1984, a multinational organisation ESPRIT was launched in Europe for the development of information technology. All major European semiconductor manufacturers are involved in the technology development and the production of non-military GaAs product. Many foundries are now available for analog GaAs products [TURN].

The performance of many GaAs device technologies are compared in different applications [GRAA]. Due to the slow hole mobility, complementary GaAs FET are impractical [ALLEN]. Fortunately, many of the nMOS design techniques and the tools for silicon can

be used directly by GaAs [LARS2], and enables GaAs to outperform silicon. For example, switched-capacitor circuits in GaAs can reach 100 Ms/s while it is 15 Ms/s in silicon. Borrowing techniques from silicon, GaAs ADCs demonstrate superior performance over their silicon counterparts in high speed and low power consumption. Cascode structure is also quoted to provide high output impedance and reduce Miller effect [FAWC].

The application of GaAs technology in analog designs have shown the potential to replace silicon in signal processing [ALLEN]. The improvements of GaAs ADC over silicon has made available low power and high speed products. [KLEKS] has reported the first complete 4 bit ADC working at 1 GHz. Using regenerative comparator for high gain, [NABER] has designed a 4 bit, 1 GHz flash ADC with only 140 mW power consumption, when its silicon counterpart consumes 12 times more power [DANI].

An ADC working at 3 Gs/s is reported by [DUCO1]. The original flash structure is used to design this fastest 4 bit ADC. The best performing ADC is also reported by [DUCO2]. This circuit used flash architecture to reach 5 bit resolution, 2.2 GHz with 320 mW for the analog circuit and 730 mW for the ECL buffers.

Yet the resolution GaAs has achieved is still not compatible with silicon. There are effects limiting the accuracy [BAYR]: 1) the drain lag effect; 2) poor device matching; 3) low transconductance; 4)backgating and sidegating; and 5) high $1/f$ noise. The mismatch of passive component does not cause real problem in accuracy [GREI] [ALLEN], when the threshold variation incurs the large offset voltage. The standard deviation is about 20 to 50 mV [LARS2]. Self calibration or offset compensation circuits are usually included

to cancel the effect of offset voltage [ALLEN2]. [FAWC] announce the first MESFET comparator with internal self calibration circuit, which offers the potential for a 6-10 bit 2 GHz ADC.

Operating in GHz region clock skew or jitter is a major concern to missing code especially for flash. Sample and hold circuit is a rescue to this problem. Apart from offset voltage, hysteresis is the main factor limiting the accuracy. It is caused by the trapped charges and frequency dependent current injection [LAU] [DUCO3]. The same reason also incurs back channel modulation. Common mode feedback [KATSU], bootstrapping [KLEKS] and cascode structure are the techniques used to reduce this effect.

Up to present, the state of the art ADC reported is 5 bit 2.2 GHz with 320 mW power consumption. Laying in front of us is a challenge of designing a higher resolution ADC working at GHz region. This leads to the initiation of this research. A target is set to design an 8 bit, 1 GHz ADC with low power consumption. All the problems associated and the techniques used in other designs are studied, this thesis is exploring the possible solutions to meet the target.

1.4 The scope of this thesis

In this chapter we have already reviewed the need of high speed ADC. At this time, the fastest ADC using silicon technology offers 650M samples per second, with 8-bit resolution and 850mW power consumption[EIND]. Using bipolar silicon technology has the

potential to implement GHz sampling rates of ADCs. However, the main drawback is the high power dissipation. The main objective of this research is to explore possible solutions and their associated complexity for designing a high speed, high accuracy and low power ADC. From the previous study of the design techniques of ADCs and the suitable area of their applications, the flash, pipeline and subranging architectures are regarded as three possible candidates for very high speed applications. The considerations about power dissipation and chip area for higher bit count ADCs make the flash architecture unsuitable for our task. Moreover, the associated complexity and potential error sources of pipeline converters may restrict the accuracy of our design. Subranging architecture poses the least problem and is most promising for further investigation.

In chapter two, three different scaling models are investigated. The effects of scaling the physical dimensions of silicon devices as well as the electrical parameters on the circuit performance are assessed. Also in this chapter the limitations of scaling are discussed.

The properties of Gallium Arsenide as a new base for semiconductor devices is introduced in chapter three. The comparison between GaAs and silicon is presented to understand the advantages and disadvantages of using GaAs VLSI technology. This is followed by introducing techniques to minimise the main problems and fulfill the advantages of using GaAs technology in an ADC design. The design of a comparator is also presented.

Chapter four gives an in depth tutorial in the effects of device size, currents, voltages and resistive load on the performance of the comparator. Simulation results are attached to demonstrate the findings and outcome.

In Chapter five, the considerations in the placement of devices are explained together with a series of layouts of main cells used.

Finally, the possible error sources in this design are discussed in chapter six. Some alternative approaches which may improve the performance of the circuit are also discussed.

Chapter 2

The review of the scaling effects on silicon MOS

The purpose of this chapter is to investigate the performance of silicon devices when they are scaled to extremely small sizes. Through the understanding of the possible improvements as well as the limitations of scaling MOS transistors and the interconnections the need of developing GaAs technology emerges.

Since the invention of transistor in 1947, and the first integrated circuit in early 1960's, four generations of technology and products have been developed. In order to characterise a technology and to guide the development in semiconductors, several indicators are used:

- Minimum feature size
- Number of gates in one chip
- Power dissipation
- Maximum operational frequency

- Die size
- Production cost

As many of the figures of merit can be improved by shrinking the dimensions of transistors, and adjusting the doping levels and supply voltage accordingly, a lot of effort has been directed toward the upgrading of process technology and scaling down of devices in last decade. Nowadays, scaling is an important step for improving the performance of semiconductor devices. To better appreciate the influences of scaling on integrated circuits and the associated problems, the effects of scaling over parameters and the restrictions which will limit the progress of scaling will be discussed.

2.1 Scaling Models

The most commonly used "Constant electric field scaling model" and "Constant voltage scaling model" were introduced some fifteen years ago. They both are simplified models which take only the first order effects into consideration. A "Combined voltage and dimension scaling model" was presented recently [BERG].

In order to express specific concerns in this paper, all above mentioned models and their applications to MOS transistors are quoted. Therefore, $1/\beta$ is chosen as the scaling factor for supply voltage and gate oxide thickness, and $1/\alpha$ is the scaling factor for all other linear dimensions including the vertical and the horizontal. To transfer to the constant field model to the constant voltage model, $\beta = \alpha$ and $\beta = 1$ are applied respectively.

2.1.1 Scaling Factors

In this section simplified calculations are used to derive the scaling factors for both device parameters and their derivations.

- Gate area, A_g

$$A_g = L \cdot W$$

where L is channel length and W is channel width. They are both scaled by $1/\alpha$. So, A_g is scaled by $1/\alpha \cdot 1/\alpha = 1/\alpha^2$.

- Gate capacitance per unit arca, C_{ox}

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

where ε_{ox} is the gate oxide permitivity which is constant, and t_{ox} is the gate oxide thickness which is scaled by $1/\beta$. Therefore,C_{ox} is scaled by $1/1/\beta = \beta$.

- Gate capacitance, C_g

$$C_g = C_{ox} \cdot L \cdot W$$

C_g is scaled by $\beta \cdot 1/\alpha \cdot 1/\alpha = \beta/\alpha^2$.

- Parasitic capacitance, C_{ox}

$$C_{ox} \propto \frac{A_x}{d}$$

where d is depletion width around the source or drain which is scaled by $1/\alpha$, and A_x is the area of depletion region around source or drain which is scaled by $1/\alpha^2$. So, C_{ox} is scaled by $1/\alpha_2 \cdot 1/1/\alpha = 1/\alpha$.

- Carrier density in channel, Q_{on}

$$Q_{on} = C_{ox} V_{gs}$$

Q_{on} is the average charge per unit area in the channel in the "ON" state. C_{ox} is scaled by β and V_{gs} is scaled by $1/\beta$. So, Q_{on} is scaled by $\beta \cdot 1/\beta = 1$.

- Channel resistance, R_{on}

$$R_{on} = \frac{L}{W} \frac{1}{Q_{on}\mu}$$

where μ is carrier mobility which is assumed constant. So, R_{on} is scaled by $1/\alpha \cdot 1/1/\alpha \cdot 1 \cdot 1 = 1$.

- Gate delay, T_d

$$T_d \propto R_{on} \cdot C_g$$

So, T_d is scaled by $1 \cdot \beta/\alpha_2 = \beta/\alpha^2$.

- Maximum operational frequency, f_o

$$f_o = \frac{W}{L}\frac{\mu C_{ox} V_{DD}}{C_g}$$

or f_o is inversely proportional to T_d. So, f_o is scaled by $1/1 \cdot 1 \cdot 1 \cdot 1/\beta \cdot 1/\beta/\alpha_2 = \alpha^2/\beta$.

- saturation current, I_{on}

$$I_{on} = \frac{W}{L} \cdot \mu C_{ox} \cdot 1/2(V_{gs} - V_t)^2$$

where V_t is the threshold voltage which is scaled by $1/\beta$. So, I_{on} is scaled by $1/1 \cdot 1 \cdot \beta \cdot (1/\beta)_2 = 1/\beta$.

- Current density, I

$$I = \frac{I_{on}}{A}$$

where A is the cross-section of the channel in the "ON" state which is scaled by $1/\alpha^2$. So, I is scaled by $\beta \cdot 1/1/\alpha_2 = \alpha^2/\beta$.

- Switching energy per gate, E_g

$$E_g = \frac{1}{2} C_g V_{DD}^2$$

So, E_g is scaled by $\beta/\alpha_2 \cdot 1/\beta_2 = 1/\alpha^2\beta$.

- Power dissipation per gate, P_g

$$P_g = \begin{cases} \frac{V_{DD}^2}{R_{on}} & \text{for the static state} \\ E_g \cdot f_o & \text{for the dynamic state} \end{cases}$$

P_g for the static state is scaled by $1/\beta_2 \cdot 1$. P_g for the dynamic state is scaled by $1/(\alpha_2 \cdot \beta) \cdot \alpha_2/\beta$. So, in both states P_g is scaled by $1/\beta^2$.

- Power dissipation per unit area, P_a

$$P_a = \frac{P_g}{A_g}$$

So, P_g is scaled by $1/\beta_2 \cdot 1/1/\alpha_2 = \alpha^2/\beta^2$.

- Power-speed product, P_T

$$P_T = P_g T_d$$

So, P_T is scaled by $1/\beta \cdot \beta/\alpha_2 = 1/\alpha^2\beta$.

2.1.2 Summary

Table 2.1 summarises the effects of the three scaling models (combined voltage & dimensions, constant electric field and constant voltage) on the device parameters

Parameters		V & D	E	V
V_{DD}	supply voltage	$1/\beta$	$1/\alpha$	1
L	channel length	$1/\alpha$	$1/\alpha$	$1/\alpha$
W	channel width	$1/\alpha$	$1/\alpha$	$1/\alpha$
d	gate oxide thickness	$1/\beta$	$1/\alpha$	1
A_g	gate area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha^2$
C_{ox}	gate capacitance per unit area	β	α	1
C_g	gate capacitance	β/α^2	$1/\alpha$	$1/\alpha^2$
C_{ox}	parasitic capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha$
Q_{on}	carrier density	1	1	1
R_{on}	channel resistance	1	1	1
I_{on}	saturation current	$1/\beta$	$1/\alpha$	1
A_c	cross-section of conductor	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha^2$
I	current density	α^2/β	α	α^2
V_g	logic level	$1/\beta$	$1/\alpha$	1
E_g	switching energy	$1/\alpha^2\beta$	$1/\alpha^3$	$1/\alpha^2$
P_g	power dissipation per gate	$1/\beta^2$	$1/\alpha^2$	1
N	gate per unit area	α^2	α^2	α^2
P_a	power dissipation per unit area	α^2/β^2	1	α^2
T_d	gate delay	β/α^2	$1/\alpha$	$1/\alpha^2$
f_o	maximum operational frequency	α^2/β	α	α^2
P_T	power-speed product	$1/\alpha^2\beta$	$1/\alpha^3$	$1/\alpha^2$
'V & D' - combined V & D model, 'E'- Constant Electric Field Model, 'V'- Constant Voltage Model.				

Table 2.1: The summary of three scaling models

of MOSFETs.

2.2 Observations and Limitations of Scaling

Scaling has been proved of great value to improve the figures of merit of semiconductor devices. However, along with the scaling down of devices, some associated problems also become severe and will eventually restrain further shrinkage of devices.

2.2.1 Substrate Doping

In the above mentioned models, the effects of built-in potential V_B was neglected because it is relatively small compared to supply voltage V_a. However, due to the progress in process technology, the V_a used in the consideration of future scaling is not much greater than V_B. So, the effects of V_B must be included. Moreover, the concentration of a substrate decides many of the characteristics of the transistors fabricated on it. Therefore, this research investigates the related effects in more detail.

In the following, a modified factor which should be used to scale substrate doping is introduced. As the channel length of a MOS transistor is reduced, in order to keep the depletion region around the source from meeting that of the drain, the depletion region width must be scaled accordingly. The depletion region width d is given by [GROVE]

$$d = \sqrt{\frac{2\varepsilon_{si}\varepsilon_0 V}{qN_B}} \tag{2.1}$$

where

ε_{si} = relative permitivity of silicon

ε_0 = permitivity of free space

V = effective voltage across the junction $= V_a + V_B$

q = electron charge

N_B = doping level of substrate

V_a = applied voltage

V_B = built-in potential

and

$$V_B = \frac{kT}{q} \ln \frac{N_B N_D}{n_i^2} \tag{2.2}$$

Where N_D is the source or drain doping, and n_i is the intrinsic carrier concentration in silicon.

In earlier processes for integrated circuits, V_B is in the order of 500 mV. Compared with high V_a, say 5V, it may be negligible when the effects of scaling N_B are considered. That yields

$$d = \sqrt{\frac{2\varepsilon_{si}\varepsilon_0 V_a}{qN_B}} \tag{2.3}$$

When V_a is scaled by $1/\beta$ and d is scaled by $1/\alpha$, N_B can be scaled by α^2/β [BERG]. Since N_B is increased to reduce d, V_B is also enlarged. For example, a transistor with $N_B = 10^{15}$ cm^{-3} and $N_D = 10^{20}$ cm^{-3} yields $V_B = 0.88$V. At the same time, the V_A sought is getting smaller to take full advantage of scaling. Thus, the engaged V_a is no longer relatively very large , and V_B should be taken into consideration for further scaling.

In the case of applying the Combined Voltage & Dimension Scaling Model [BERG] to a transistor which works at a known V_a, we can reasonably assume $V_a = m \cdot V_B$. Where m can be any real number. Thus

$$V = V_a + V_B = m \cdot V_B + V_B$$

Now we scale V_a by $1/\beta$. That gives us

$$V_s = \frac{m \cdot V_B}{\beta} + V_B = \frac{\beta + m}{\beta(m+1)} V \tag{2.4}$$

Where V_s is the scaled effective voltage across the depletion region. As the the result of the calculation shows, V is scaled by $(\beta+m)/\beta(m+1)$. Consequently, N_B should be scaled by $\frac{\alpha^2(\beta+m)}{\beta(m+1)}$, so that d can be scaled by $1/\alpha$.

This model not only expresses the effects of the relationship between V_a and V_B,

but also shows their connection to the scaling factor β. In the cases of large m and small β the scaling factor of N_B returns to α^2/β. But in other cases where β and m are not much greater than one, the value of this model will become significant.

Here the adjustment of scaling factor for depletion width according to the scaled doping will also be investigated. In the previous discussion, N_B is increased to reduce depletion width. This also incurs a higher threshold voltage V_t, which moves against the trend of scaling down voltage. According to [HOEN] the maximum N_B must be kept below 1.3×10^{19} cm^{-3}. At higher N_B the maximum electric field which can be applied to gate oxide does not invert the substrate.

However, the technology of deep channel implantation can increases the concentration near the junction of source and drain. This reduces the depletion width and maintains the substrate concentration in the channel area and prevents the problem. Nonetheless, the depletion width and the built-in potential will still restrict the progress of scaling.

From Eq 2.1 and Eq 2.2

$$E_{max} = \frac{2V}{d} \tag{2.5}$$

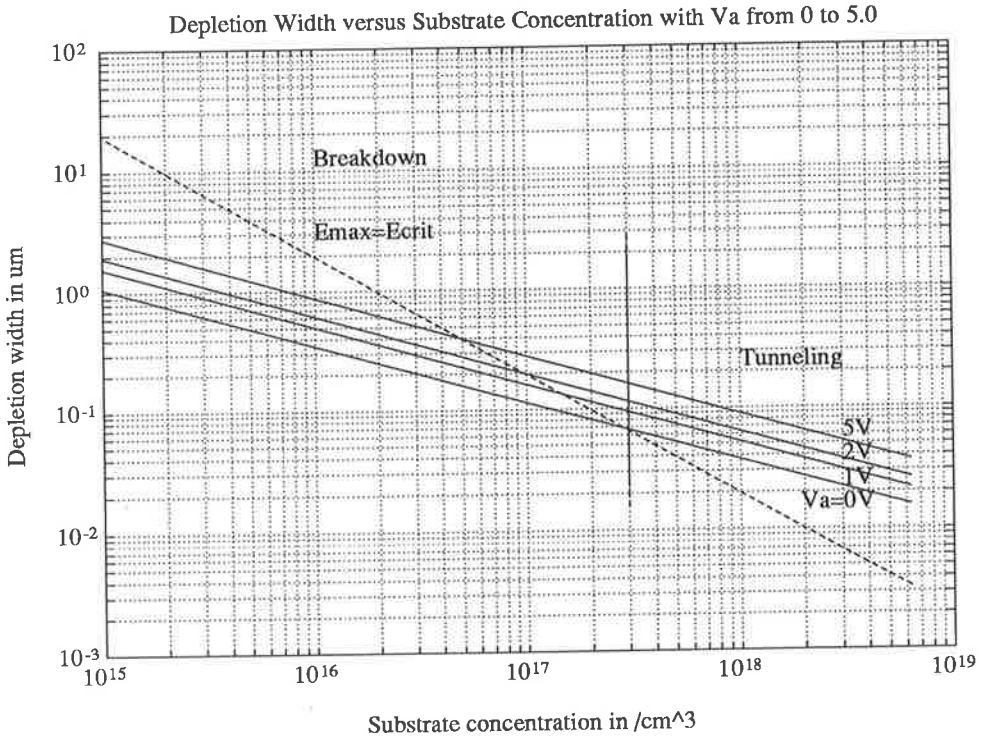


Figure 2.1: Depletion width versus substrate concentration

where E_{max} is the maximum electric field induced in the one-sided step junction. When N_B is increased by α, if $V_a = 0V$, V_B is increased by $\ln \alpha$, and d is decreased by $\sqrt{\frac{\ln \alpha}{\alpha}}$. Therefore, the electric field E across the depletion region is increased by $\sqrt{\alpha \ln \alpha}$. Consequently, the E will reach the E_{crit} with the increasing N_B.

Figure 2.1 shows the depletion width as a function of substrate concentration and supply voltage. The dash line indicates the maximum depletion width when $E_{max} = E_{crit}$. Applying Eq 2.5 to Eq 2.1 yields

$$d = \sqrt{\frac{2\varepsilon_o \varepsilon_{si} \cdot (\frac{1}{2} E_{crit} d)}{q N_B}}$$

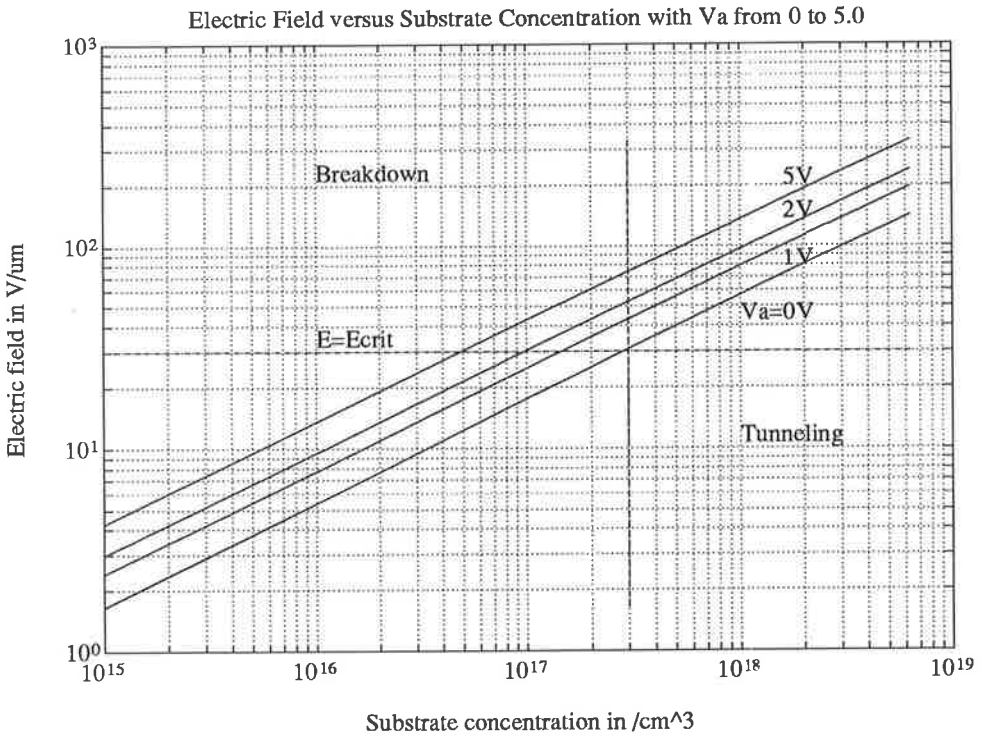


Figure 2.2: Electric field versus substrate concentration

$$d = \frac{\varepsilon_o \varepsilon_{si} E_{crit}}{qN_B} \tag{2.6}$$

In the area above the dashed line, the increased electric field will cause breakdown to happen. The point where the dashed line meets the line of $V_a = 0\text{V}$, represents the maximum allowable substrate doping, which is around $3 \times 10^{17}\text{cm}^{-3}$ when N_D is $1 \times 10^{20}\text{cm}^{-3}$. At higher substrate doping level junction tunneling will happen. Therefore, depletion width of a junction can only exist between the line of $V_a = 0\text{V}$, which indicates the minimum depletion width, and the dashed line.

Figure 2.2 illustrates the maximum electric field in the depletion layer versus N_B. Any supply voltage $V_a > 0\text{V}$ will enhance the field strength and cause breakdown to happen at lower substrate concentrations. In the above discussion, the effects of N_D is relatively small, and was therefore neglected.

2.2.2 Limits of Miniaturisation

The minimum size of a transistor is determined by the process technology and the physics of device itself. The finest geometry and the spacing between lines heavily depend on the alignment accuracy and the resolution of the photolithography technology. The availability of E-beam direct write could push the size of finest lines further down from current limit of $0.3\mu\text{m}$ which is determined by optical pattern generation equipment.

The size of a transistor is usually defined by the channel length. As the channel is scaled down, the depletion region around the source is brought closer to that of the drain. In order to prevent punch through and maintain operation, the channel length L must be kept greater than 2 times of depletion width d which is given in Eq 2.1. L is determined by the concentration of substrate N_B and supply voltage V_a.

Applying the conclusions from the previous section, the minimum possible channel length can be estimated to be 0.14μm. Moreover, the minimum transit time for an electron to travel from source to drain can be calculated. From [SZE]

$$V_{drift} = \mu E$$

where V_{drift} is the carrier drift velocity.

and

$$L = 2d$$

So, transit time

$$T = \frac{L}{V_{drift}} = \frac{2d}{\mu E}$$

Referring to figure 2.2, due to the field strength in the depletion layer being greater than 10^4 V/cm, the carrier drift velocity is approximately equal to V_{sat}, which is 1×10^7 cm/sec [SZE], regardless of the electric field induced by the supply voltage.

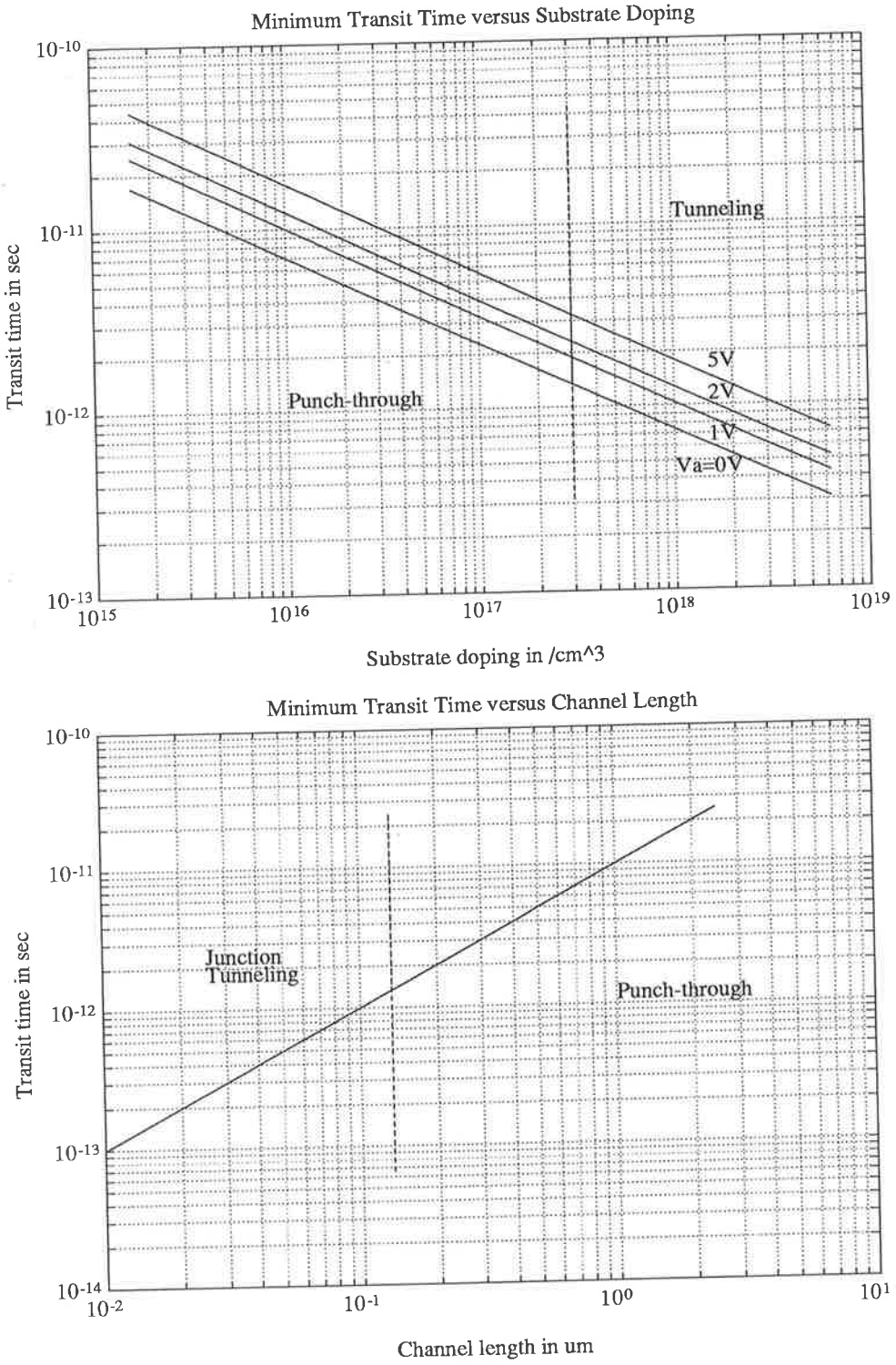


Figure 2.3: Transit time versus substrate doping and channel length

Therefore, the minimum transit time happens at the minimum size transistor when V_a is approaching 0V. Figure 2.3 shows the minimum transit time assuming the transistor size is $2d$ with zero space between depletion regions.

2.2.3 Limits of Interconnect and Contact Resistance

Since the width, thickness and spacing of interconnect are scaled by $1/\alpha$, the cross-section of conductor and contact area are scaled by $1/\alpha^2$. In the case of short distance interconnections, the length of conductor is scaled by $1/\alpha$. So the resistance R is scaled by α. In constant field scaling, current I is scaled by $1/\alpha$, therefore IR drop remains unchanged while supply voltage and logic level is scaled down. That means the IR drop consumes higher ratio of output voltage and degrades driving capability and noise margins.

Together with the decreasing of device dimensions, the level of integration is also increased, which enlarges the die size and lengthens the interconnect from one side of chip to the other. Therefore, both the resistance and capacitance of interconnect are increased, and the RC constant is deteriorated. Propagation delay, signal decay and skew will pull down the maximum operational frequency, even though the shrunk transistors can work with less gate delay.

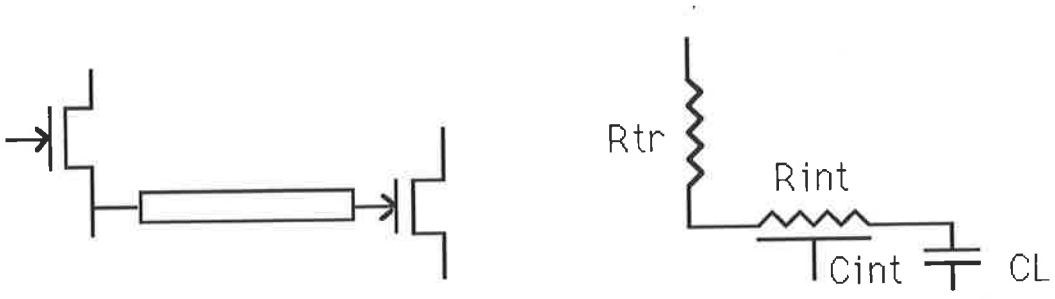


Figure 2.4: Model of metal interconnect

Solutions are introduced to overcome above problems. For instance, multilayers of interconnect with thicker and wider lines can reduce the resistance of a conductor as well as the die size. Cascaded drivers and repeaters are also used to improve the driving capability and minimise propagation delay.

Optical interconnections could be another option for very high speeds and high level of integration. In order to use optical interconnections, optical fibers, laser diodes, receivers and amplifiers must be included in the circuits. Their performance vary with the properties of materials used. In this paragraph only a rough estimation is presented for comparison with metal interconnect. Figure 2.4 shows a model of a metal interconnect and its equivalent circuit. A transistor which R_{tr} is $5k\Omega$ is selected as a output driver. The propagation delay on a single layer aluminium interconnect can be calculated by using approximation equation given by [SAKU]

$$T = R_{int}C_{int} + 2.3(R_{tr}C_{int} + R_{tr}C_L + R_{int}C_L) \tag{2.7}$$

$$T \approx (2.3R_{tr} + R_{int})C_{int} \tag{2.8}$$

$$R_{int} = \frac{\rho \cdot L}{H \cdot W}$$

$$C_{int} = \varepsilon_{ox}[1.15\frac{W}{t_{ox}} + 2.28(\frac{H}{t_{ox}})^{0.222}]L \tag{2.9}$$

where

R_{tr} is the ON resistance of the transistor

R_{int} is the resistance of the interconnect

C_{int} is the capacitance of the interconnect

t_{ox} is the thickness of dielectric oxide

ρ is the resistivity of the interconnect

L, W, H are the length, width, and height of the interconnect

$\varepsilon_{ox} = 3.4515 \times 10^{-5}$ pF/μm is the permitivity of SiO_2

If we use the value in [BAKO], ρ of aluminium is 3$\mu\Omega$-cm, and choose a 0.8μm thick oxide, the propagation delay on a 1μm thick, 3μm wide and 1 cm long wire is given by

$$T = (2.3 \times 5k\Omega + 10k\Omega)2.5 = 53ns$$

Figure 2.5 shows a simplified optical interconnection, in which a laser diode, a

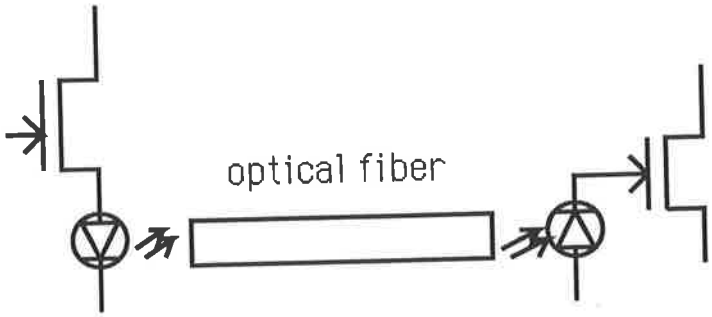


Figure 2.5: Electro-Optical interconnection

segment of optical fiber and a receiver are used to replace the metal interconnect in figure 2.4. R_{int} and C_{int} are assumed zero, and the time needed for the output driver to transfer a logic state is given by

$$T = 2.3R_{tr}C_L + t_{laser} + t_{int} + t_{rec} \tag{2.10}$$

where

C_L is the capacitance of laser diode

t_{laser} is the delay time of laser diode

t_{int} is the propagation delay of interconnect

t_{rec} is the delay time of receiver

and

$$t_{int} = \frac{n \cdot L}{c}$$

where

n is the refractive index of optic fiber material

L is the length of optic fiber

c is the speed of light in free space ($c = 3 \times 10^8$m/sec)

Since both laser diode and receiver can work at frequencies above 10 GHz, the delay time for each of them is estimated to be 100 ps. The capacitance of a discrete laser diode is approximately 1 pF [HOT]. The refractive index of the commonly used materials for optical fibers is about 1.5 to 2.0. Therefore, the total delay time T for a 10 mm interconnect is about

$$T = 2.3 \times 5\text{k} \times 10^3 \times 1 \times 10^{-12} + 1 \times 10^{-10} \times 2 + 2 \times 1 \times 10^{-4}/(3 \times 10^8) = 11.77ns$$

Figure 2.6 show the delay time of various materials of interconnect versus line widths and line lengths. Three different widths are also chosen to demonstrate the effects of scaling on the propagation delay. It is obvious that the longer the interconnect is, the more speed advantage can be acquired by using optical interconnections. In the plot of delay time versus line width, while C_{int} remains independent to line width, R_{tr} dominates the delay time of aluminium interconnect and R_{int} dominates that of a Poly line.

The performance of laser diodes and receivers can be improved, if they are built in an integrated circuit. Gallium Arsenide (GaAs) is the material which can accommodate electronic components and optical interconnection on one chip and make total integration possible.

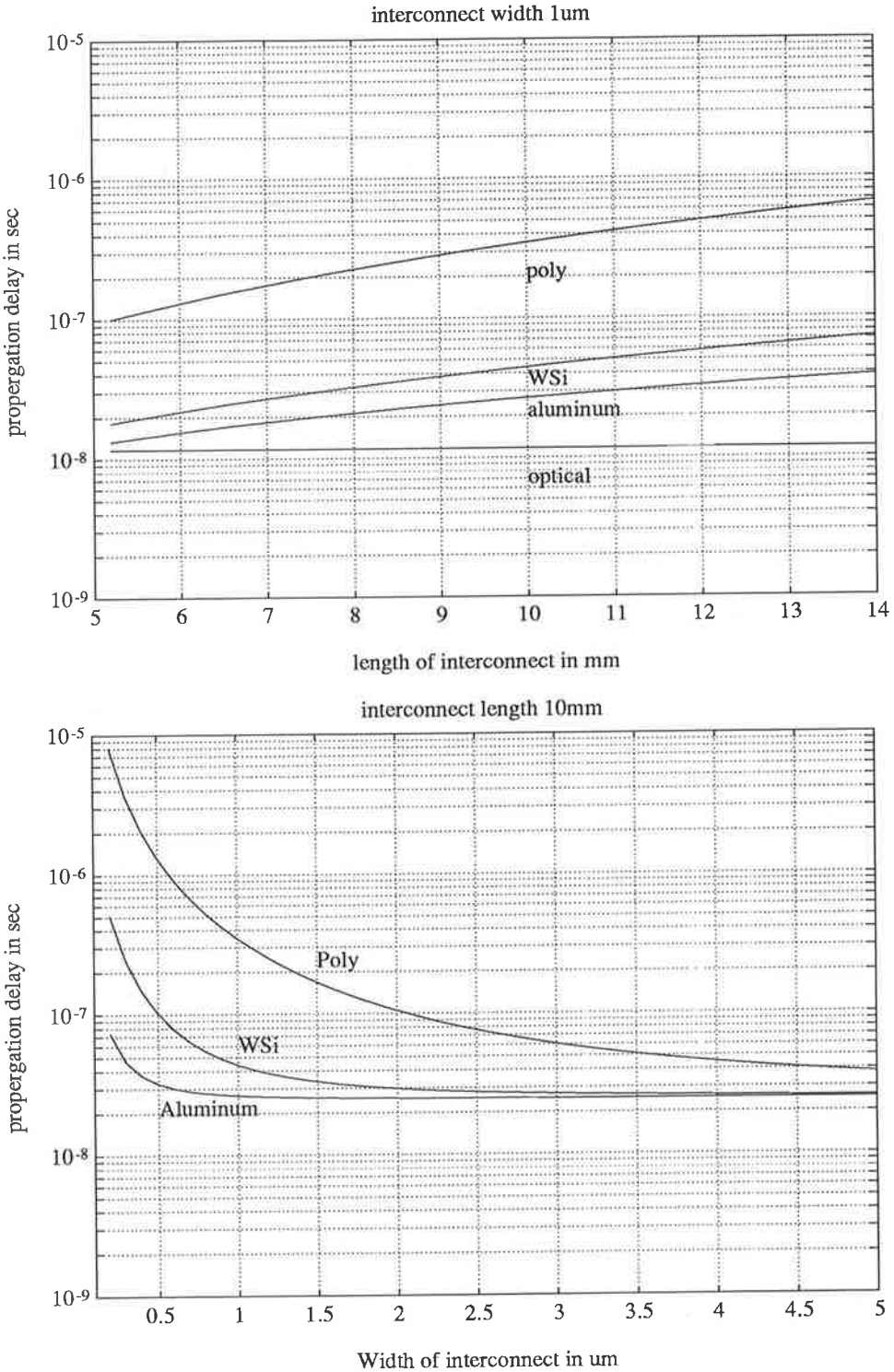


Figure 2.6: The propagation delay versus interconnect length and width. R_{tr}=5 KΩ, H=$W/3$, tox=$W/3$, $\rho_{Al} = 3\mu\Omega$-cm, $\rho_{WSi} = 30\mu\Omega$-cm and $\rho_{Poly} = 500\mu\Omega$-cm.

2.2.4 Limits of Subthreshold Current

One of the major concerns of scaling devices is the effects on subthreshold current I_{sub} which is directly proportional to $\exp^{(V_{gs}-V_t)q/kT}$ [SZE] whereV_{gs} is the voltage across gate and source, V_t is threshold voltage, T is temperature(K), q is electron charge, and k is Boltzmann's constant.

When a transistor is in the off state, the value of $V_{gs} - V_t$ is expected to be negative and as large as possible to minimise the subthreshold current. If V_t is scaled down, the ratio of $V_{gs} - Vt$ to kT will drop and the subthreshold current will increases dramatically. Therefore, V_{gs} and V_t are proposed to be scaled together with supply voltage by $1/\beta$ instead of $1/\alpha$, while α is greater than β in most cases. However this unequal scaling also incurs concerns about increasing electric field and decreasing breakdown voltage.

The maximum electric field across depletion region is given by [GROVE]

$$E_{max} = \frac{2(V_a + V_B)}{d}$$

for a one-sided step junction. As discussed previously, $(V_a + V_B)$ is scaled by $(\beta + m)/(\beta(m+1)$ and d is scaled by $1/\alpha$, E_{max} is scaled by $\alpha(\beta+m)/\beta(m+1)$. Again, if α is greater than β more electric stress will be applied to the depletion regions of shrunk transistors. At the same time, the junction breakdown voltage which is

given by [GROVE]

$$BV = \frac{\varepsilon_{si}\varepsilon_o E_{crit}^2}{2qN_B} \tag{2.11}$$

where

E_{crit} is critical electric field

N_B is substrate doping level

is scaled by $\beta(m+1)/\alpha^2(\beta+m)$, and is decreasing. So, care must be taken to estimate the breakdown voltage of scaled devices. Especially breakdown usually happens at lower voltages at the interface where a corner of diffusion region meets silicon dioxide.

2.2.5 Limits of Logic Level and Supply Voltage by Noise

Shorter gate delay time and low power dissipation are two main advantages of scaling transistors, higher operational frequency and low supply voltage are expected. However, together with the decreasing supply voltage and the spacing between lines and the increasing switching speed, problems of noise, which is either retained in amplitude or amplified, are becoming a serious concern.

Caused by the random motions of the current carriers, thermal noise is a fundamental noise source. In [SAH] the mean-square current fluctuation in the channel

is represented by a equivalent noise resistance R_n at the input and is given by

$$\langle i^2 \rangle = 4kTR_n g_m \Delta f$$

where

k is the Boltzmann constant

T is the absolute temperature in Kelvin

g_m is the transconductance

Δf is the band width

F.M. Klaassen [KLA1] has investigated the thermal noise in a MOS transistor with substrate doping N_B in the range of 10^{14} to 10^{17} cm^{-3}. When the transistor works in saturation the g_m is no longer proportional to the gate voltage V_g, and can be expressed as

$$g_m \approx BV_p$$

where

$$B = \frac{\mu W C_{ox}}{L}$$

and V_p is the pinch-off voltage given by

$$V_p = V_g' - \frac{1}{2}(\frac{a}{C_{ox}})^2[(1 + \frac{4V_g' C_{ox}}{a})^{1/2} - 1]$$

where

$V_g' = V_g - V_t + V_B$

$a = (2\varepsilon_{si} q N_B)^{1/2}$.

V_B is the built-in potential.

Then

$$R_n = (\frac{1}{2}\frac{V_g'}{V_p'} + \frac{1}{6}) g_m^{-1}$$

where $V_p' = V_p + V_B$.

Because V_p is a monotonically decreasing function of the thickness of gate oxide t_{ox} and substrate doping N_B, R_n is a monotonically increasing function of the same parameters. Consequently, the main factor of the thermal noise $R_n g_m$ is expressed by

$$R_n g_m = \frac{1}{2}\frac{V_g - V_t + V_B}{V_p + V_B} + \frac{1}{6} \tag{2.12}$$

which appears to be a strongly increasing function of t_{ox} and N_B, and a weak function of V_g. Figure 2.7 show the experimental results which supports the above theory introduced by F.M. Klaassen.

Considering the effects of scaling for current technology for thin oxide, the effect of N_B is smaller [SAH]. V_p' and V_g' are replaced by V_p and V_g respectively. So, Eq 2.12.

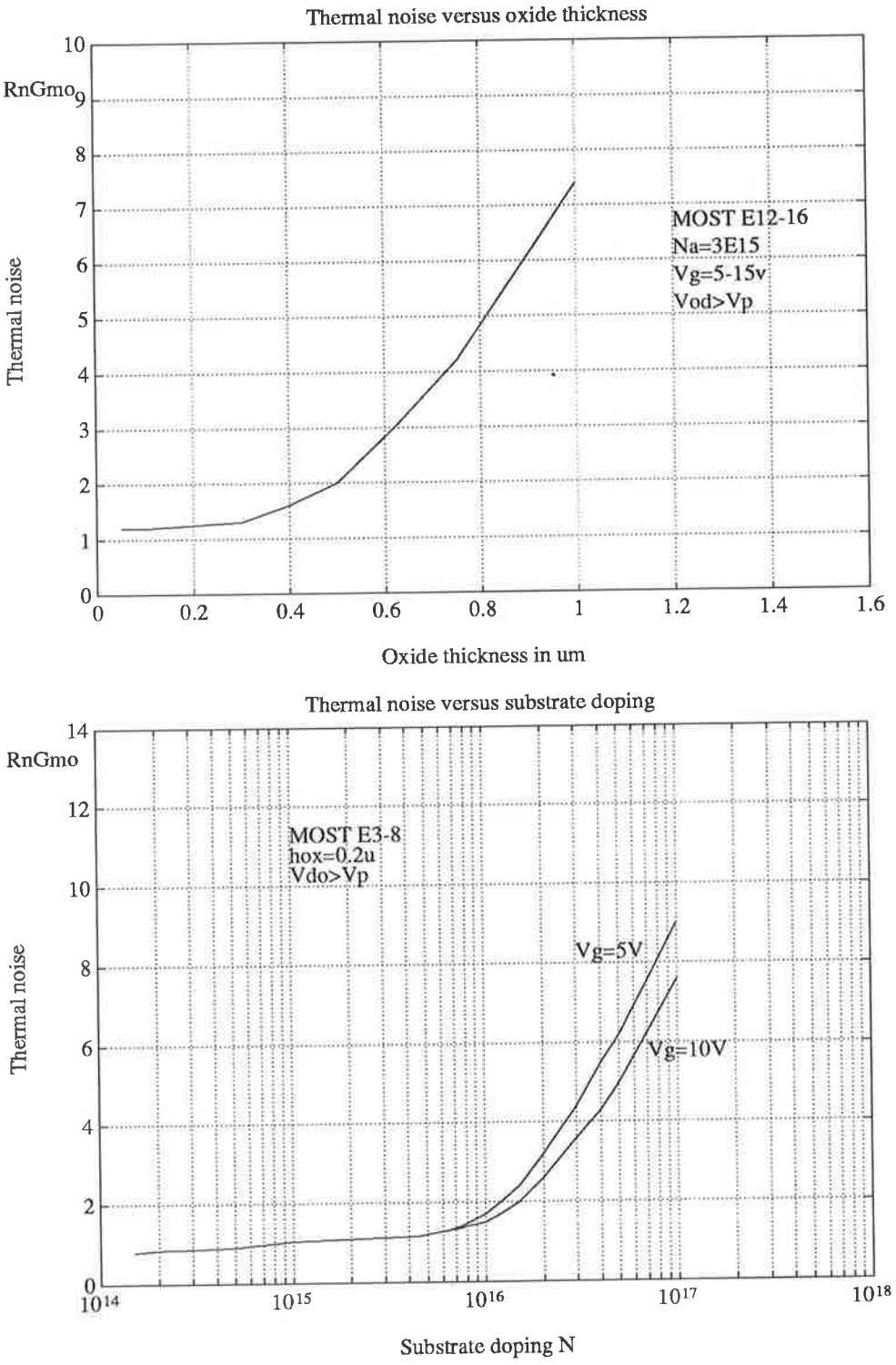


Figure 2.7: Thermal noise versus oxide thickness substrate doping

becomes

$$R_n g_m = \frac{1}{2} \frac{V_g}{V_g - \frac{1}{2}(\frac{a}{C_{ox}})^2(1 + \frac{4V_g' C_{ox}}{a})^{1/2} - 1} + \frac{1}{6}$$

When constant field scaling is applied, V_g is scaled by $1/\alpha$, C_{ox} and N_B are scaled by α. In turn, $R_n g_m$ is only slightly reduced by the increased C_{ox}. Therefore, the ratio of thermal noise to logic level is devastated by almost the same factor of scaling.

Flicker noise has become a subject of many investigations since a model was introduced by A.L. McWhorter in 1956. The noise was observed and explained as a result of the fluctuation of the carriers trapped by surface states in the transistor channel.

In the conclusion of the investigation by F.M. Klaassen [KLA2] the change in the number of the trapped carriers dn_t due to the change in that of induced free carriers dn presents a current fluctuation Δi at the output.

$$\Delta i^2 \approx \frac{q\mu s I V_d}{L^2 f} \tag{2.13}$$

where

$s = \frac{dn_t}{dn}$ is the surface state efficiency

I is the DC drain current

f is the frequency

V_d is the applied drain voltage

Usually, the output noise is represented by an equivalent noise voltage source ΔV at the input [KLA2].

$$\Delta V^2 = \frac{sq(V_g - 1/2V_d)}{C_g f}$$

When the transistor operates in saturation $V_d \approx V_g$. So

$$\Delta V^2 = \frac{1}{2}\frac{sqV_g}{C_g f}$$

where

V_g is the applied effective gate voltage

C_g is the gate capacitance.

Since s is a process dependent factor, the Flicker noise is scaled by 1 or by α^2/β^2 when constant field or combined scaling model is applied. The normalised Flicker noise is increased by at least a factor of α along with the scaling of supply voltage and transistor size. In addition to the two noise sources discussed, noise coupled by mutual inductance and mutual capacitance could be the practical limit to decide the smallest operational voltage.

Considering the cross talk between two parallel signal lines on a chip, the model of coupling presented in [WATTS] shows that the capacitive noise is proportional to $C\frac{dV}{dt}$, where C is coupled capacitance from one line to the other, and $\frac{dV}{dt}$ approximately equals $\frac{V_a}{\tau}$, where τ is the rise time of a signal. The inductance noise

is related to $L\frac{dI}{dt}$, where L is the coupled inductance, and $\frac{dI}{dt} \approx \frac{I_{sat}}{\tau}$. For small capacitive loads, as are usual in MOS ICs, currents which charge up gate capacitors are small, and capacitive coupling tends to dominate. Therefore, the increased operational frequency which in turn reduces τ aggravates the problems of coupling.

External noise may be generated by radio frequencies, voltage spikes, voltage drops on power or ground lines, unterminated signal lines or lines with nonuniform impedance characteristics. While the supply voltage and the logic level tend to be reduced, neither internal nor external noises can be alleviated with the progress of scaling. Thus, the decreasing signal to noise ratio will reduced the yield and the reliability of circuits.

A typical peak to peak noise of at least 100 mV on power supply and ground is observed on well designed multilayer PC boards [LONG]. In order to evaluate the effects of noise on the probability of failure in a circuit, in figure 2.8 the minimum required signal to noise power ratio to operate the circuit is assumed to be 4 units [ESHR], and the noise is assumed zero mean with standard deviation $\sigma = 100$ mV. The probability of failure $Q(x)$ is estimated by integrating the Gaussian Distribution.

$$G(x) = \frac{1}{\sqrt{2\pi}} e^{-\mu^2/2}$$

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{-\mu^2/2} d\mu$$

For example, a supplied voltage (maximum signal level) is 1V, the maximum tol-

erable noise is then 250 mA which is equivalent to 2.5 deviations of noise. When noise level is over 250 mV the circuit will fail. So, the probability of failure is the integral of one tail end of the Gaussian distribution from $x = 2.5$ to infinite.

2.2.6 Limits of Current Density

Due to the increasing level of the integration of a chip, the requirements for low delay time and high operational frequency are also increased. High purity Al seems to be the most promising material for interconnect on VLSI. However, the continuous shrinking of dimensions also increases the current density in conductors by the same factor, if constant constant field scaling is applied.

When current density of Al interconnect approaching $10^6 A/cm^2$, the migration of metal atoms is likely to happen and the lines will be burnt off. Thus, the current density should be kept substantially below the limit. This will restrain the scaling of the dimensions of interconnect.

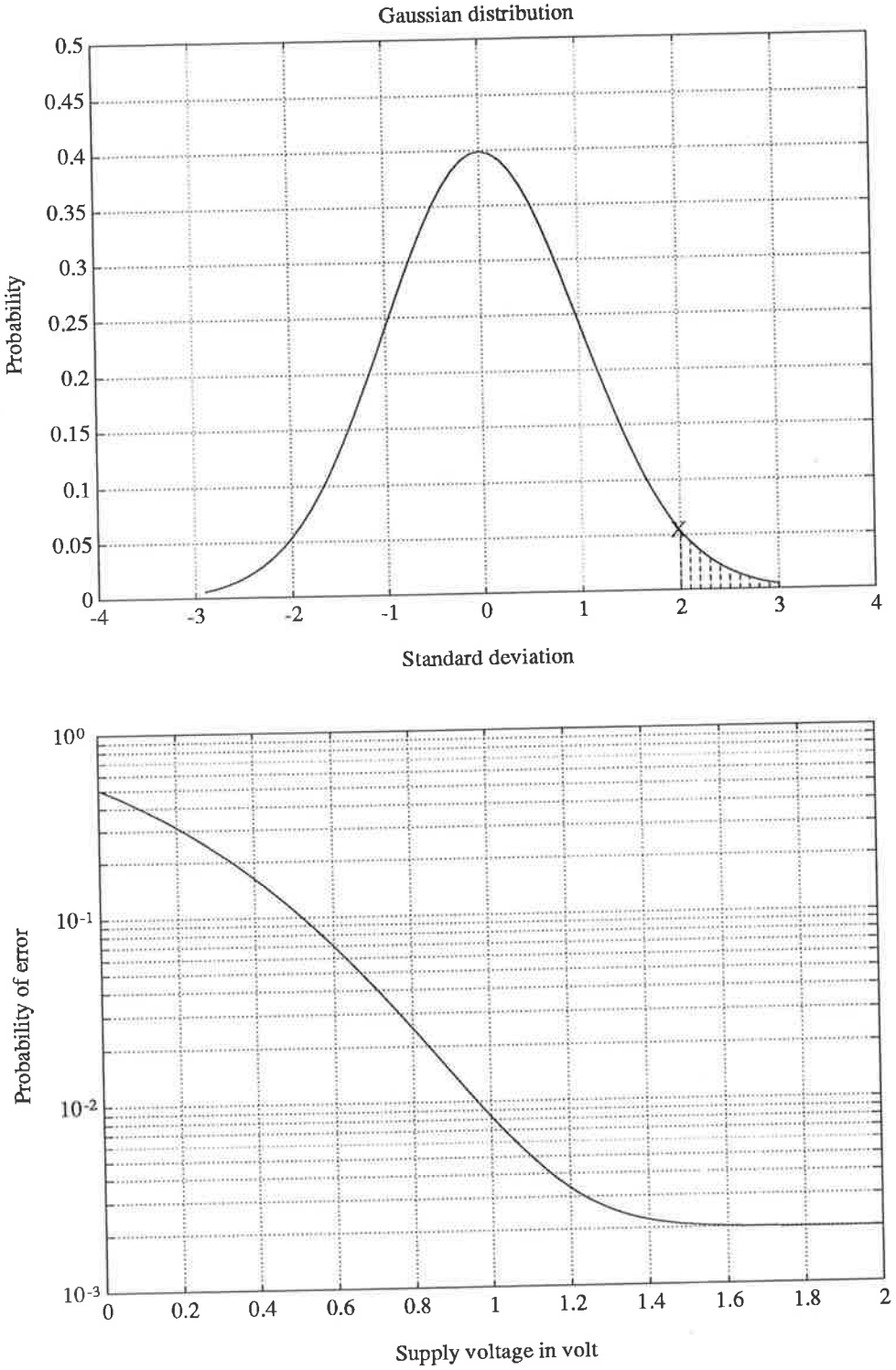


Figure 2.8: Probability of error versus supply voltage. Assuming zero mean noise with σ = 100 mV and the minimum required SNR is 4 units.

2.3 Conclusion

Scaling has not only been developed theoretically, it has also been widely used in manufacturing factories as a direct and simple way of making smaller chips. A 10% or 20% linear shrinkage in horizontal dimensions is very often and successfully implemented in making preliminary products before the real design for smaller devices is ready.

The contributions of scaling is significant, especially in the consideration about power dissipation, switching speed and chip size which in turn determines the production cost. However, the consistent decreasing on dimensions has been pushing the products toward both technological and physical limits.

Investigating the track history, we can find that a generation of microelectronic products is introduced every four years, and the dimensions of devices is reduced by about 20% for each new generation. If the pace is maintained, the possible minimum size of transistors for silicon will be reached in next decade. In order to keep in step with progress, more effort is required toward the development of alternative materials for high speed, low power and high integration microelectronics, such as GaAs and super conductors.

Chapter 3

An ADC design using GaAs technology

3.1 Introduction to GaAs devices

Silicon MOS technology has been the main medium for computer and system applications for years and will continue to fill this role. However, the limitations of speed and power dissipation are becoming apparent at high high levels of intergation and in fast switching applications, which has brought about the need for the development of alternative materials. Much of the developments in material technology

that has paralleled those of silicon, has been related to group II-VI and group III-V compounds, with Gallium Arsenide (GaAs), a group III-V compound showing the most promise. The compound GaAs was first discovered in 1926, but its potential as a high speed semiconductor was not realised until 1960's [ESHR].

3.1.1 Advantages of GaAs over silicon

The advantages of GaAs over silicon as a base material for ICs are: [ESHR][BUSH][SZE] [FIRST] [SIMONS].

a) At normal doping levels the saturated carrier drift velocity for GaAs and silicon are 1.4×10^7cm/s and 1×10^7cm/s respectively. However, the drift velocity of GaAs reaches the peak at a electric field strength around 0.35 V/μm, and then reduces and approaches to the saturated velocity as the electric field strengthens. On the other hand the drift velocity of silicon increases with electric field and the saturated velocity is achieved at a electric field strength about four times that of GaAs. Therefore, up to 70% reduction in power dissipation can be obtained over the fastest silicon technology such as ECL. Figure 3.1 demonstrates this property.

b) Electron mobility in GaAs is six to seven times higher than in silicon. Therefore, GaAs transistors with typical gate lengths of 0.5-1 μm with transit times as short as 10-15 ps, corresponding to current gain-bandwidth products in the range of 15-25 GHz can be obtained. There is a three to five times improvement over silicon devices.

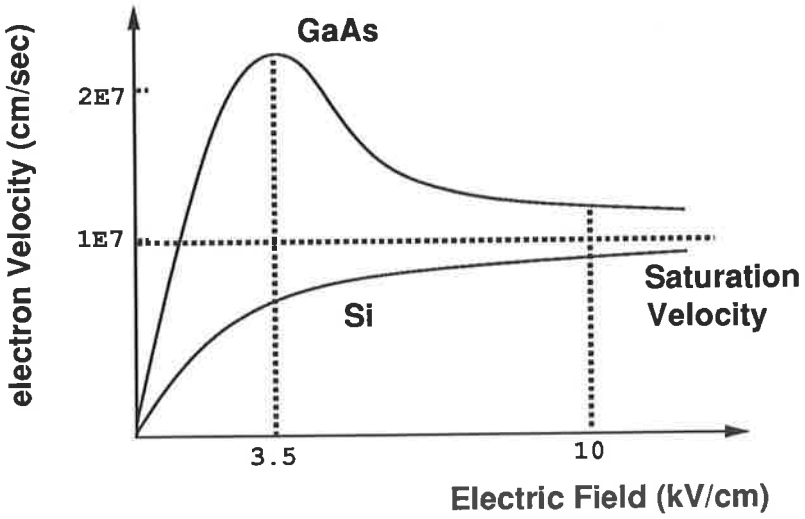


Figure 3.1: The drift velocity in GaAs and silicon

c) Due to the absence of gate oxide to trap charges, GaAs device is more radiation resistant than silicon. Which is an important benefit to the applications in the space where radiation is a major concern for silicon devices.

d) A larger bandgap offers GaAs semi-insulating properties. The high resistivity in the range of $10^7 - 10^9\Omega$-cm at room temperature is another advantage for high performance devices. It not only minimises the parasitic capacitances but also reduce the leakage current between devices on the same substrate as it is in silicon.

e) A wider operating temperature range is possible due to the larger bandgap. GaAs devices are tolerant of wide temperature variations over the range -200 to +200 °C.

f)Schottky barriers can be realised on GaAs with a large variety of metal such as aluminium, platinum and titanium, leading to high quality Schottky junctions with excellent ideality factors (less than 1.1) and fairly low reverse currents (< 1 A/cm^2).

Properties	GaAs	Silicon
Electron mobility (cm^2/Vs)	5000	800
Maximum electron drift velocity (cm/s)	2×10^7	1×10^7
Hole mobility (cm^2/Vs)	250	350
Energy gap (eV)	1.43	1.12
Type of gap	Direct	Indirect
Density of states in conduction band (cm^3)	5×10^{17}	3×10^{19}
Maximum resistivity (Ω-cm)	10^9	10^5
Minority carrier life time (s)	10^{-8}	10^{-3}
Breakdown field (V/cm)	4×10^5	3×10^5
Schottky barrier height (V)	0.7-0.8	0.4-0.6

Table 3.1: The comparison of the physic properties of silicon and GaAs

g) The direct bandgap of GaAs allows efficient radiative recombination of electrons and holes, meaning that forward-biased p-n junctions can be used as light emitters. Thus, efficient integration of electrical and optical functions is possible.

A summary of the electric properties of silicon and GaAs is given in Table 3.1 [GLOA].

3.1.2 Technologies of GaAs

Having discussed the superior performance potential of GaAs material compared with silicon, we also need to consider the development of GaAs device technology which realise designs and utilise the advantages of GaAs effectively. During the last few years a number of different devices have been developed for GaAs. They fall

into two categories, the first and second generation [ESHR]. First generation devices include:

- depletion-mode metal-semiconductor field-effect Transistor, DMESFET;
- enhancement-mode metal-semiconductor field-effect transistor, EMESFET;
- enhancement-mode junction field-effect transistor, EJFET;
- complementary enhancement-mode junction field-effect transistor, CE-JFET.

First generation GaAs gates exhibited switching delays as low as 70 to 80 picoseconds for a power dissipation in the order of 1.0 mW to 0.2 mW.

The second generation devices are:

- high electron mobility transistor, HEMT;
- heterojunction bipolar transistor, HBT.

Due to better exploitation of the GaAs, electron mobility in second generation transistors can be up to five times greater than in the first generation. Therefore, very fast devices are possible. For example the operation frequency of DFETs, in general, is between 20 to 80 GHz and for HEMTs it can very from 70 to 100 GHz [BUSH] [SWAN].

Parameter	MESFET	HEMT	HBT	SI BIPOLAR	UNIT
f_T	15	20	30-40	5-10	GHz
f_{max}	35	50	25	15	GHz
$C_{DS} + C_{Dsub}(C_{csub})$	0.25	0.25	($\ll 1$)	(1)	fF/μm
$C_{ds}(C_{bc})$	0.2	0.2	2	2	fF/μm
Complexity	1	-	-	3-10	transistor
g_m	150	200	2000-4000	3000	ms/mm
$V_{gs}(V_{BE})$ match	5-20	5-20	(1)	(< 1)	mV
$I_g(I_b)@I_D = I_C = 1$ mA	$\ll 1$	$\ll 1$	25-50	12	μA
$BV_{DS}(BV_{CE})$	6-10	6-10	8-10	(8)	V
$1/f$ noise	40	40	3	1	μV
Hysteresis	20	10	< 1	$\ll 1$	mV
$\star$ data in () is not certain; '-' means data is not available					

Table 3.2: The performance comparison of GaAs devices

3.1.3 Comparison of GaAs device performance

To better understand the suitability to applications of different GaAs devices a technology/device comparison is given in Table 3.2 using bipolar silicon technology as a reference [KEN]. The values selected for the table are typical of current capability or achievable without further development work. As it is shown in this table, all the GaAs devices offer much higher unity gain cut-off frequency f_T and maximum frequency of oscillation f_{max} and lower parasitic capacitance than silicon technology. Among GaAs devices, HBT gives the highest value of transconductance which makes possible the gain of a transistor as high as in bipolar silicon.

Circuit parameters	MESFET	HEMT	HBT	SI BIPOLAR	UNIT
Speed (50dB harmonic)	0.1-2	0.1-3	0.1-2	0.01-0.2	Gsps
Linearity	50-80	50-80	-	50-90	dB
Droop (C_H=1 pF)	1	1	5-50	2-10	mV/ns
Offset	50	50	10	5	mV
Hysteresis	10	5	< 1	< 1	mV
Noise (BW=3GHz)	0.2	0.2	0.2	0.1	mV

Table 3.3: The comparison of GaAs devices

In Table 3.3 GaAs devices/technologies capabilities for implementing flash quantizers is compared. It demonstrate an order of magnitude increase in sampling rate over their silicon counterpart in the comparison of sampling and hold circuit performance. In this table, MESFETs and HEMTs demonstrate their superiority of low droop as well as the disadvantages of offset and hysteresis.

In the above comparisons, HBT presents a superior capability in high speed applications. However, the most important factor in the implementation of high speed VLSI circuits, apart from high operating frequency, is the maturity of the process which in turn determines the manufacturing cost and reproducability. At present the first generation MESFETs pose the least problems in processing [ESHR], so they are the most widely used devices for VLSI applications. They can be easily manufactured at sub-micron level and provide high operation frequencies.

3.1.4 The fabrication process of MESFETs

Since the GaAs substrate is a semi-insulator, in the fabrication process for MESFETs, a conductive layer is usually formed on the top of the substrate by implanting silicon atoms into the substrate, while HBT and HEMT devices require molecular beam epitaxy to grow the conductive layer. A typical process of manufacturing MESFET ICs is described in figure 3.2. Also the symbols and structures of enhancement MESFETs and depletion MESFETs are shown in figure 3.3 [ESHR].

The GaAs MESFET has demonstrated its superior performance in the applications of high speed IC. Also, the process maturity of GaAs is reaching the level where real VLSI (>20,000 transistors) is possible [BUSH].(information says that a 1.4 million devices ASIC is fabricated in Vitesse recently). In the applications of very fast analog ICs, GaAs ADCs have achieved 3 GHz with 150 mW [DUCO] and 2.2 GHz with 320 mW for its analog circuit and 730 mW for buffers. But, they offer only four bit and five bit resolution respectively which is less accurate than silicon technologies can reach. Lying behind this are the reasons why GaAs IC can not parallel silicon technology in the applications of analog circuits.

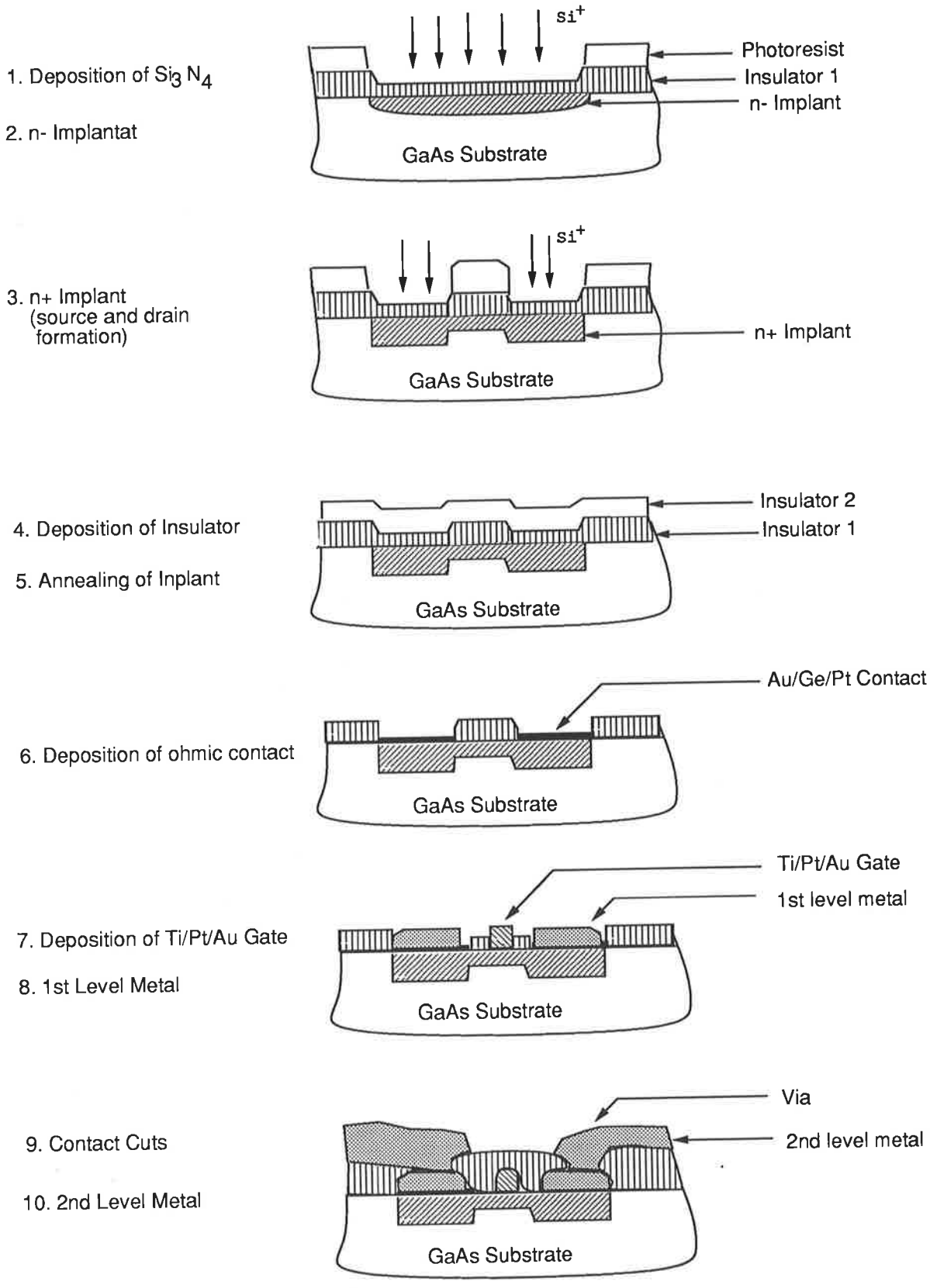


Figure 3.2: The typical MESFET process

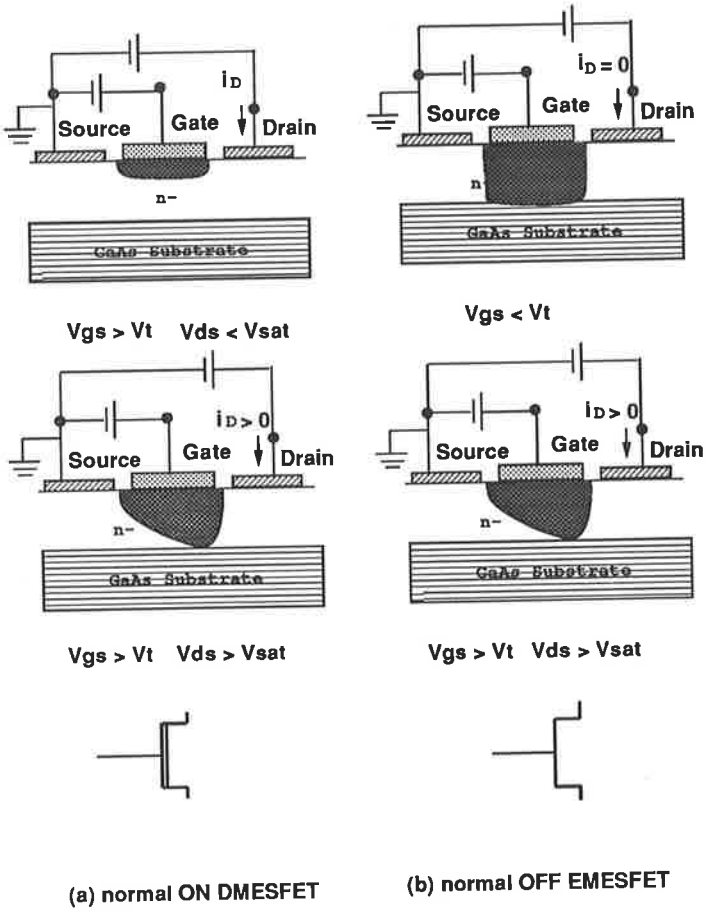


Figure 3.3: The symbols and profiles of MESFET

3.1.5 The disadvantages of GaAs over silicon

The driving force of analog signal processing market is the accuracy with speed. This market is currently dominated by Si MOSFET and Si bipolar technologies. For most applications of data converters and other analog signal processing circuits they require a minimum of 6-8 bits resolution and absolute accuracy [BAYR]. Circuit design using standard GaAs technologies are hard pressed to meet this accuracy criteria. There are many factors which limit the accuracy of GaAs circuits.

- frequency dependent voltage gain
- high offset voltage
- lack of device isolation
- high MESFET $1/f$ noise (higher than bipolar)
- low transconductance
- limited input range

Because there is no gate oxide to isolate gate metal and the underneath conductive channel as it is in silicon MOS, the Schottky junction formed by the gate and the channel can be easily forward biased and large gate current will flow through. This limits the gate to source voltage in the range of 0.7-0.8V depending the gate metal used. Consequently, this increases the difficulty for GaAs devices to match the operation conditions of existing silicon ICs and to be included in systems.

GaAs MESFETs like Si MOSFETs have a very small transconductance compared to Si bipolar (table 3.2). Therefore, voltage gains of MESFETs as high as Si bipolar is not possible. The typical voltage gain of a Si bipolar transistor is 120 dB, where MESFET op amp's are usually limited to 60-80 dB [BAYR].

The $1/f$ noise in GaAs MESFET technology can be 100 times greater than Si bipolar at low frequencies and the noise corner in Si bipolar is typically 100 Hz while it can be as high as 100 MHz in MESFETs [FOLK][BAYR].

The problems associated with the lack of isolation are known as the backgating and sidegating effects. Depicted in figure 3.4, the effects are mainly caused by the capacitive coupling of the channel of a MESFET to the floating substrate. Then the substrate can modulate the drain current of the FET as a backgate, and the adjacent devices as a sidegate[BAYR]. The remedy is to place transistors further away from each other. Unfortunately, this conflicts with the technique used to put devices in close proximity for good matching. Nonetheless, the above three factors causing low accuracy are categorized as second order effects compared to the offset and drain lag effects.

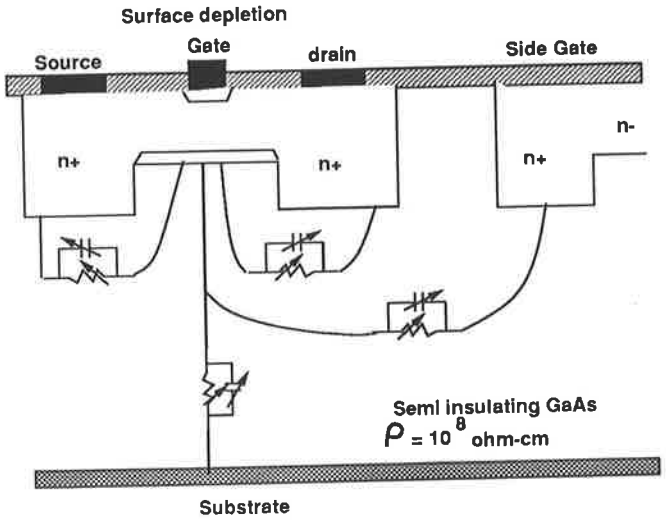


Figure 3.4: The backgating and sidegating effects of GaAs FETs

3.1.6 The Hysteresis and Offset of GaAs MESFETs

As a direct consequence of the floating backgate, the drain current is modulated and a long transient decay time (1 ms - 1 sec) can be observed when the drain voltage is changed by an AC input signal [BAYR]. This effects also causes the looping seen in the current-voltage characteristic by using a curve tracer and in the transfer curve of a inverter [BAYR]. Figure 3.5 exhibits the hysteresis effect in the transfer curve of an inverter operating at 1 KHz. Until present time, this effect has limited the development of high accuracy A/D converters[BAYR].

Although, the mechanism of hysteresis is not yet clear, it seems that the mobile charges trapped at the interface of channel and underneath the substrate is the main cause of hysteresis and drain lag. As a result of the investigation done by

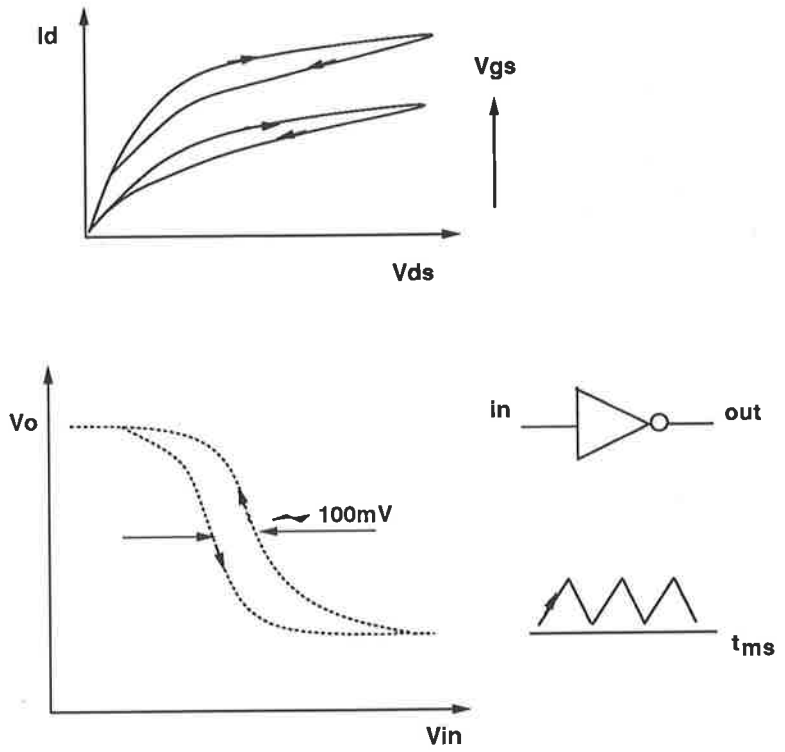


Figure 3.5: The hysteresis of an inverter

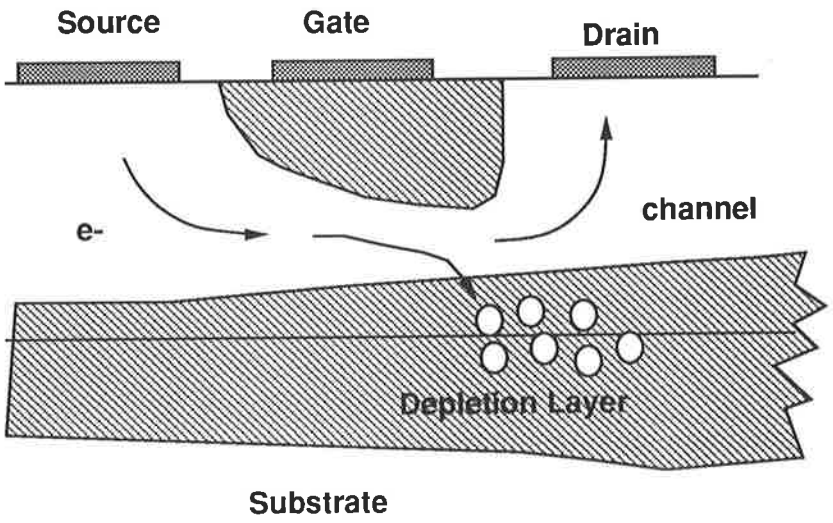


Figure 3.6: The trapped charges at deep channel

LEP, a research organisation of the Philips group, hysteresis is not only frequency dependent, it also strongly depends on V_{gs} and V_{ds} which fix the electric field conditions at the interface (figure 3.6) [DUCO3]. Due to the lack of good models which can effectively characterise the behaviour of hysteresis, this effect is hardly included in the design simulations. The consequences of hysteresis appearing in a circuit is an uncertain drain current when the V_{gs} is fixed or an uncertain V_{gs} when drain current is imposed. In the case of fixed V_{ds}, more drain current can be expected when the V_{gs} is going upward [LAU]. The normal way of reducing the problems is to restrict the swing of the drain-to-source voltage by using cascoding structure or common mode feedback [KATSU].

Offset is caused by a mix of threshold variation, component mismatch and low frequency $(1/f)$ noise. Normally, the threshold variation as a result of process and material nonuniformity is the main contributor to offset. An offset voltage gives an unbalanced intrinsic bias to the devices in different parts of a circuit. This incurs initial voltage and current shift and reduces the noise margin of logic circuits and the accuracy of analog circuits. It is also directly related to the design yield and the achievable resolution of an ADC circuit (figure 3.7[LEP]). The achievable resolution is given by $FSR = 2^N \cdot 6 \cdot \sigma_{offset}$ where FSR is the full scale range of the input, σ_{offset} is the offset variation, N is the achievable bit count, and $6\sigma_{offset}$ is the minimum distance between two adjacent logic states (1LSB) for them to be resolved. The design yield can then be estimated by the integral of Gaussian distribution function

G(x)

$$G(x) = \frac{1}{\sqrt{2\pi}} e^{-x^2/2}$$

$$P_\Phi = \int_{-3}^{+3} G(x)$$

$$P_N = P_\Phi^{2^N}$$

where x is the offset value in term of σ_{offset}. So P_Φ is the offset related yield of a single gate and P_N is the yield of a N bit ADC . If for some reasons, $1LSB < 6\sigma_{offset}$, (i.e. 1 LSB $= 4\sigma_{offset}$,) then the single gate design yield will become $P_\Phi = \int_{-2}^{+2} G(x)$. We can define $V_{offset} = 3\sigma_{offset}$ and to have good yield, V_{offset} should be less than 1LSB.

At the present stage, large threshold variation is still an important issue for the process engineer to overcome, and the effects can only be reduced by design techniques.

3.2 The ADC architecture

In the previous discussion, the performance of various types of ADC architectures have been compared. Flash, subranging and pipeline are three possible candidates for high speed applications.

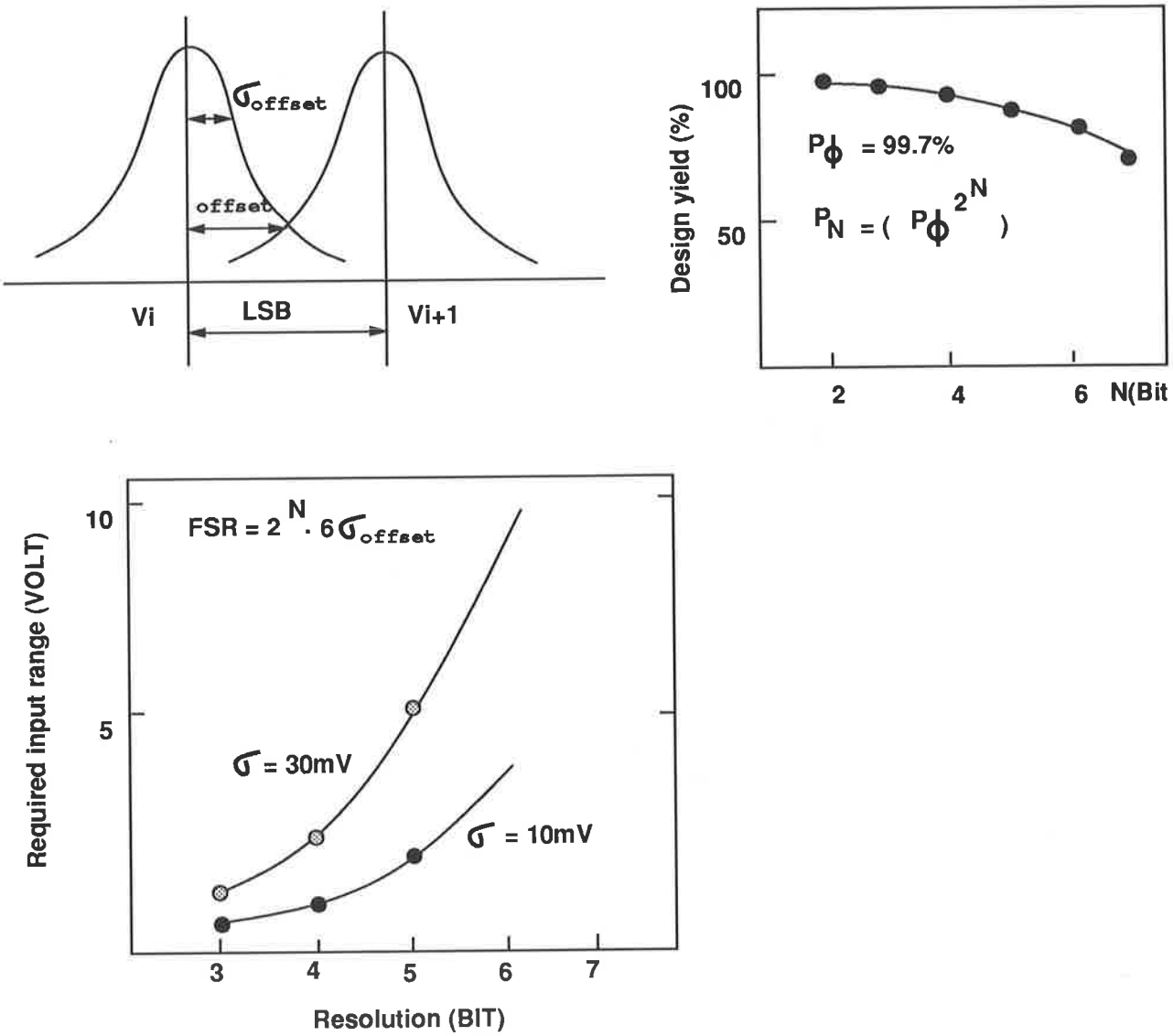


Figure 3.7: Design yield and resolution versus offset

The flash architecture will be restricted to low resolution applications by the number of components it uses. Pipeline converters are limited to medium accuracy applications by the errors in the multiplication and subtraction subcircuits.

Therefore, the subranging architecture appears to be the most promising candidate for the task which aims to design an 8-bit 1 Gsample/second analog to digital converter operating over a 1V input range.

3.2.1 The configurations of the ADC

To reach this target, following configuration must be included in the design;

- offset cancellation
- hysteresis reduction
- at least 16 comparators
- 256 reference voltages
- sample and hold (S/H)
- overall gain >= 100

As explained in the previous section offset voltage and hysteresis are two main obstacles to be overcome before the specified accuracy can be achieved.

In a subranging converter, $2^{N/2}$ comparators are needed to perform the coarse comparison and the subsequent fine comparison. Therefore, 16 comparators are required for an 8- bit ADC. At the same time, $2^N = 256$ quantization levels must be generated to be compared to the input voltage.

Due the high speed and accuracy requirements, clock skew in the input path will be a important contributor to performance degradation. So, a sample and hold (S/H) is necessary in this design. However, the realisation of a high performance S/H is as complicated as the design of the ADC itself, moreover a GaAs S/H circuit has already been developed. Therefore, it is not included in this project.

In addition to offset cancellation and hysteresis reduction a high output gain of the comparator is another key factor to the required resolution. When input dynamic range is 1V and the logic output range is 8-bit, the circuit must be able to resolve 4 mV input change, in other word 1 LSB = 4 mV. However, an error measure less than $\frac{1}{2}$LSB is usually desired in a design.

Meanwhile, the expected output load of this design is a GaAs logic gate, which the input range is from 0 to 0.7V, and a 0.2V swing above and below the threshold point is the minimum requirement for the input device to drive the logic effectively.

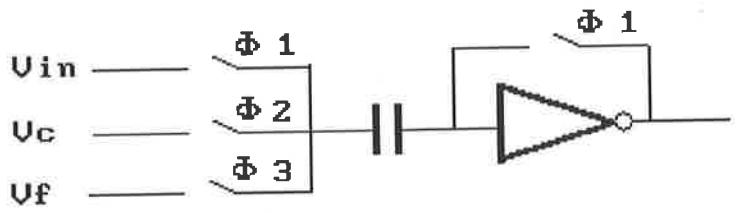


Figure 3.8: A simple comparator

Therefore, an output gain greater than 100 is necessary.

3.2.2 The reference sampling comparator

A very simple and commonly used way to carry out the function of a comparator is to use an inverter together with a few switches and a coupling capacitor. Figure 3.8 [HOSO] shows the structure of this comparator. In the operation of this circuit, assuming it is the Kth comparator of a ADC and $X \cdot V_r/16 < V_{in} < (X+1) \cdot V_r/16$, V_{in} and the offset voltage will be stored at the input capacitor, which performs the self calibration, in the first phase. Then, during phase 2 the coarse reference voltage $Vc = K \cdot V_r/16$ is sensed, and a change of $V_{in} - K \cdot V_r/16$ will appear at the input of the inverter through capacitor coupling. This performs a coarse comparison. In phase 3 the fine reference voltage $Vf = X \cdot V_r/16 + K \cdot V_r/256$ will be chosen base on the result of the coarse comparison to replace Vc and $V_{in} - (X \cdot V_r/16 + K \cdot V_r/256)$ will be detected at the inverter input, and a fine comparison is performed.

This scheme is simple and only a small number of devices are used. However, the input capacitor of each comparator needs to be charged or discharged by the input devices at the beginning of every operation cycle. Therefore 16 capacitors are driven by an input source which may be a S/H. That makes the RC constant of the input path large and will slow down the operation. Moreover, the sizes of the switches must be large as well and the complexity of the S/H will be increased. Another major disadvantage of this scheme is its sensitivity to noise.

In order to reduce the sensitivity of the comparator circuit, a differential amplifier is adopted. Due to the symmetry structure, most of the common mode noises will be cancelled. To decrease the capacitive load seen by the input devices, a "Reference Sampling" structure is designed and demonstrated in Figure 3.9.

In this circuit, the offset voltage and the coarse reference voltage are stored at 2 input capacitors C1 and C2 in phase one. This performs the self calibration.

$$V_{c1} = K \cdot V_r/16 - V_{cal}^{+}$$

$$V_{c2} = K \cdot V_r/16 + V_{cal}^{-}$$

$$V_a - V_b = V_{cal}^{+} - V_{cal}^{-} = V_{cal}$$

where V_{c1} and V_{c2} are the voltages across the two input capacitors respectively. $V_{cal}+$ and $V_{cal}-$ are the voltages induced by the offset voltage at the comparator plates of the capacitors at the end of self calibration period. V_a and V_b are the voltages at

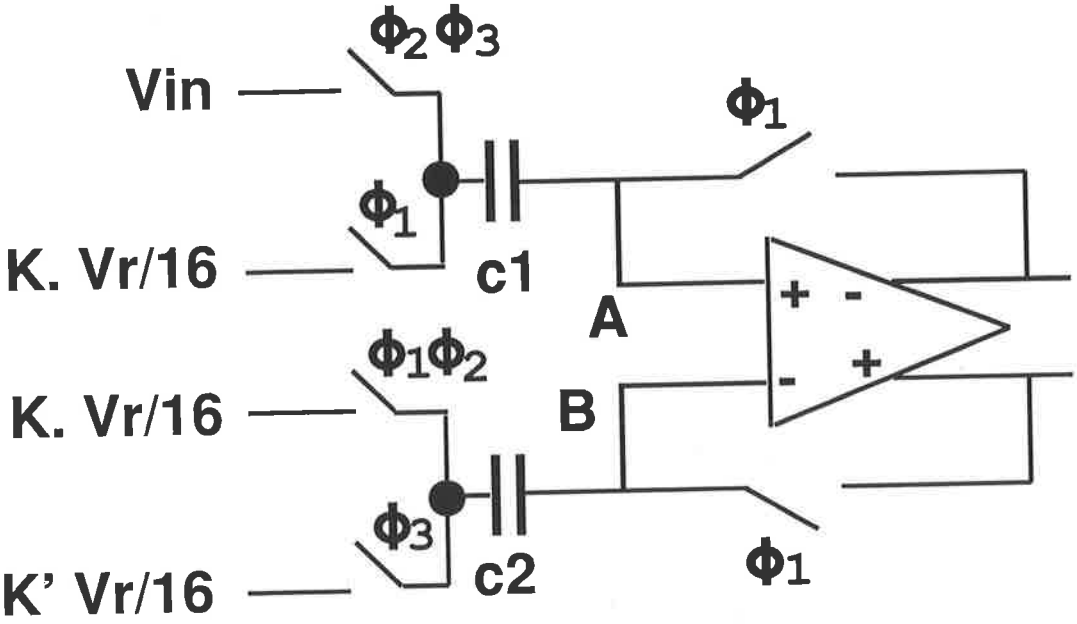


Figure 3.9: The reference sampling structure

the positive and the negative input nodes of the comparator.

During phase 2, V_{in} is sensed at the left plate of C1 and a change of $V_{in} - K \cdot V_r/16$ is coupled to the positive input of the comparator while the negative input is retained. Thus

$\Delta V_a = V_{in} - K \cdot V_r/16$

$\Delta V_b = 0$

$V_a - V_b = V_{in} - K \cdot V_r/16$

and the coarse comparison is performed.

In phase 3, the level at the left plate of C1 and node A remains unchanged while that of the left plate of C2 is switched to $X \cdot V_r/16 + K \cdot V_r/256$. So

$\Delta V_a = 0$

$$\Delta V_b = X \cdot V_r/16 + K \cdot V_r/256 - K \cdot V_r/16$$

$$V_a - V_b = V_{in} - (X \cdot V_r/16 + K \cdot V_r/256)$$

and the performance of the fine comparison is completed.

The most important advantage of this structure is that the input capacitors are charged up by reference voltages at the initiation stage only. Then, due to charge conservation of the capacitors, provided the leakage is negligible, it takes negligible time to change the voltages at the left plates of the capacitors and the input nodes of the comparators in the operations to follow. The theoretical derivation is attached in Appendix A.

The self calibration cycle is still needed to refresh the charges in the capacitors, but the load seen by the input driving devices is reduced dramatically. This increases the input response, simplifies the S/H and reduces the size of the switches and power consumption.

In addition, the symmetrical differential structure also suppresses the common mode noise and minimise the effect of power supply noise and clock feedthrough which are of major concern in non-symmetrical structures.

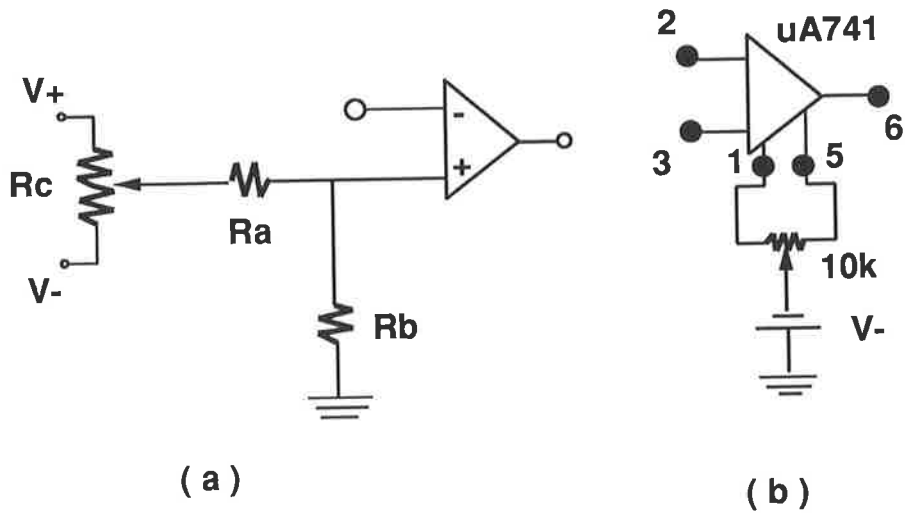


Figure 3.10: Examples of offset nulling circuits

3.2.3 The offset cancellation scheme

In many analog circuit designs offset cancelling circuits are included. A very popular technique is to use a nulling resistor to cancellation the offset between two inputs of differential amplifiers. A example is displayed in figure 3.10. In figure 3.10.a R_a and R_b are used as a voltage divider. The voltage at the positive input node can be varied by adjusting the potentiometer until the output is zero volts. Figure 3.10.b is the pin connection of the operational amplifier. The disadvantage of this scheme is that it requires manual operation to perform the offset cancellation through a external potentiometer. So, it is not suitable for high end monolithic applications.

Another offset cancellation technique used in integrated circuit design is shown in figure 3.11. In this scheme, the offset voltage of each differential amplifier is detected by an internal subcircuit. The data is stored and then used to generate a

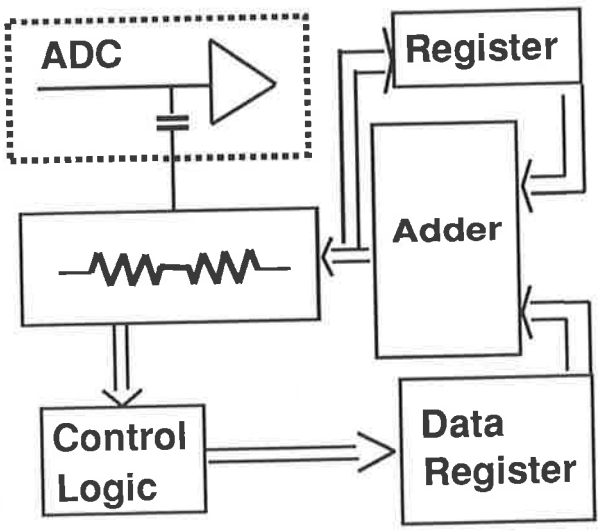


Figure 3.11: Block diagram of an offset compensation ADC

compensation voltage usually by a digital to analog converter. Memory and complex logic circuits are often included. This may generate more source of errors and higher power consumption. Therefore, a self calibration scheme instead of an offset compensation circuit is selected in the design of the comparator structure.

The main idea of offset cancellation is to bring down the output differential voltage $V_o = V_{od}$ which is incurred by the offset voltage appearing as an equivalent input differential voltage $V_{id} = V_{off}$.

Figure 3.12 expresses that when the feedback switches of the differential comparator presented in figure 3.9 are closed for self calibration and the output nodes are connected to the input nodes, $V_{od} = V_{id} = V_{cal}$ will be achieved if the feedback

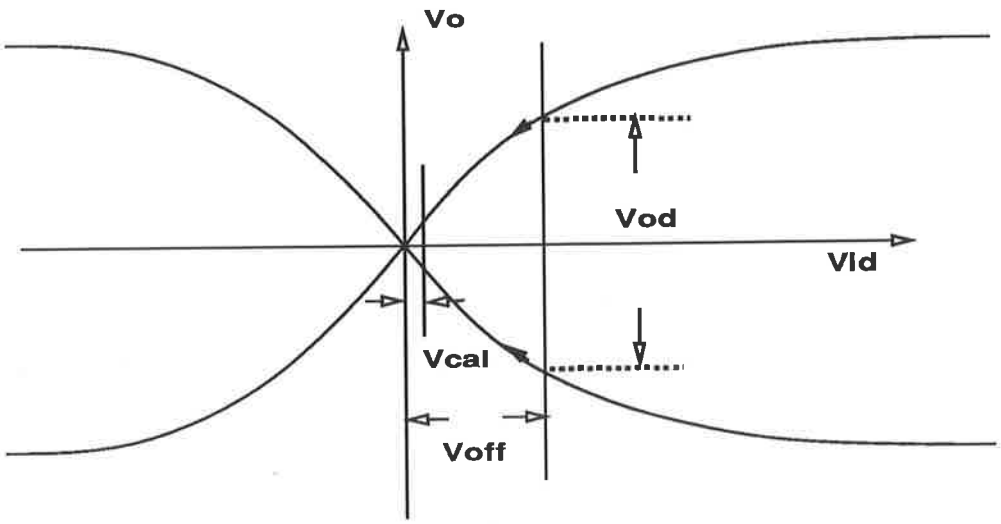


Figure 3.12: The diagram of offset cancellation

loop contains no resistance. Eventually, a very small value of output differential voltage remains and the effect of offset is almost cancelled. Only when the gain of the differential amplifier is infinite the remaining V_{od} or V_{cal} will reach 0V.

3.3 The realisation of the ADC in GaAs

3.3.1 Technology used

Normally different process are needed to fabricate digital and analog ICs. For ADC ICs both analog and digital circuits are integrated in one chip. Therefore a special process is required to build ADC chips. In this research, the ER07AD pro-

cess of Philips Microwave Limited (PML France) is selected. This process features enhancement-mode MESFET, diodes, capacitors and resistors. Depleted type transistors were not available until the design of the comparator was completed.

The main DC parameters of this process are:

Threshold voltage $V_t = +0.175$V

Drain-Source current $I_{dss} = 60$ mA/mm @$V_{gs} = +0.7$V, $V_{ds} = 2$V

Transconductance $G_m = 210$ mS/mm @$V_{gs} = +0.7$V, $V_{ds} = 3$V

Unity current gain frequency $F_t = 17$ GHz

Gate capacitance $C_{gs} = 1$ pF/mm

The large signal model and the parameters for simulation are shown as follow;

Level = 2, Alpha = $4.42V^{-1}$, Lambda = 0.1166, Tou = 4 ps,$V_{TO} = 0.217$, CGSO = 0.39E-15, CGDO = 0.26E-15, Beta = 2.59E-4, $C_{ds} = 0$, $R_g = 0.06\ \Omega$, I_s = 2E-14, N = 1.35, Fc = 0.875, Vbi = 0.324, M = 0.258, UT = 25.25 mV/@20°C, $R_s = 1.7$ kΩ, $R_d = 1.7$ kΩ, B = 0

Above parameters are based on 1 μm gate length. In this model Cd, Cs and Cg re external parasitics, Rg, Rs and Rd are the access resistance. Total gate width $W = N_{bd} \times W_u$, where N_{bd} is the number of gate fingers and W_u is the gate width of each finger in μm. The simulation parameters are for Curtice model for which the equation of Drain-Source current is defined by

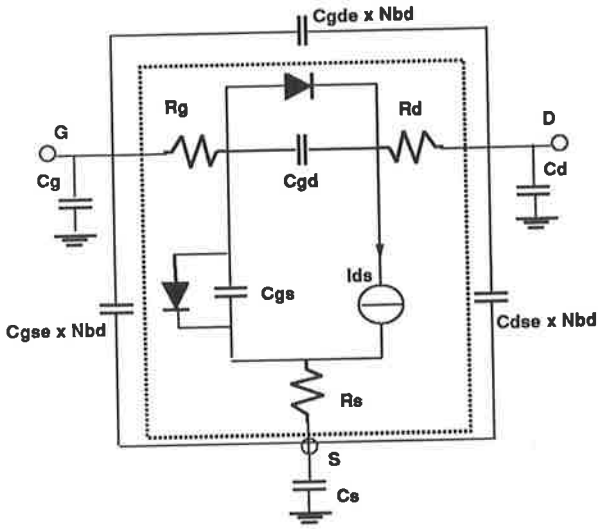


Figure 3.13: The PML model for GaAs EMESFET

$$I_{ds} = \beta \cdot (1 + \lambda \cdot V_{ds})(V_{gs} - V_{to})^2 \cdot tanh(\alpha \cdot V_{ds})$$

for $V_{gs} > V_{to}$

where V_{to} is the threshold voltage, λ is to modulate the Drain-Source conductance in saturation. The use of 'tanh' function is an efficient way of accounting for the early saturation effect by the use of the α coefficient.

The Gate-Source and Gate-Drain diode are modelled by the classical diode equation:

$$Igs = Is \cdot [exp(\frac{V_{gs}}{N \cdot Ut}) - 1]$$

and

$$Igd = Is \cdot [exp(\frac{V_{gd}}{N \cdot Ut}) - 1]$$

where N is the emission coefficient or ideality factor of the diode, and Is is the saturation current. The gate junction capacitance is described by

$$C_{gs} = C_{gso} \cdot (1 - \frac{V_{gs}}{Vbi})^{-M}$$

if $V_{gs} \leq FC \cdot Vbi$

$$C_{gs} = C_{gso} \cdot (1 - FC)^{-(1+M)}(1 - FC \cdot (1 + M) + M \cdot \frac{V_{gs}}{Vbi})$$

if $V_{gs} > FC \cdot Vbi$ The equations for C_{gd} is the same as above except V_{gd} takes place of V_{gs}.

where M is the grading coefficient

V_{bi} is the gate potential, it is also called Pb in the HSPICE terminology. The value 0.324V doesn't seem reasonable here. However, it is the value that fits best in PML's model.

Cgso is the zero bias capacitance

FC is the forward bias capacitance coefficient.

A limitation of the Curtice model lies in its inability to be fitted in the simulations of small V_{gs}. In the given parameters, V_{to} is assigned 0.217V, when its V_t is 0.175V. As a matter of fact, the predicted I-V curves fits less to the measured values when the V_{gs} is under 0.4V. The simulations for this design are done by using HSPICE h9007 version.

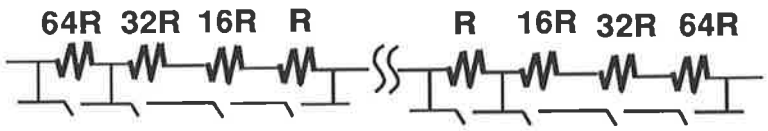


Figure 3.14: A switch controlled resistor string

3.3.2 The generation of 256 reference voltages

Due to the superior of mismatch, a resistor ladder appears to be the best choice to generate the reference voltages. Figure 3.14 is a kind of resistor ladder used in some cases.

First it uses 16 resistors with the same value of R to provide 16 coarse reference voltages when all switches are open and a fixed voltage is applied across the chain during the coarse comparison period. The result of the coarse comparison will then be processed to generate a control word which sets a combination of the switches on while others are turned off. The total resistance of the chain will be set to 256R. So, when current flow through the resistor chain, 16 fine quantization states will be established by the 16 R value resistors. Mean while the combination of 16R 32R 63R ...etc. will generate a voltage level for the 16 states based on the input level.

In this scheme, only a limited number of resistors are used that occupies a small chip area. However, different value of resistors are included in the ladder and that will increase the mismatch when the circuit is fabricated. Also, the involvement of

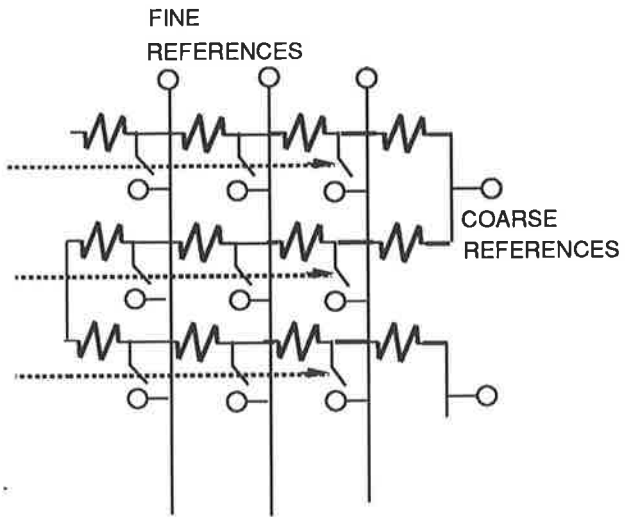


Figure 3.15: The design of a resistor ladder

switch resistance in the current path is a major drawback of this approach. Because the channel resistance varies very much from switch to switch. This increases the nonlinearity of the ADC. Moreover, the high switch resistance will add to the RC constant and low down the responding speed.

To prevent the problems, a resistor ladder formed by 256 identical segments is a better choice. Figure 3.15 shows the idea of a resistor ladder commonly used in ADC circuits and adapted for this design. It is divided into 16 folds each consists of 16 segments. The coarse reference voltages are picked up from the end of each fold, when the fine reference voltages are detected from each tap in the chosen fold decided by the result of the coarse comparison.

A switch is attached to each resistor segment. Total 256 switches are grouped in the same way as the resistor ladder. Thus, a control signal will be sent base on the result of the coarse comparison from the logic to select 16 segments in a resistor fold. Then, 16 selected fine reference voltages will be put on the bus and used by the 16 comparators.

In order to minise the total resistance of the ladder, and facilitate the high speed application a metal line is used as the resistor ladder. Only the voltage levels in the ladder are sensed by the comparator, no current will flow in or out of the ladder. So, the disturbance to the reference voltages is minimised.

3.3.3 The design of an analog switch

In logic circuits, a single transistor can be used to carry out the functions of a switch, because the absolute value of the voltages applied to control and to pass through the switch are not a major concern. It only cares about whether the voltage is above a threshold level and represents an '1' or below the threshold and represent an '0'. Usually, only a few selected voltage levels will appear at switch terminals during the operation.

Contrasting with logic switches analog switches must be capable to pass variable voltages appearing at the input nodes to the output within required distortions all the time in operation. Therefore, the voltages applied to the control gates must be adjusted to trace the changing input levels and maintain $V_{gs} > V_t$ to keep the switches on.

An ideal analog switch posses following characteristics[BSC];

- zero impedance gives zero voltage drop when it is on
- infinite impedance gives zero leakage when it is off
- no gate offset voltage at zero current
- no offset current at zero gate voltage
- no load to the controlling source

In addition to above listed requirements, a very important character of GaAs switches is the existence of a Schottky diode across the metal gate and the conductive channel of the transistor. The diode can be easily forward biased and incur gate leakage that distorts the signals passed through the switches and it must be prevented.

A usual design of analog switch is demonstrated in figure 3.16 [LARS]. In this switch, a subcircuit is used to provide a voltage shift tracking the input voltage and to charge up node A to turn the switch on when the clock is at low level. When the

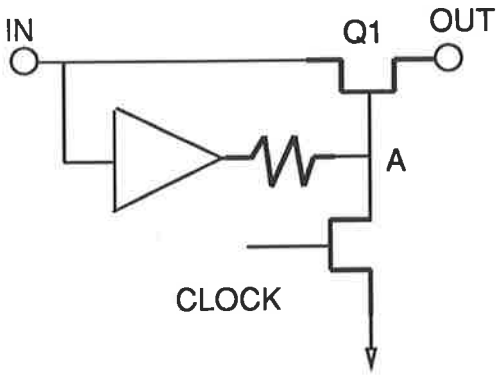


Figure 3.16: A commonly used switch

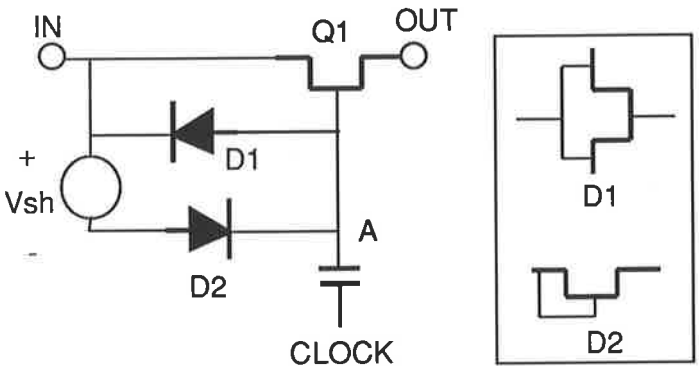


Figure 3.17: A better switch structure

clock goes high, node A will be pull down to zero volt and turn the switch off. A large number of transistor and rather high current are used in the subcircuit.

A better switch structure is designed and shown in figure 3.17. This switch uses a diode D2 to charge up node A to a level which is lower than the input voltage by V_{sh}. Then, the voltage at node A will be raised through the coupling capacitor to turn on the switch when the clock goes high.

In order to maintain high charging speed when the voltage across D2 is low and keep node A always following input, a diode connected transistor, in which the gate is connected to the drain, is selected here. This diode is also used to keep the charges at node A from being lost when the voltage goes up.

The voltage shift can be provided by a source follower when this switch is used to pass analog input signals, while a second resistor chain is used in the case of transferring reference voltages.

The input voltage is changing from time to time when it is connected to analog input source, and if $V_{in}(\mathrm{t1}) = V_{max}$ and $V_{in}(\mathrm{t2}) = V_{min}$ overshoot will happen at the rising edge of the clock. So diode D1 is used to release the charges from node A to input end and reduce the overshoot at output end. D1 must be connected as indicated in figure 3.17. So not to lose charges when it is not necessary. However, D1 can be eliminated if V_{in} is a fixed voltage when the switch is on. This is applicable when the input is connected to a fixed voltage reference.

The voltage travel at node A is decided by the clock swing multiplied by the ratio of $C_{couple}/(C_{couple} + C_{sw} + C_{diodes})$. If the voltage travel and the V_sh are carefully chosen, the overshoot can be prevent and low channel resistance can also be obtained

when it is used in the path of reference voltages.

However, the voltage travel at node A must be greater than 1V to prevent unexpected switching. Because in the design the outputs of the two switches are connected together before they are fed into a comparator, and the output voltage can be pull down 1V by another switch after the first one is turned off. In case, node A travels less than 1V, the gate to output voltage may become larger than the threshold voltage and turn the switch on again.

3.4 The realisation of the comparator

The structure of the reference sampling comparator is explained in the previous chapter. The figure is quoted here again. To realise the comparator we need a differential amplifier, and a switch for self calibration and an input capacitor for each branch of the differential amplifier.

The simplest structure which includes above mentioned components is shown in figure 3.19.a. In this circuit, a pair of inverter and a single transistor current source are used to form a differential amplifier. S1 and S2 are for self calibration when S3 to S6 are used for input selection.

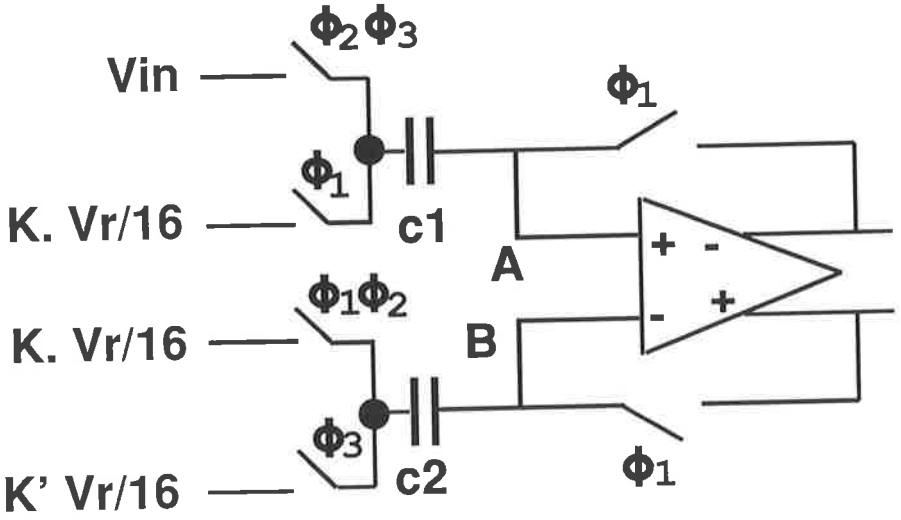


Figure 3.18: The reference sampling structure

This circuit is very simple and consists of a small amount of devices. It provides very good offset cancellation and high speed, even though the Miller effect exists. However, due to the Schottky diode across the input node A and the output node B, the V_{gd} can not exceed 700 mV. But, assuming the gain of this differential amplifier is A_v, when input goes up V_{in}, the output will travel down by A_v times V_{in} and make $V_{gd} = (1 + A_v)V_{in}$.

So, the input range will be restricted to within $700\text{mV}/(1 + A_v)$, otherwise the diode will be turned on and short input to output. Then the function of the differential amplifier will be lost completely. Therefore, this scheme can not be accepted for 1V input dynamic range.

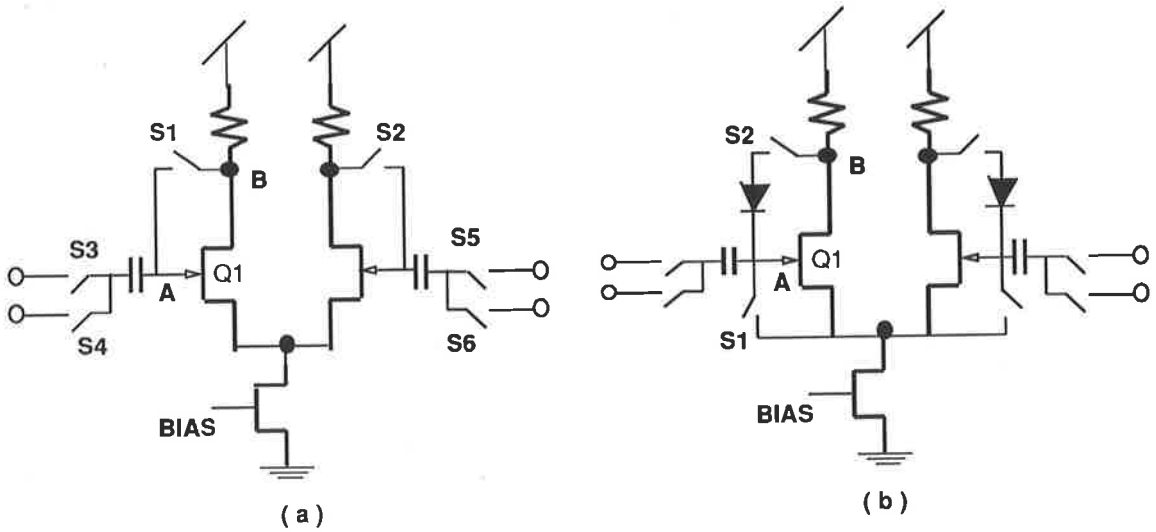


Figure 3.19: The design of a basic comparator

To release this problem, a voltage shift from output node to input gate must be applied to create more room for V_{gd} to swing. The simplest and common way to provide a voltage shift is to use a diode. Figure 3.19.b shows the modified circuit in which, a diode and another switch are added to each branch of the amplifier. When both S1 and S2 are on during phase 1, the current will flow through the diodes and the switches, this will generate a level shift from the output to the input node.

Mean while, if the ratio of the size of S1 and S2 are carefully chosen, the voltage across S1 will be small enough to switch the transistor off. This is an attempt of hysteresis reduction, and will be discussed in the section of "Hysteresis Reduction".

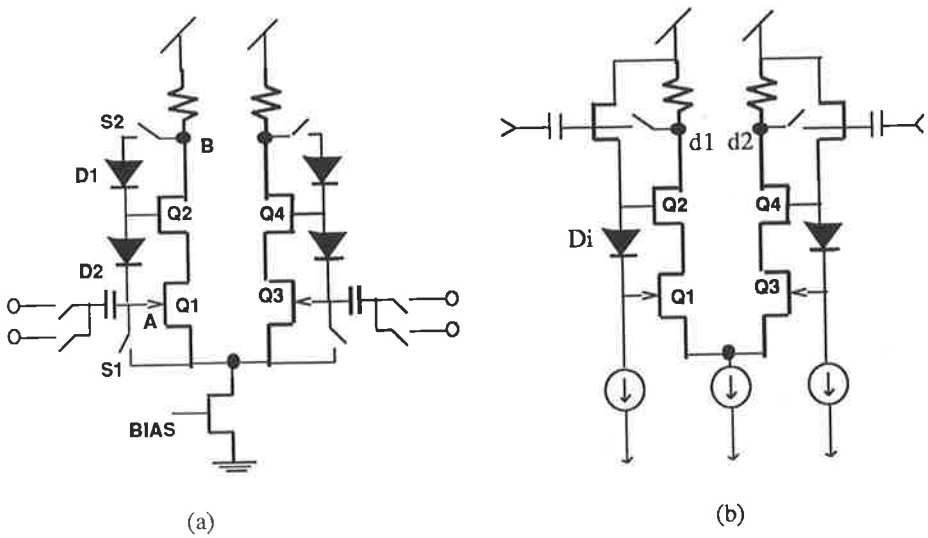


Figure 3.20: Comparators with bootstrapping structure

After the voltage shift was formed in about 100 ps, S1 of both branch will be opened and allow the transistors to work for self calibration. Even though, the voltages at node A and node B will be slowly raised by the cut off current of the diodes in the approximately 150 ps of self calibration period, the offset cancellation will be performed and the level shift will be maintained.

This circuit is still very simple and consume very small power, when it works very fast and performs very high percentage of offset cancellation. However, due to the lack of confidence in the hysteresis relief, this scheme is modified again and a "bootstrapping structure" is adapted.

In figure 3.20.a, two diodes are included in each branch, D1 is to provide room for

V_{gd} of Q2, and D2 is to provide a level shift from Q1 to Q2 to perform hysteresis reduction which will be explained in the next section. The input signals are supposed to appear at both gate of Q1 and Q2. But, the positive going input voltage at Q2 is coupled through the stray capacitance of D2, and the ratio of $C_{d2}/(C_{d2} + C_{q2})$ makes a severe decay of input signal at Q2. Where C_{d2} and C_{q2} are the stray capacitance of D2 and Q2 respectively. Therefore, this circuit is not suitable for further investigation.

A source follower appears to be a good solution to above problem. The circuit shown in figure 3.20.b is the final candidate for this design. The transistor Q_f of the source follower provides a level shift from the output node d1 to the gate of Q2, and a diode di generate a voltage shift between Q1 and Q2. S1 in the previous scheme is cancelled because a "bootstrapping" is used for hysteresis reduction and a current source is attached to provide constant voltage shift.

This structure posses high potential to meet the design targets. Its performance will be discussed in detail in the latter sections.

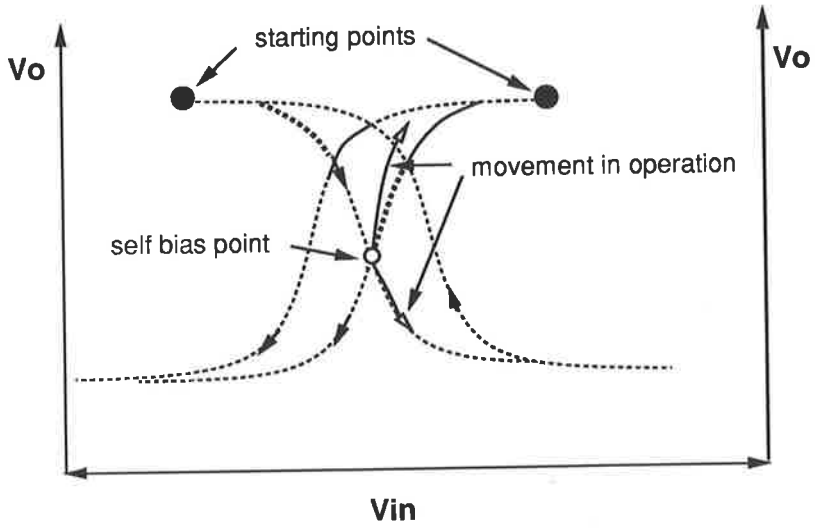


Figure 3.21: Differential amplifier transfer curve with hysteresis

3.4.1 A bootstrapping structure for hysteresis reduction

As it was discussed in section 3-1, the hysteresis is mainly caused by the releasing process of the trapped charge carriers at the interface of the channel and the substrate. It causes uncertain drain current when the V_{gs} is selected or uncertain V_{gs} when the drain current is imposed. An attempt to reduce hysteresis is to push the V_{ds} and the V_{gs} to zero volt at the beginning of each operation cycle before self calibration. In doing this we assume the trapped charges can be totally redistributed when the transistor is pushed off. In this case only the charge trapping during self calibration period will cause hysteresis and affect the accuracy of the comparison afterward. And this hysteresis effect will be detected as a part of the offset voltage. The hysteresis only changes the trace of the output voltage as shown in figure 3.19.b and the comparison can still be performed correctly.

This idea is illustrated in figure 3.19.b by using the S1. However, this idea is suspended because the time needed for the trapped charges to be released can be as long as milliseconds during operation and the measurement of that for a switched off transistor is not clear. Therefore, the usual way of dealing with hysteresis, that is to restrict the V_{ds} travel is adapted. Since the hysteresis is a function of V_{ds} and V_{gs}, it is generally believed that the hysteresis will be minimised when V_{ds} is fixed.

To fixed V_{ds} swing three methods can be used, the Common Mode Feedback (CMF) presented in [KATSU], cascoding structure and bootstrapping structure[LARS1]. Cascoding is also commonly used to minimise Miller effect. However, it does not appear to be the best choice for minimising V_{ds} travel compared to bootstrapping. The following three schemes are compared to facilitate a better choice for hysteresis reduction. In figure 3.22.a is the structure of conventional cascoding. Assuming all the transistors used are identical and the V_{IN} raises $2\Delta V$ at the time observed, and the effects of V_{ds} on drain currents are negligible. Then, due to the total current of the differential amplifier is determined by a current source and is constant, the current increased at one branch equals the current reduced in the other branch.

The initial current in each branch is equal and is decided by

$$W \cdot \beta(V_{IN} - V(5))^2 = W \cdot \beta(V_{RE} - V(5))^2$$

and initially

$$V_{IN} - V(5) = V_{RE} - V(5)$$

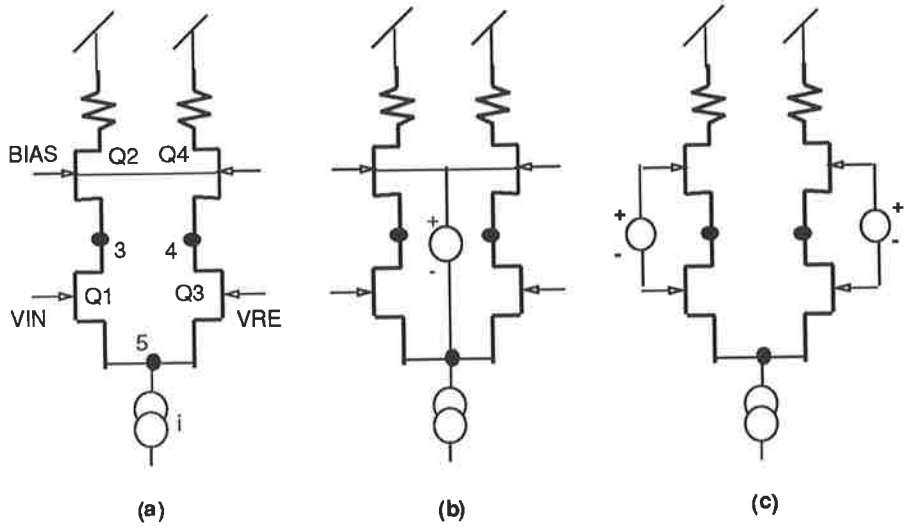


Figure 3.22: Three type of hysteresis reduction schemes using Depletion MESFETs

$$V_{IN} = V_{RE} = V_i$$

then voltage change Y at node 5 will be induced by the input change. So the equal current change in each branch yields

$$V_i + 2\Delta V - (V(5) + Y)^2 - V_i - V(5)^2 = V_i - V(5)^2 - V_i - (V(5) + Y)^2$$

where Y is smaller than ΔV. Solving this equation, we have

$$2(V_i - V(5))(2\Delta V - Y) + (2\Delta V - Y)^2 = 2(V_i - V(5)) \cdot Y - Y^2$$

when ΔV is small, Y^2 and ΔV^2 are negligible and $Y = \Delta V$ is obtaincd.

So, the common mode level V(5) will be raised by ΔV and the final V_{gs} change at V_{IN} side is ΔV. Since the current in Q2 is the same as it is in Q1, the V_{gs} of Q2 must equal to that of Q1. When, $V_{IN} - V(5) = \Delta V$ and the "BIAS" is fixed, the voltage at node 3 V(3) must go down ΔV, so that the V_{gs} of Q1 and Q2 remain the same. Therefore, a total $2\Delta V$ swing can be found at the V_{ds} of Q1 and zero volt swing at the V_{ds} of Q3.

The same analyses can be applied to the structures in figure 3.22.b where the "BIAS" is not a independent voltage level but a fixed voltage shift from common mode level V(5). The result found is that the V_{ds} travel at Q1 is ΔV and the travel at Q3 is $-\Delta V$.

In the structure shown in figure 3.22.c, the "BIAS" voltages follow V_{IN} and V_{RE}, this structure is called "bootstrapping" rather than cascoding, the V_{ds} variation detected at both Q1 and Q3 are zero volt. The graph illustrated in figure 3.23 shows the simulation results of above three structures when a 50 mV input voltage is applied. The bootstrapping structure incurs a fluctuation of only a few millivolts when others have about 25 mV or 50 mV drifts. Although, increasing the size of Q2 in the first and the second case to much larger than Q1, the V_{ds} travel of Q1 can be reduced, the bootstrapping structure appears to be the best choice for restricting V_{ds} swing when small chip size is preferred.

Though, the V_{ds} of Q1 is nearly fixed, the V_{ds} of Q2 is still traveling a wide range according to the gain and the V_{in}. Fortunately, this does not cause hysteresis concern. Because the drain to source current of Q2 is decided by the V_{gs} and V_{ds} of Q1, and the V_{ds} of Q2 is determined by the current and the resistive load of the circuit. The V_{gs} of Q2 will be adjusted automatically to meet the already defined current and V_{ds}. Therefore, the existence of hysteresis in Q2 will not affect the accuracy of the circuit.

However, Miller effect is still a concern of the third approach since both the gate of Q1 and Q2 are driven by the input source and performs as an input node. Although the fixed V_{ds} of Q1 also avoids the Miller effect at Q1, the capacitor across the gate and drain of Q2 incurs Miller effect in this scheme, while it is reduced dramatically in other two cases. Thus, other skills such as using small gain are required to deal with speed.

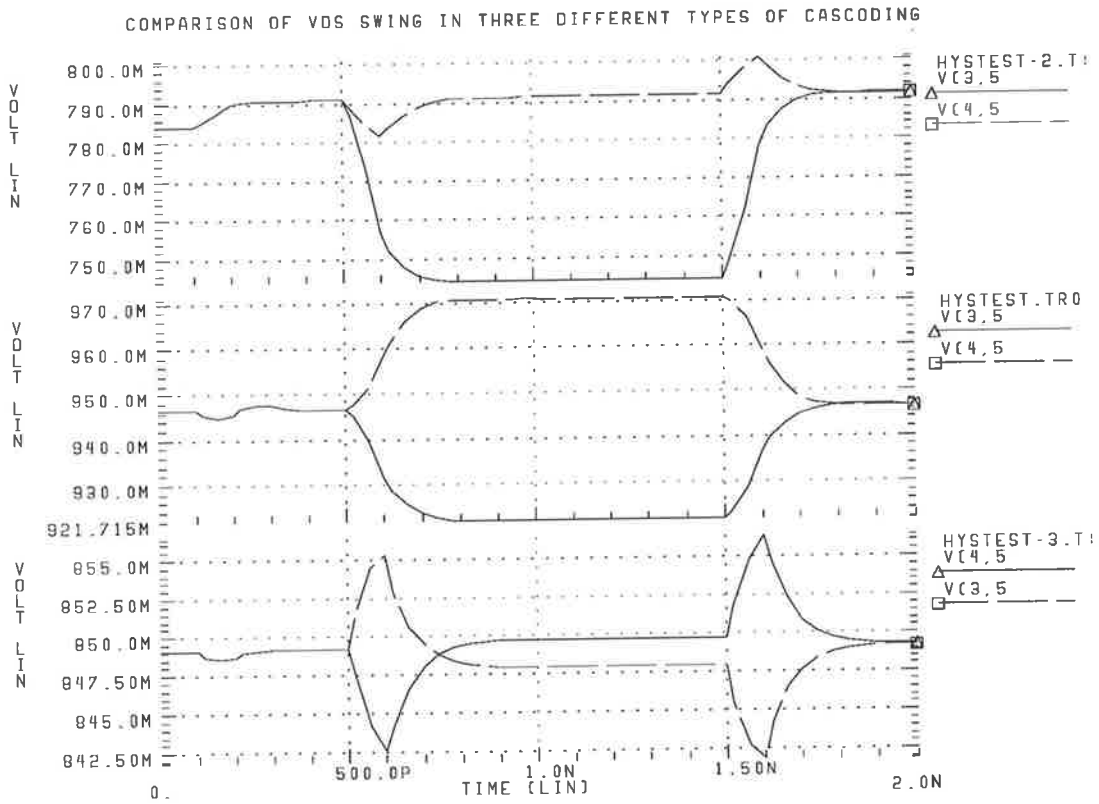


Figure 3.23: The simulation results of three hysteresis reduction schemes

Chapter 4

ADC performance optimisation

In the previous section the complete circuit of a comparator is designed. It exhibits the potential of fulfilling the required specifications. Nonetheless, the sizes of devices, the currents and the voltages applied to the circuit are very important factors to obtain the required performance. Care must be taken to size the circuit so that it can operate as what is expected. This chapter will discuss the effects of the electrical parameters on the offset cancellation, voltage gain and the response speed of the circuit. Simulation results will be presented to support the findings.

4.1 The effect of offset cancellation on performance

In the discussion in section 3-2, a switch connecting the output node and the input gate of the source follower is included to perform offset cancellation. To avoid disturbance of the self bias point at the high impedance input gate when the switch is turning off, we need to compensate the clock feedthrough.

Clock feedthrough is caused by the movement of charges around the depletion region coupling through the gate-drain or the gate-source capacitor of the switch. In the first case, the charges in a conducting channel of a transistor will be released to the source and drain when the channel is turned off. The charges will then cause voltage drifts at the receiving nodes. If the node is a high impedance terminal, the drifted voltage will remain for a long time, whereas it will be redistributed and cause a small glitch for a low impedance terminal.

The contribution of the parasitic capacitors to the feedthrough is illustrated in figure 4.1 and can be expressed by [?]

$$\Delta V_c = (\frac{C_{gd}}{C_{gd} + C_o}) Min[(V_{in} + V_t), (V_c + V_t)]$$

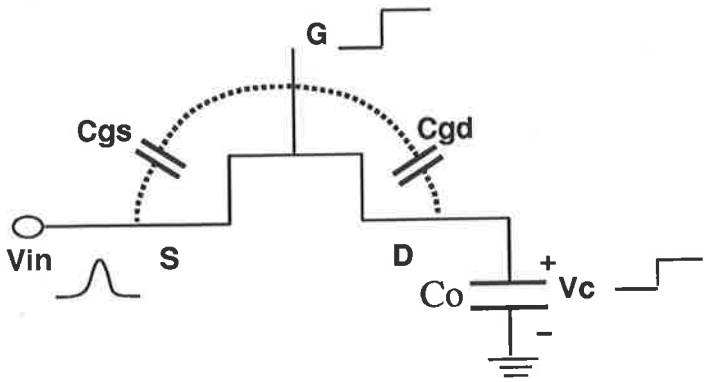


Figure 4.1: Clock feedthrough

where V_t is the threshold voltage. Clock feedthrough only couples part of a transition from 0V to $V_{in} + V_t$ when the transistor is off and the drain is connected to a high impedance output capacitor. After the gate-source or the gate-drain voltage is high enough to turn the transistor on, the drain is connected to low impedance source, and the clock doesn't couple to the drain. Figure 4.2 illustrates a modified switch aimed to reduce the clock feedthrough. Since the feedthrough depends on the voltage travel between the threshold of the switch and the low level of the clock, it is important to equalise the gate voltage swing at both transistor. This is similar to MOS technology where only half of the charges need to be compensated at the output end. So the sizes of the devices in the right half of the switch which compensate the feedthrough are half the size of the original switch itself.

The performance of this modified switch depends heavily on the behaviour of the channel clock feedthrough which is related to the modification of the depletion region under the gate. Unfortunately, this property is not characterised in our model.

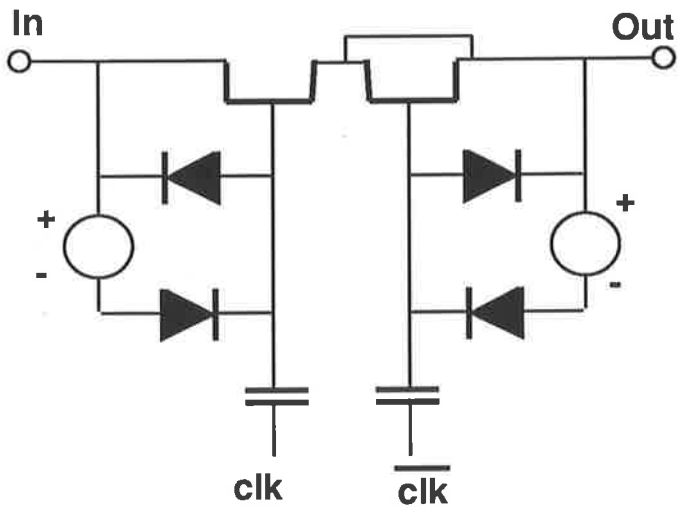


Figure 4.2: A modified switch for self calibration

The expected voltages at both end of the switch should be the same at the end of each self calibration cycle. So the switching function can be carried out by a single transistor if the voltage applied to the gate is carefully chosen. Also the concern of perturbating the self bias point can be greatly reduced by using a small ratio of the size of the switching transistor over the input gate. With the use of a single transistor, the capacitive load seen by the output node is much smaller than that of using the analog switch which helps determine the operating speed (figure 4.3).

There are two reasons for the choice of a high gate-source voltage to the switch. One is that the resistance of the switch, which is an important factor of switching speed, depends on the applied voltage. The second is that insufficient gate voltage

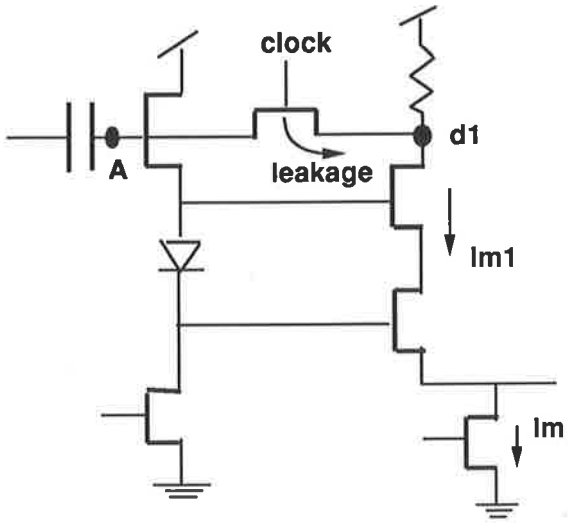


Figure 4.3: A single transistor feedback switch

will turn the switch off before the input node A is charged up to the level of the driving output node, d1. This causes poor offset cancellation performance. Figure 4.4 shows the input and output curves of a comparison cycle (bottom one) and the magnified original self calibration (top one). It demonstrates that the differential output voltage (dashed line) approaches the differential input voltage when the applied gate voltage increases.

However, a very high gate voltage will incur gate leakage which will replace part of the normal current in the differential amplifier. This will cause an incorrect result at the output node and it will be transferred to the input gate during the self calibration cycle and cause errors after the self calibration cycle.

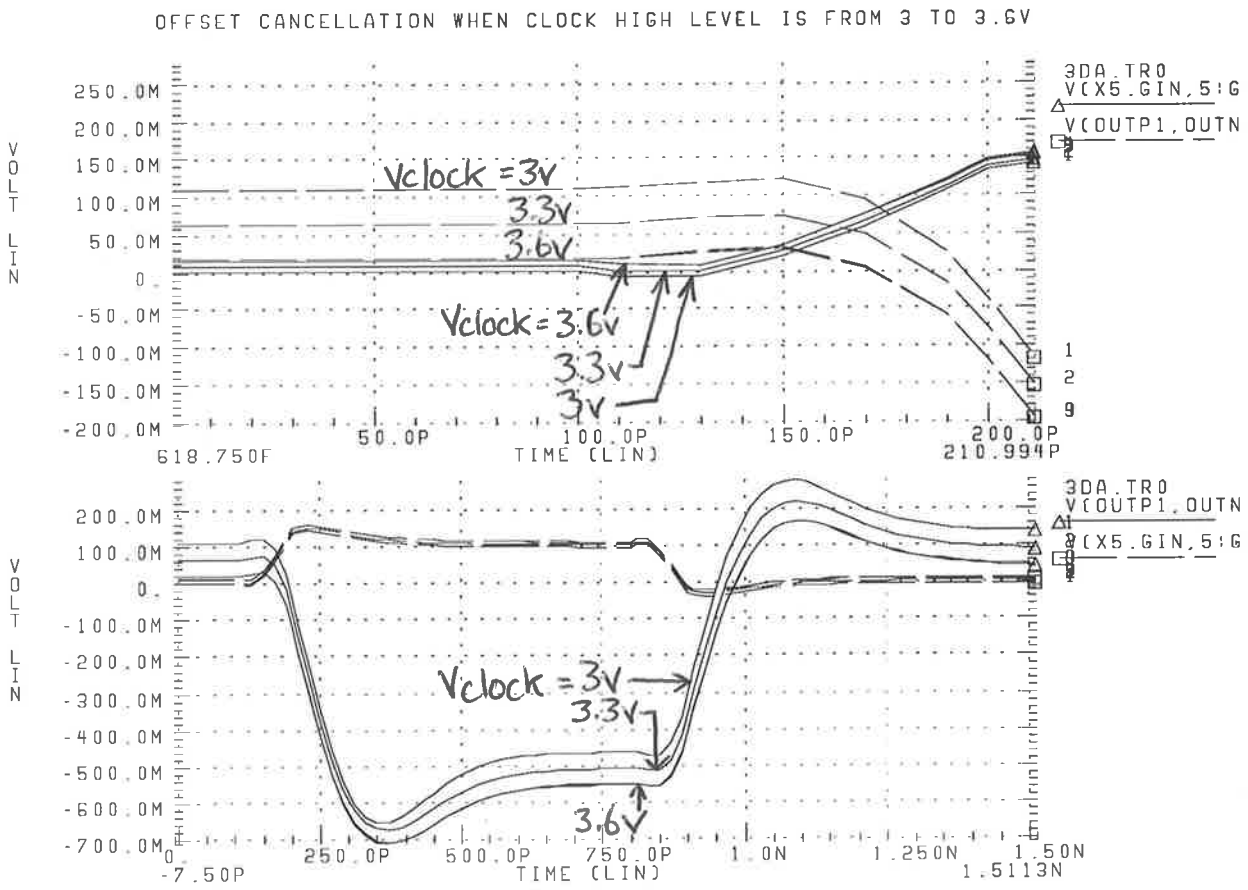


Figure 4.4: The simulation of offset cancellation

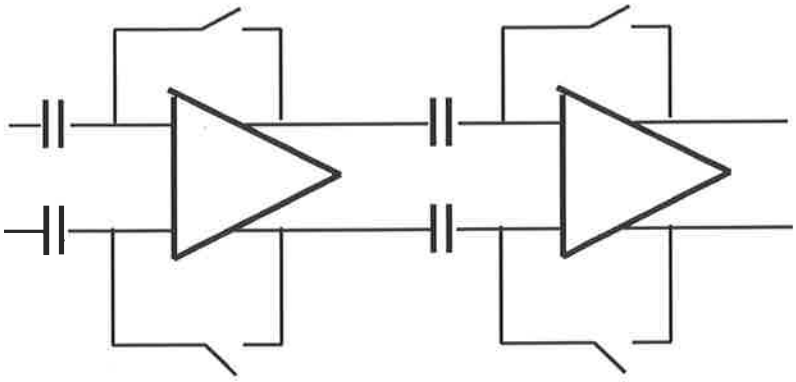


Figure 4.5: The cascaded structure of switching capacitor comparator

Therefore, the level of d1 at the quiescent state after self calibration is limited to 0.3-0.4V. The low level of the clock applied to the switch is determined by the need to keep the switch off when the output node d1 travels to the bottom of its dynamic range. A very low voltage should be avoided to prevent large clock feedthrough. This voltage level can match the one applied to all analog switches if the output swing equals the input dynamic range.

There is another feature in this design that can reduce the effect of offset voltage, - the cascaded structure of the switching capacitor comparator. Since this design may use more than one comparator stage and the output of each stage is isolated by the input capacitor of the following stage, only the dynamic change can be passed and amplified in the following stages.

Therefore, the ADC operates as an offset free circuit when the following two con-

ditions are true. First, the final differential input voltage caused by the offset is well within the linear gain region of the comparator, so that it will not degrade the gain. Second, the differential output voltage of the last stage is much smaller than the output voltage swing, so that the differential output can represent the logical results of the comparisons correctly.

4.2 The comparator gain and operating range

In the previous study the requirement of a comparator gain greater than 100 has been discussed. The larger gain improves the resolution of the comparator, but very often the factors which lead to a high gain are also the draw back of other figures of merit such as power dissipation, speed and chip size. When a large gain is considered the associated cost to other factors should not be ignored.

Due to the small transconductance of GaAs circuits compared to Silicon technology, very high gain is unachievable, therefore a cascade structure of amplifiers is necessary. The lack of a depletion transistor (DFET) as the load forces us to choose either resistors or enhancement transistors for loads. If an enhancement type transistor is used as a load, the gain of the comparator will heavily depend on the ratio of the load transistor over the current supply transistor. Resistor loads may be selected if

small chip area and low parasitic capacitance are required.

4.2.1 The equivalent circuit and the analysis for gain

From the mathematical derivation in Appendix B and Appendix C, the midband gain, in which the effects of the stray capacitances are negligible, can be expressed by

$$A_v = \frac{C_{in}}{C_{in} + C_f} \cdot \frac{G_{mf}}{G_{mf} + G_{df}} \cdot \frac{-G_m}{G_l}$$

where

C_{in} is the input capacitance

C_f is the gate-drain capacitance of Q_f

G_{mf} is the transconductance of Q_f

G_{df} is the output conductance of Q_f

G_m is the transconductance of Q1 (Q1, Q2, Q3 and Q4 are identical)

G_l is the $1/R_l$

set

$$Av_{cin} = \frac{C_{in}}{C_{in} + C_f}$$

$$Av_{in} = \frac{G_{mf}}{G_{mf} + G_{df}}$$

$$Av_{out} = -\frac{G_m}{G_l}$$

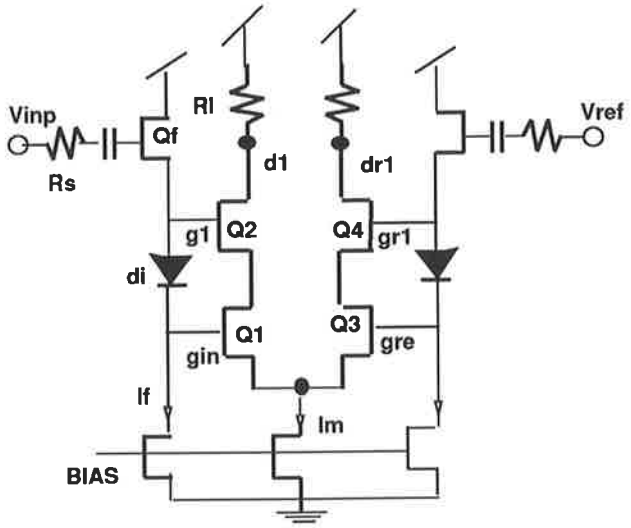


Figure 4.6: The circuit for the measurement of gain

It is obvious that the gain of the comparator consists of three main components: the ratio of the input capacitor over the input gate capacitance (Av_{cin}), the gain of the source follower, it will be called input gain (Av_{in}) hereafter, and the gain of the differential amplifier or the output gain (Av_{out}). Because the circuit will be required to operate in large signal applications, the sensitivity of the Schottky gate diode must be always kept in mind through out the design work. The cross influences between the source follower and the amplifier makes it necessary to consider the effects of each parameter on the overall performance.

4.2.2 The factors affecting voltage gain

Av_{cin} is determined only by the ratio of the capacitances, it behaves as a voltage divider at a very wide frequency range. When C_{in} increases or the size of Q_f decreases, Av_{cin} increases and then saturates and approaches to one from below. In order not to consume too much area, we keep C_{in} in 1 pF range.

In order to explore to effects of the parameters on the gains, the input gain Av_{in} is measured as $(V_{gin} - V_{gre})/(V_{inp} - V_{ref})$ and Av_{out} as $(V_{d1} - V_{d2})/(V_{gin} - V_{gre})$. The characteristic of V_{d1} and V_{dr1} versus $V_{inp} - V_{ref}$ are also simulated to understand the overall effects.

Some conditions must be preset based on the requirements for commonly used devices and the possible operating range of the final design. First, a 4-5V power supply is chosen to match the most popular V_{dd} range used in logic circuitry. Then the resistive load is 1 kΩ, transistor sizes are W_f = 80 μm, W_m= 40 μm, W_{di} = 10 μm, currents are set to I_f = 1 mA, I_m = 2 mA and the initial voltage at the gates of the source followers are set to $V_{dd} - (I_m \cdot R_l)$. The detailed structure of the simulated circuit appears in Appendix D: Av-meas.

The variations of the gains will be discussed in two parts: the effect of the source follower and the effect of the differential amplifier. Since the G_{df} is usually much

smaller than G_{mf}, the input gain Av_{in} is determined mainly by G_{mf} which is a strong function of the source follower current I_f. Distinct from typical source followers, this structure includes a diode and drives two output capacitors. However, if the diode is driven into a high output conductance point by a high I_f, as it is explained in Appendix B, the equivalent resistance of the diode can be neglected. Then, the two output capacitors can be treated as one, and the circuit can be analyzed as a typical source follower.

1) **The effects of source follower size and the current**

Since the current I_f is imposed by a current source, so when the width of G_f changes the $V_{gs} - V_t$ will be changed according to I_f or vise versa. From $G = \beta \cdot W \cdot (V_{gs} - V_t)$ and $I = 2 \cdot \beta \cdot W \cdot (V_{gs} - V_t)^2$, we know that when W increases by a factor M and I_f is constant, $V_{gs} - V_t$ will decrease by $1/\sqrt{M}$, so G increases by $\sqrt{M}$. This condition can be applied to the source follower, and an Av_{in} change by approximately $\sqrt{M}$ can be expected. The change in W_f will also change Av_{cin}. This reduces the influence of W_f on overall gain.

On the other hand a very small W_f related to the I_f will incur a high V_{gs} which causes gate leakage at Q_f and generates a low resistance ratio of gate impedance over input resistance which degrades the input signals and the Av_{in}. The value of G_{mf}/G_{gs} ,where G_{gs} is the gate conductance of Q_f, appears to be a good indicator of the compromise. According to PML's measurement, the best trade off is at V_{gs}

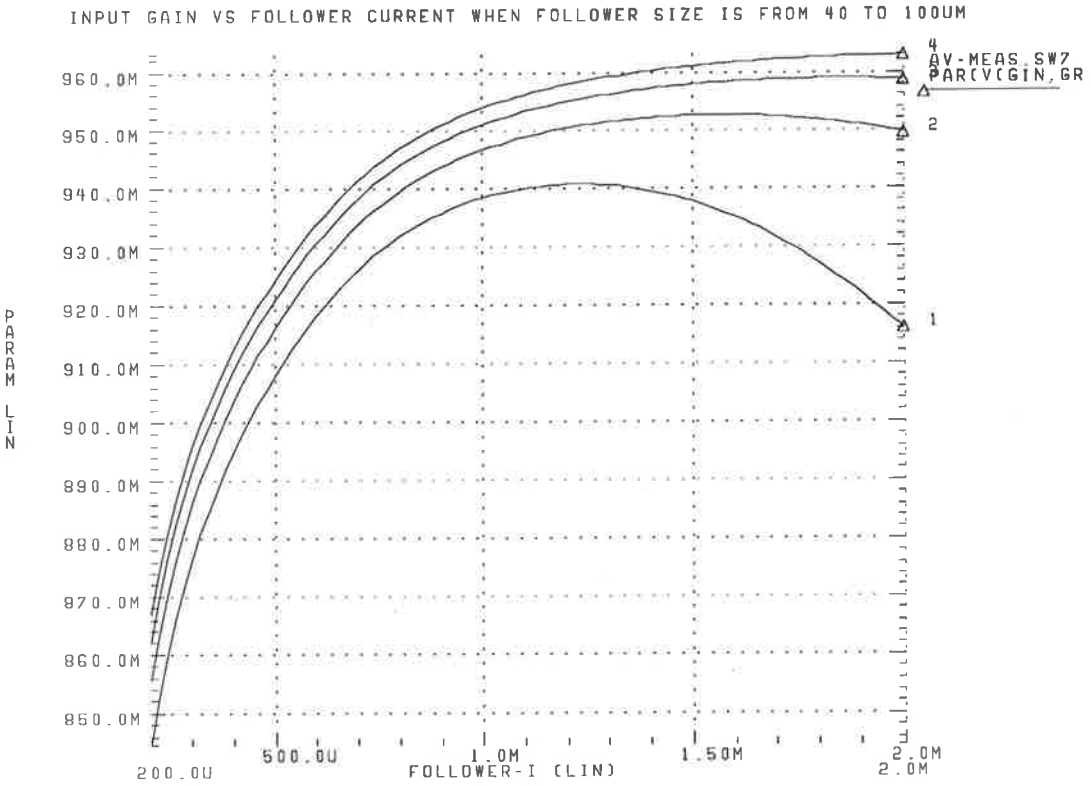


Figure 4.7: The input gain versus source follower current

$= 0.4$V.

As a pre-requisit condition for proper operation of the source follower the current I_f must be large enough, in fact the larger I_f gives more G_{mf} and hence the higher the value of Av_{in} (figure 4.7). It also affects the output gain through its gate-source voltage drop. In the case of insufficient I_f the $V_{gs} - V_t$ will be very small and the voltage at g1 will be very close to d1. Thus, the V_{ds} of Q2 will be pushed into the ohmic region and high output gain is available only at small input voltage (figure 4.8).

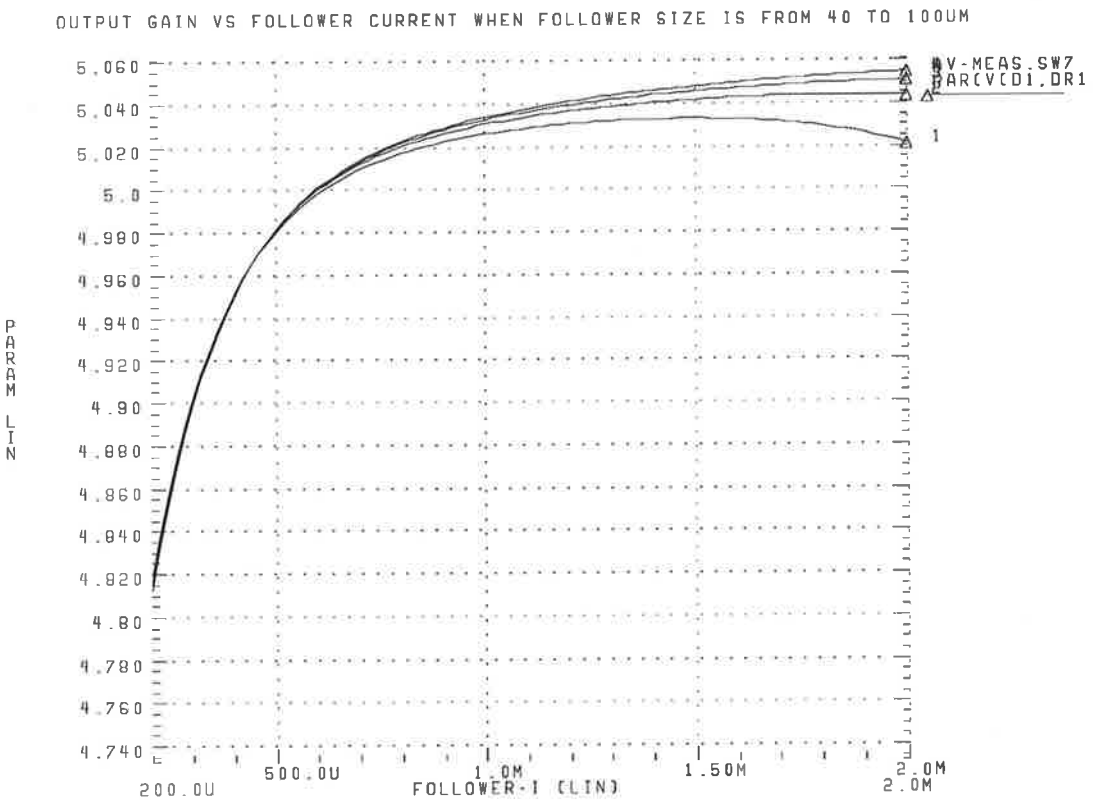


Figure 4.8: The output gain versus source follower current

2) **The effect of amplifier parameters**

The gain of a basic differential amplifier as shown in figure 3.19 is the same as an inverter, $\frac{G_m}{G_l+G_d}$ where G_m is the transconductance, G_d is the output conductance of the transistor in an inverter and G_l is $1/R_l$ of the resistor load. With a fixed V_{ds} of Q1, our bootstrapping structure also offers a gain as an ideal inverter, in which the effect of G_d is cancelled (Appendix B). Thus the gain is determined by G_m and R_l. It is easy to see that larger values of R_l and G_m implies higher output gain can be achieved.

G_m is a function of the amplifier current I_m, the transistor size W and $V_{gs} - V_t$. This is the same as the source follower, only W or $V_{gs} - V_t$ may be determined independently while the other will be adjusted by the selected I_m which is determined by the size and the bias voltage of the current source. When

$$I = \frac{G^2}{4 \cdot \beta W}$$

or

$$G = 2\sqrt{I \cdot W \cdot \beta}$$

and

$$G = 2 \cdot \beta \cdot W \cdot (V_{gs} - V_t)$$

are applied to

$$Av_{out} = -\frac{G_m}{G_l}$$

a better expression of the output gain can be obtained when W is fixed

$$Av_{out} = -\frac{2 \cdot I_m \cdot R_l}{V_{gs} - V_t} \tag{4.1}$$

or

$$Av_{out} = -2 \cdot R_l \sqrt{I_m \cdot W \cdot \beta} \tag{4.2}$$

when $V_{gs} - V_t$ is fixed.

In expressions 4.1 and 4.2 R_l is the dominant factor. It shows a linear relationship with the output gain while other factors have a square root relationship. In figure 4.10 the output gain Av_{out} is proportional to R_l, and increases with the increasing bias voltage when W_m remains constant. But for a fixed V_{dd}, a very large value of $I_m \cdot R_l$ will pull down the common mode level and the operating point through the source follower during self calibration. This will cause an insufficient V_{ds} of the current source and the amplifier current I_m will be reduced and so is output gain. At the same time, the increasing bias causes increasing gate leakage and pull Av_{in} down, while the R_l mostly doesn't affect the input gain. When the $I_m \cdot R_l$ becomes too large and the I_m is reduced, the V_{gs} of Q1 also reduced. Thus, the gate leakage declines and Av_{in} goes up again. However, the circuit does not work any more beyond this point because the current source is nearly turned off and the supplied current is too small.

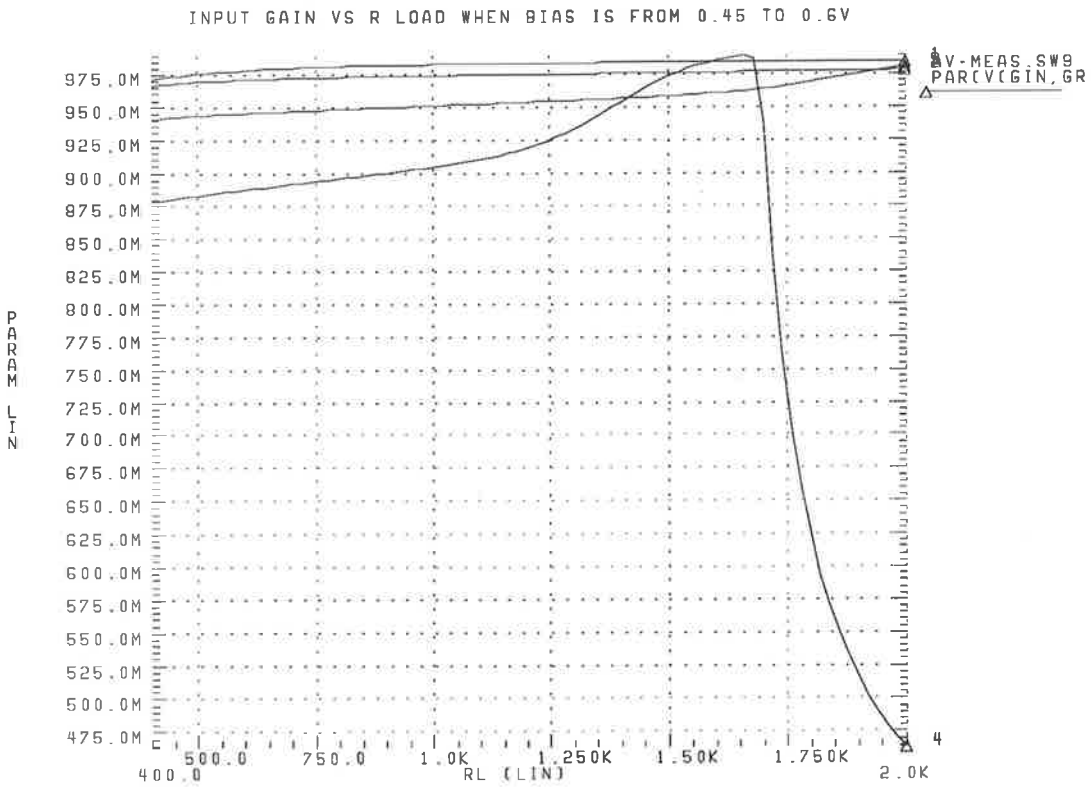


Figure 4.9: The absolute input gain versus resistive load when bias is 0.45 (bottom) - 0.6V (top)

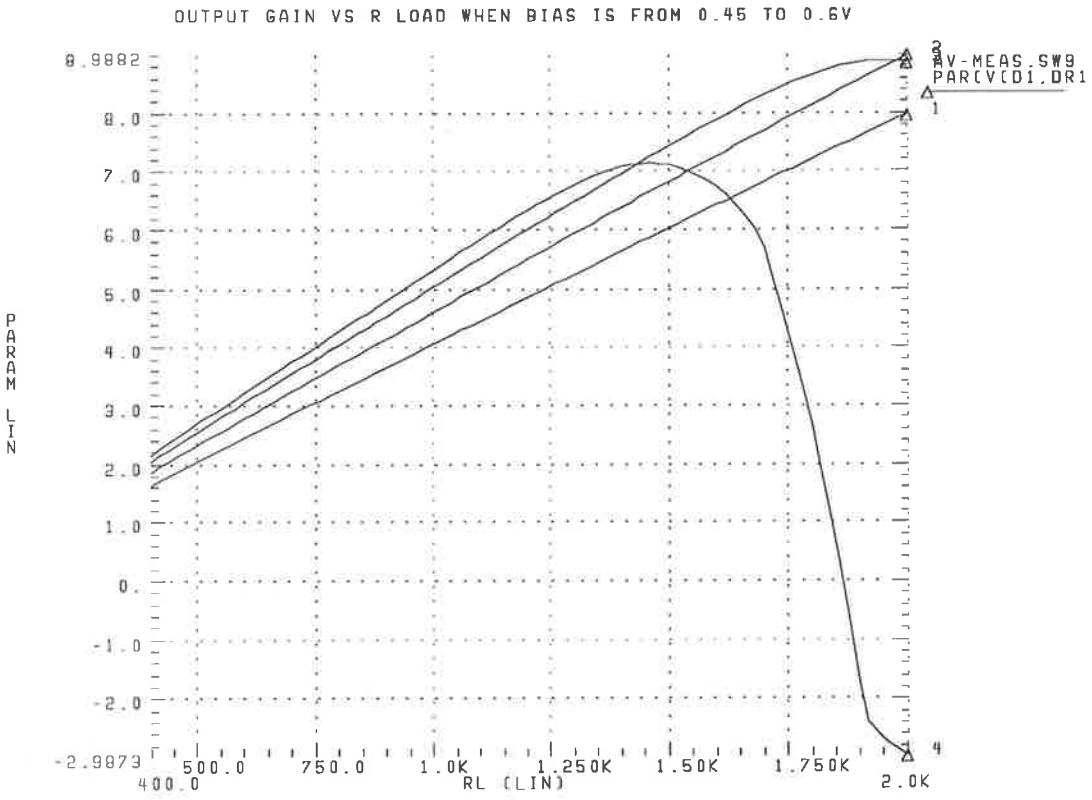


Figure 4.10: The absolute output gain versus resistive load when bias is 0.45 (top) - 0.6V (bottom)

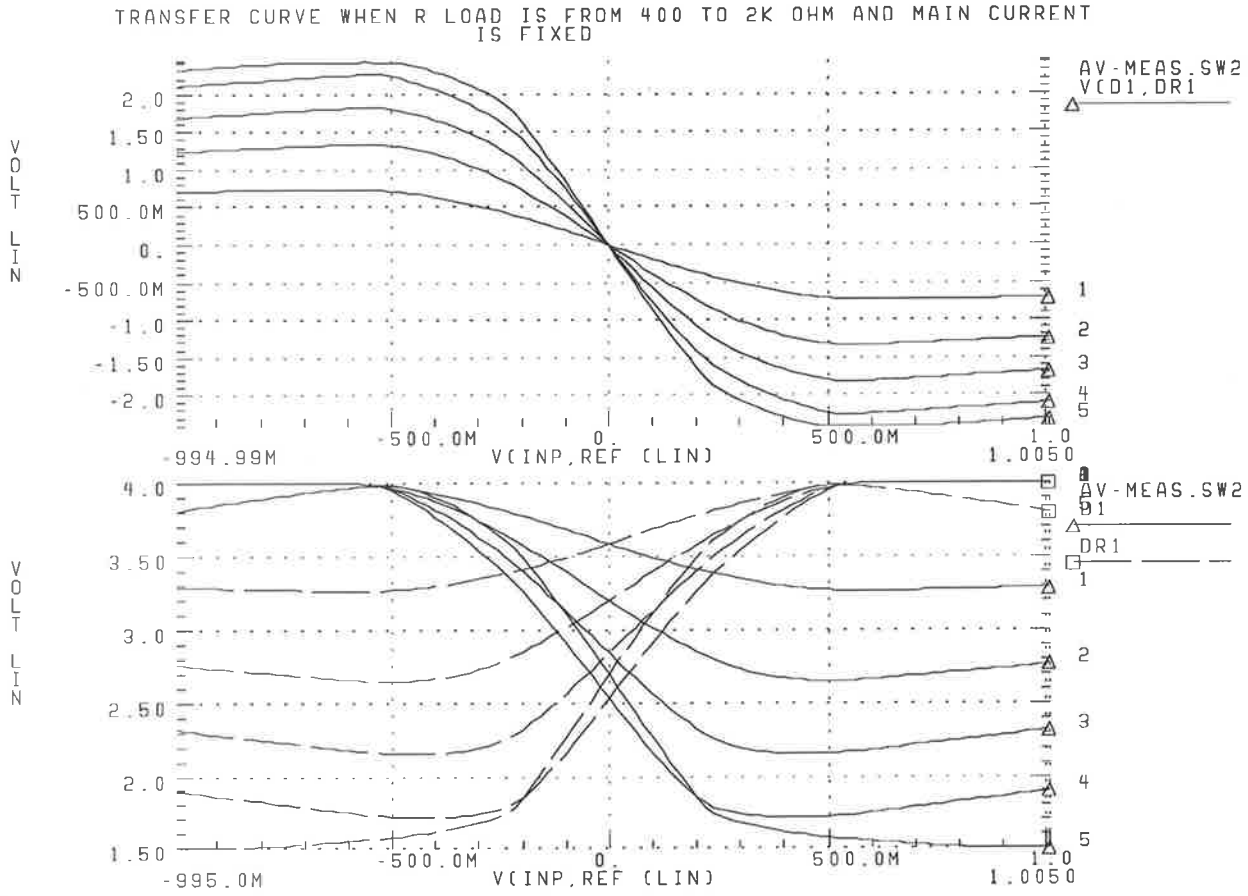


Figure 4.11: The transfer curve when R_l is 400 (marked 1) - 2KΩ(marked 5)

The transfer curve illustrated in figure 4.11 shows the overall effect of the input and the output gain. Many important characteristics of the comparator are demonstrated in this figure. The top graph in figure 4.11 shows the differential output voltages versus differential input voltage, and the bottom one displays the absolute output voltages V_{d1} and V_{dr1}. In the simulation, a fixed voltage is used to supply the power. The common mode level (V(5)) is determined by the $I_m \cdot R_l$ and the voltage drop through the source follower during self calibration cycles.

First, it shows the larger $I_m \cdot R_l$ gives a wider output swing and the steeper slope of the curve which represents the total gain. Second, the maximum value of V_{dr1} can reach the V_{dd} level when the current in the branch of dr1 is totally cut off.

In contrast, the V_{d1} travel is restricted by a combined effect of gate current and the desaturation of Q2. When input increases, the current in the branch of V_{d1} increases and the V_{ds} of Q2 drops, this drives Q2 into the ohmic region. Meanwhile, the input also enhances gate current and V_{d1} starts to go up due to the reduced current. Then the gate current increases exponentially as the current in the branch increases by the square law with the increasing input voltage. Eventually, the fast increased gate leakage will take the place of the normal current and supply the current required by the current source. This will cause a current reduction in the branch and positive gain will occur.

From the above study, a large input voltage does not give a large output. This implies a result of input decreasing will be given when a very large increasing input is applied. This problem is aggravated at the latter stages of the comparator where the input voltages are amplified by the earlier stages. So the output range needs to be controlled. On the other hand, maximum gain is desired for small input voltages, therefore, the value of R_l must be carefully chosen so that the output response is large enough to make the initial output voltage caused by the offset negligible and also prevent severe degradation of output performance.

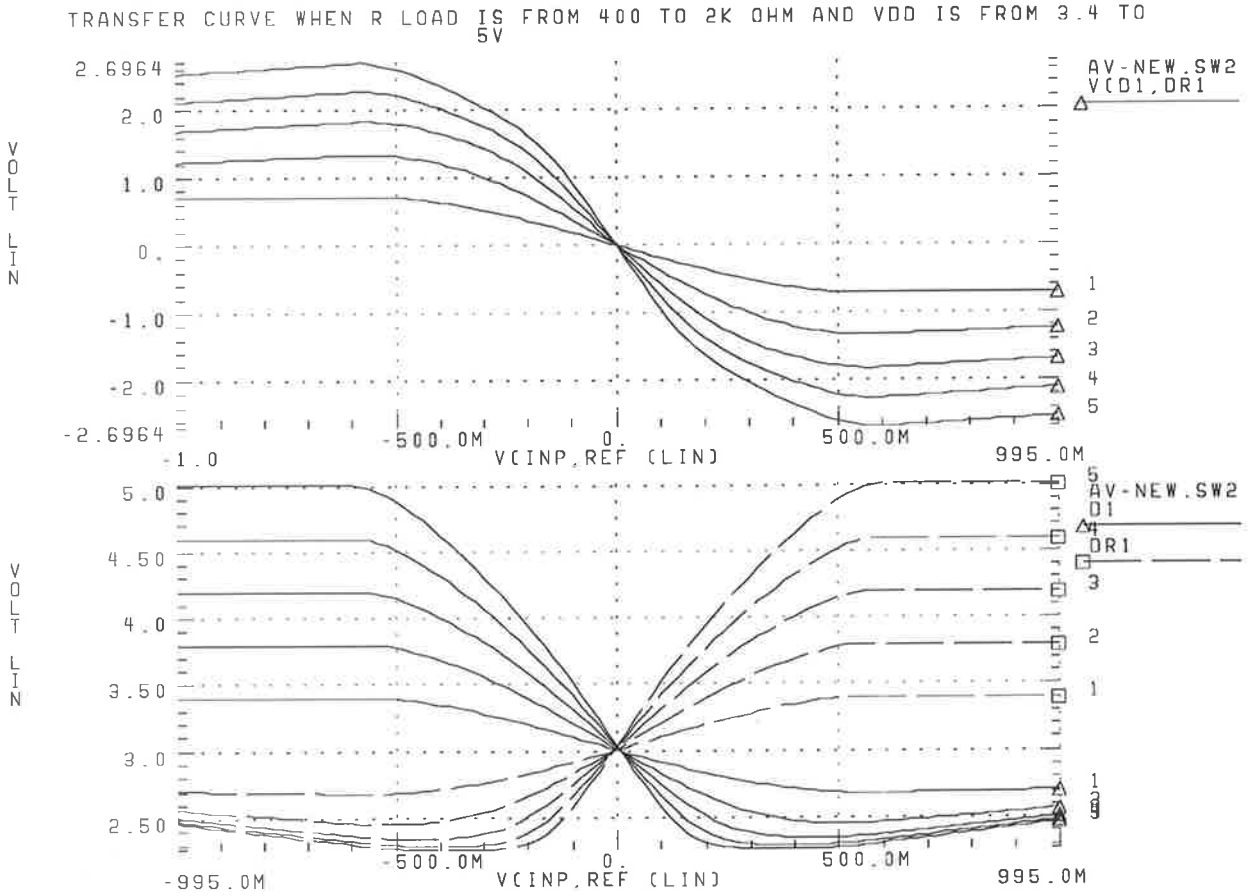


Figure 4.12: The transfer curve when power changes with $I_m \cdot R_l$. Curve 1 is for $R_l = 400\Omega$ and curve 5 is for $R_l = 2K\Omega$

In figure 4.11 the effect of a very large $I_m \cdot R_l$ is presented in the case of $R_l = 2$ kΩ (curve marked 5). However, a larger V_{dd} can alleviate the problem at the cost of higher power consumption. Figure 4.12 shows that the curve bending is reduced when the initial output level is set constant and the power supply voltage follows the $I_m \cdot R_l$.

I_m is another factor which significantly affect gain, but it can not be investigated independently as R_l was done. This is because it will incur a change in size or V_{gs}

of the main transistors Q1 - Q4. So, the effects of the transistor size W_m will be discussed together. Since the design uses the minimum channel length of the transistor which is defined by the process technology, only changing the channel width is discussed.

First, the curve in figure 4.13 demonstrated that the change of Av_{out} in the case of a fixed I_m is proportional to $\sqrt{\alpha}$ when W_m changes by the factor α which agrees with equation 4.2. Meanwhile, an increasing W_m induces a smaller V_{gs} and less gate leakage, so a slowly increasing Av_{in} is obtained (figure 4.14). On the other hand, when W_m is getting smaller, the rapidly increasing V_{gs} and the gate leakage forces Av_{in} to drop very quickly. When we look at the curve of Av_{in} versus V_{gs}, we can see that Av_{in} drops very quickly when V_{gs} is greater than 0.6V (figure 4.15).

The transfer curve in figure 4.16 shows the overall result of changing W_m when I_m and R_l are fixed. Usually the output swing is determined by $I_m \cdot R_l$, but this simulation result shows a smaller output range for a small W_m. This is because the gate leakage associated with the smaller W_m are larger and they restrict the current gain in the amplifier.

For larger transistors, the initial V_{gs} and gate leakage are small. When an input change V_{in} is applied to $V(gin, gre)$, the gate-source voltage of Q1 increases by $1/2V_{in}$ while that of Q3 decreases by almost the same amount. So, the current in

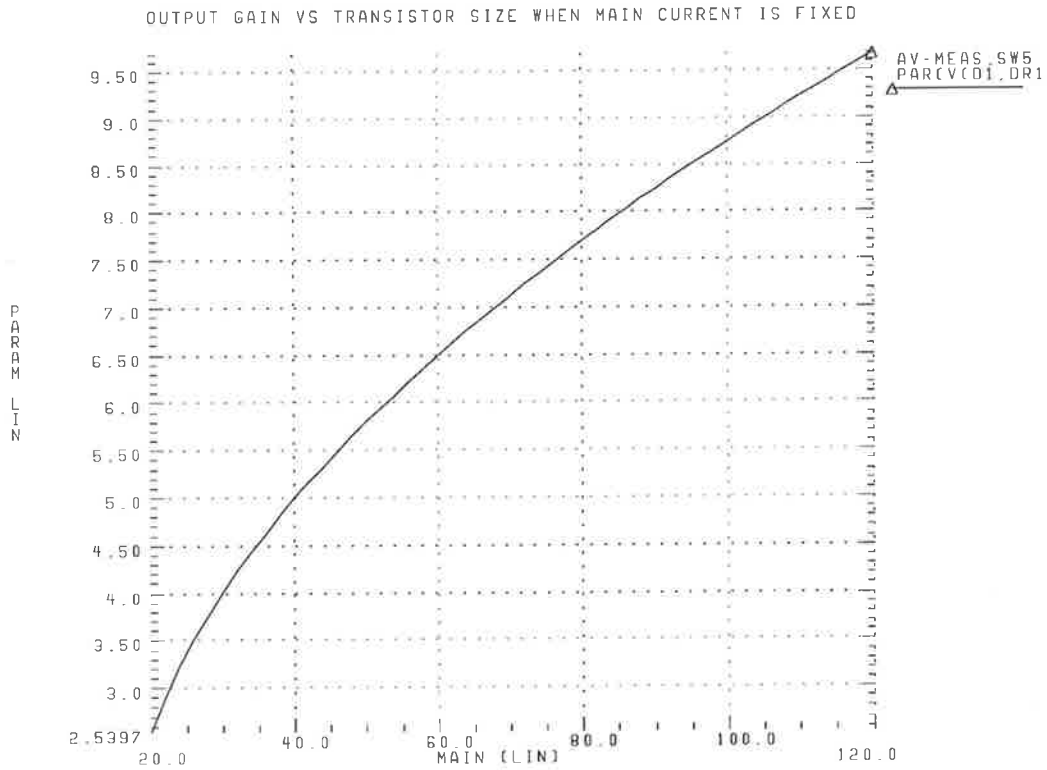


Figure 4.13: The absolute input gain versus main transistor size

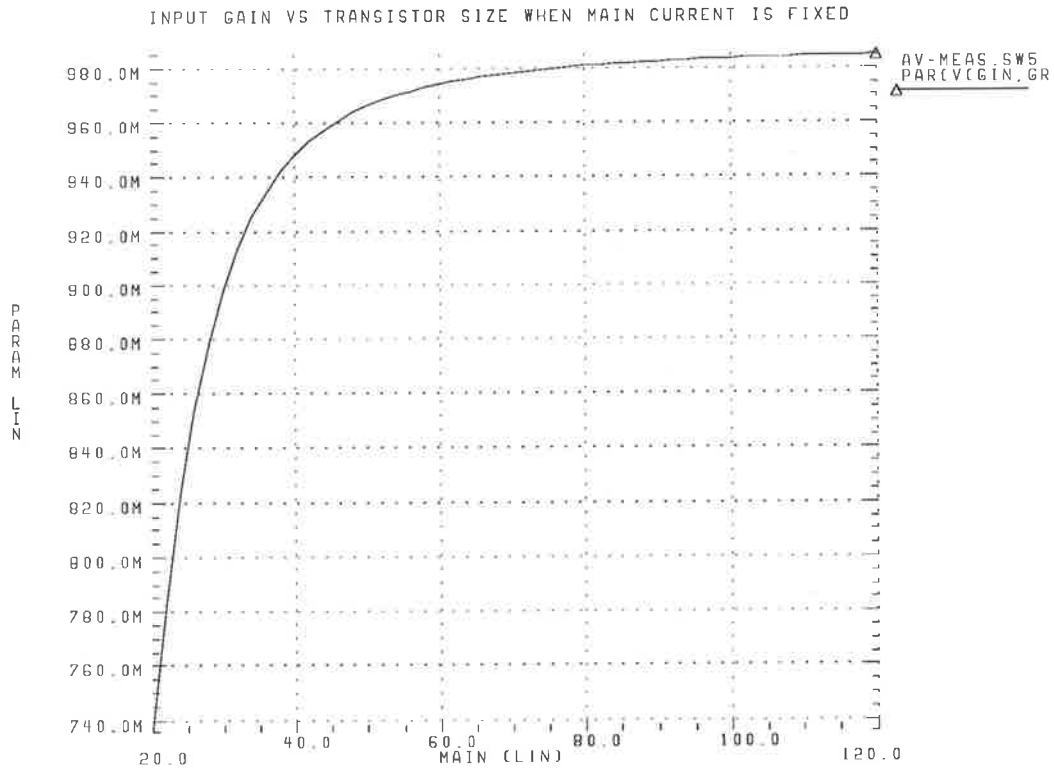


Figure 4.14: The absolute output gain versus main transistor size

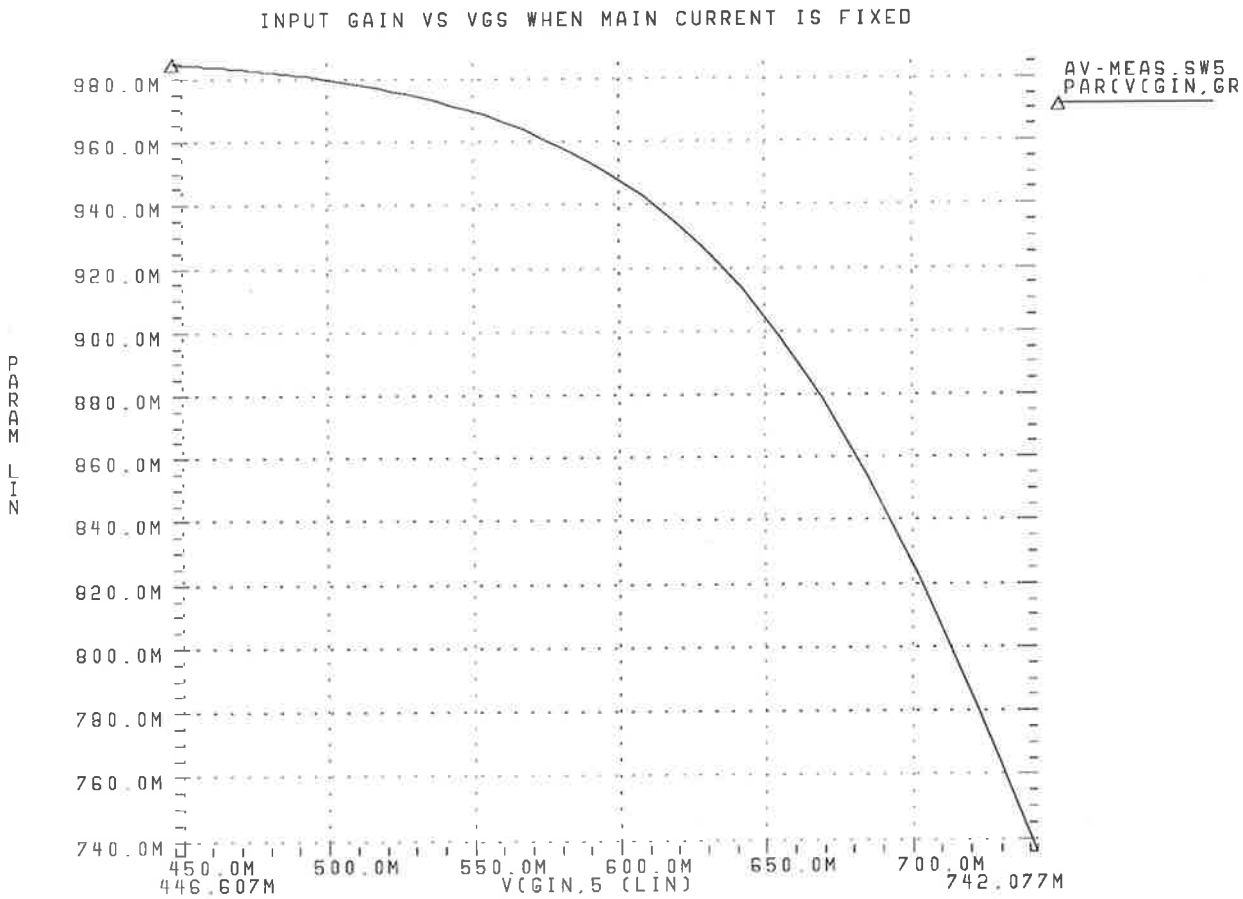


Figure 4.15: The absolute input gain versus V_{gs} of main transistor

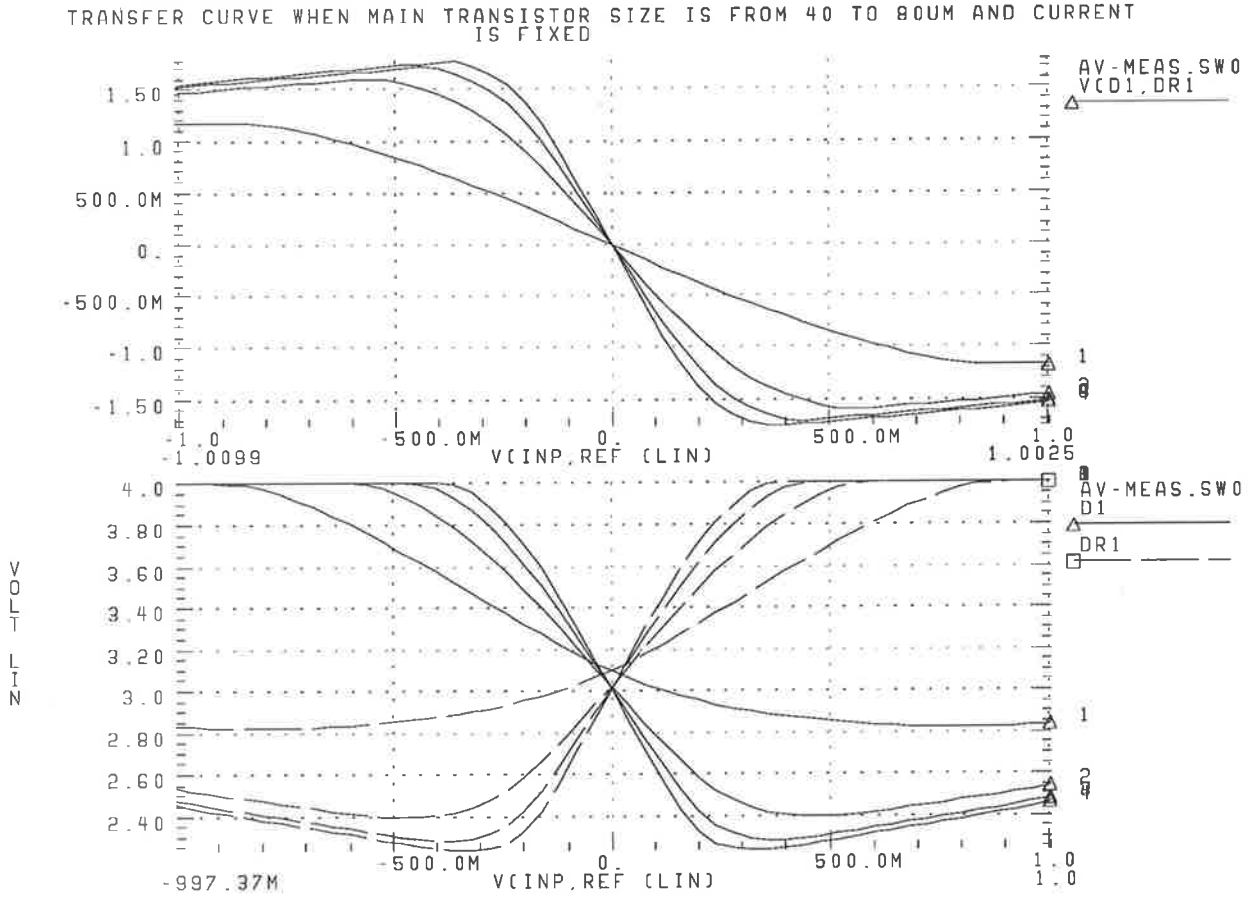


Figure 4.16: The transfer curve when W_m is changing

d1 branch increases and that in the dr1 branch decreases, meanwhile the leakage current in the d1 branch also increases. Because of the relatively large value of G_m for large transistors, the current switching is faster and it is demonstrated by the steeper slope in the transfer curve in figure 4.16.

Both branches of the amplifier remain working until the input increases to a point which turns off Q3 and all current needed to supply the current source will be drawn from the d1 branch. Since the initial V_{gs} of Q3 is small, and the room for Q3 to drop before it is turned off is also small, this point can be reached at small input voltages. The leakage is still small and the current is mainly supplied through the resistive load. This enables the output swing to reach a level very close to the maximum value of $I_m \cdot R_l$. Beyond this point, the input variation will be totally reflected on the V_{gs} of Q1 and Q2. Moreover, the decreased V_{ds} of Q2 will push its V_{gs} further for the same amount of current. This accelerates the increase of gate current. When gate leakage is increasing and the total current remains the same, the normal current is decreasing. This causes the decline of output differential voltages.

What happens in the case of small transistors is that a higher V_{gs} is activated and large gate current is drawn before input is applied. Due to the small G_m and large V_{gs}, the normal branch current is added slowly while the leakage supplies a significant part of the total current. Therefore, the output voltage not only goes up slowly it also stops and starts to decline before the branch of dr1 is turned off. Therefore,

the maximum output voltage can never be reached even though the V_o starts to drop at higher input voltage. It is also shown in figure 4.16, that the output of a larger transistor reduces faster than smaller one. This is due to the gate current of larger transistors increasing quicker.

In the case of the application of a large negative input, the common mode level V(5) will be pulled down. If the initial V(5) doesn't have enough room for the swing, the V_{ds} of the current source of the amplifier will become too small and I_m will be reduced or even turned off. This should be prevented when determining V_{dd} and $I_m \cdot R_l$.

Suppose V_{gs} is fixed and W_m of Q1 is changed. That in turn changes I_m. The result will be the same as when R_l is an independent variable, and the choice of V_{dd} is critical. So far, we have the perception that the power must be large to assure stable operation. In fact, when the power consumption is not a concern, the problem associated with a restricted V_{dd} in the study of high value of $I_m \cdot R_l$ can be eliminated and a very high gain is possible. However, a minimum power dissipation is also one of the important figures of merit. The minimum power supply voltage should be enough to provide the V_{ds} for Q1, Q2 when the output nodes are swing within the $I_m \cdot R_l$, and allows the current source to operate in saturation when the input is travelling in 1V range. Therefore, 4V is a suitable supply with $I_m \cdot R_l = 1V$.

4.2.3 Summary of gain constraints

The conclusion for the choice of the parameters for the highest gain with a compatible power supply and power consumption are:

1. large R_l but it should not cause insufficient common mode level and desaturation of the current source.
2. large I_m but care must be taken to prevent the same problem as R_l.
3. large W_m and keep V_{gs} small, a V_{gs} exceeding 0.6V should be avoided for Q1 - Q4. But it is not a restriction for the current source. Also a V_{gs} greater than 0.4V is necessary for the simulation model to fully characterise the circuit.
4. large I_f, however the effect of high I_f on the Av_{in} tends to saturate when I_f is sufficient for certain sizes of source follower and diode.
5. suitable size of W_f to keep the V_{gs} at 0.4V according to I_f.

In order to give a guide line for further study of the speed, the possible number of stages in cascade is investigated. Since the overall gain of the comparator must be greater than 100, assuming $Av_{cin} \cdot Av_{in} = 0.9$, $\beta = 2.59E-4$ and $V_{gs} = 0.4\text{V}$, $Av_{out} > 110$ is required and following two formula are used to estimate the values of parameters.

$$Av_{out} = -\frac{2 \cdot I_m \cdot R_l}{V_{gs} - V_t}$$

and

$$Av_{out} = -2 \cdot R_l \sqrt{I_m \cdot W \cdot \beta}$$

In the case of a single stage structure, $2 \cdot I_m \cdot R/(0.4 - 0.217) > 110$, so $I_m \cdot R > 10$V. Therefore a 12V power supply is required in addition to the large current and huge transistor to operate properly. For a two stage structure, $Av_{out} > 11$ is required, so $I_m \cdot R$ >1.0V is enough using 4V power supply, one milliampere current with a resistor of 1KΩ, and a transistor size of 110 μm is suitable. As for a three stage structure, $Av_{out} > 5.2$ and so $I \cdot R$ >0.47V is required. Therefore, a power supply less than 3.5V and a 50 μm transistor is needed to perform the specified functions.

4.3 The factors affecting operating speed

The conversion time specification provides an indication of the system sampling rate. The time needed to completed a conversion is expressed as:

conversion time (8 Bit) = 1 ns

or as a rate

conversion rate (8 Bit) = 1 GHz or simply 1 Giga sample/second.

When the speed of the comparator is considered, the following items must be investigated;

1. slew rate which is related to the driving current
2. poles and zeros which are directly related to response time and
3. the coupling by stray capacitances which may cause unexpected delay.

In addition the time needed for self calibration is also a major factor.

Slew rate is defined as the voltage swing driven by a output device per unit time. It is usually expressed in the form of $\frac{\Delta V}{\Delta t}$. Slew rate heavily depends on the driving capability of the output device and the load seen by it. Therefore, slew rate is also expressed in the form of $C \cdot \Delta V = I \cdot \Delta t$ when $Q = C \cdot V$ and $\frac{\Delta Q}{\Delta t} = I$ are combined.

In this design, assuming the output load is the stray capacitance C_{gd} of an 80 μm wide transistor gate and the slew rate is 1V/300ps, the current needed to satisfy this specification can be calculated,

$$0.26fF \cdot 80 \cdot 1\,V = I \cdot 300ps$$

$$I = 0.07mA$$

The current used to meet the required gain is more than enough to drive the out-

put load. Considering the slew rate of the source follower driving the amplifier, the input gates of the amplifier are in the range of 40 to 70 μm wide with a gain of approximately five, thus a current greater than 0.35 mA will be sufficient. The total resistance of the resistor ladder is around of 30 Ω when the voltage across the ladder is 1V. So the driving current is around 33 mA which is enough to drive 16 gate capacitances of 80 μm wide transistors with the same rate. Therefore, the slew rate is not a concern for the operation speed of this design.

Concerning the response time, the locations of poles must be studied. The pole is given by $s_p = 2\pi f_H = 1/RC$ and the rising time $Tr = 2.2RC = 0.35/f_H$[Millman] is defined as the time from 10 % to 90 % of voltage swing.

An energy storage element in a circuit forms a pole. In the analysis of the operating state of the design, poles can be found simply by locating the independent energy conservative networks in the simplified equivalent circuit as illustrated in figure 4.17.

Three poles are found in the circuit at:

$$s_{p1} = \frac{G_s}{C_{gdf} + C_{gsf}(1 - Av_{in})} s_{p2} = \frac{G_{mf} + G_{df} + G_o}{C_m} s_{p3} = \frac{G_l}{C_l} \tag{4.3}$$

where

$C_m = C_{gsf} + 2C_{gsm} + (1 - Av_{out})C_{gdm} + C_{gdo}$

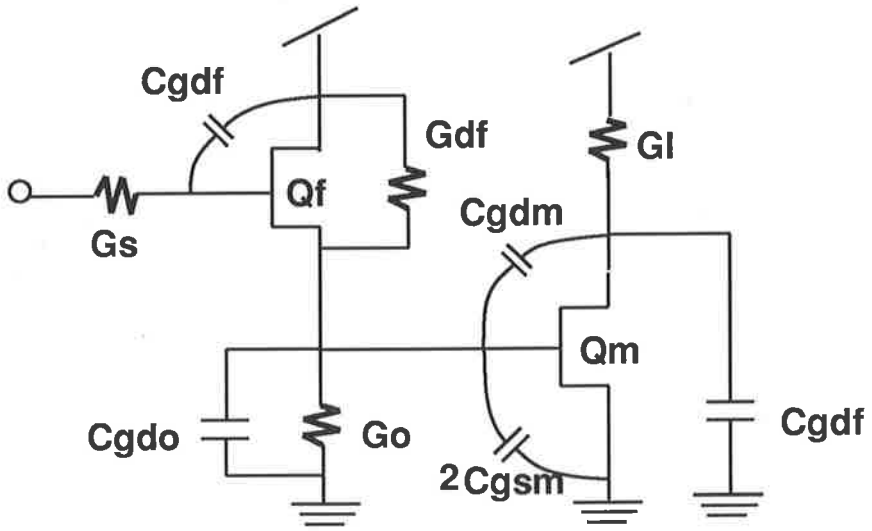


Figure 4.17: A simplified comparator equivalent circuit

$C_l = C_{gdf} + C_{gdm}$

This result is identical to what is found in the analysis in Appendix C. The two C_{gsm} in C_m is du to two input gates in the amplifier. From the locations of the poles we find that the circuit can be split into three modules. Each pole represents the speed of a module which can be investigated and modified individually for the response of the circuit. Those response speeds of the modules are called switching speed, input speed and the output speed. If any of the three poles satisfies $s_{pa} > 4s_{pb}$, then s_{pb} will be the dominant pole and the deciding factor of the overall response time. [Millman]

The locations of the poles are estimated based on the possible sizes of transistors used in the circuit. The results show that three poles are located in the

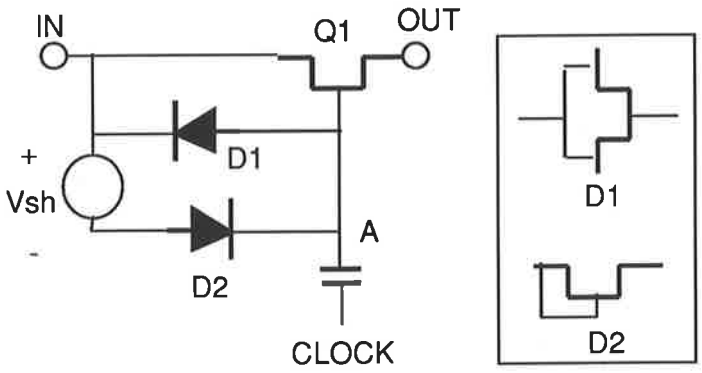


Figure 4.18: The analog switch

range 20 GHz to 75 GHz. Because they are very close to each other, there is no dominant pole in this circuit. So any change in the parameters can affect the speed of the circuit. In order to optimise the performance of this comparator, the effects of the values of each component on the response time are studied by observing the response at three differential voltages. These are defined as $V_s = V_{fo2g} - V_{for2g}, V_{in} = V_{gin} - V_{gre}, and V_{out} = V_{outp1} - V_{outn1}$ (Appendix D: meas-3da), these are detected at the input gates of the source followers, the input gates of the amplifier and the output nodes of the amplifier. They correspond to the switching speed, input speed and output speed respectively.

s_{p1} is related to the switching speed which is determined mainly by the channel resistance R_s of the switch when it is in the 'ON' state and the gate to drain capacitance C_{gdf} of Q_f. When C_{gdf} is a function of W_f and V_{gsf}, R_s is determined by the size of the switch W_s and the gate to source voltage V_{gs} applied.

The gate-source voltage of the switching transistor Q1 (figure 4.18) can be calculated as

$$V_{gss} = V_{in} - V_{sh} + V_{clk}(\frac{C_c}{C_c + C_s + C_{d1} + C_{d2}})$$

where

C_c is the coupling capacitance,

C_s is the gate capacitance of the switching transistor,

C_{d1} and C_{d2} are the stray capacitances of D1 and D2

Obviously, large values of V_{gss} and W_s lead to small value of R_s and high response speed. As discussed previously the clock swing must match the required voltage change at node A, and a high clock level must be under the limit of the maximum value for the feedback transistor of the amplifier. So the clock range may be determined and V_{gs} can be adjusted through the capacitance ratio and V_{sh}. When W_s increases, the channel resistance tends to decrease. At the same time the weight of C_c decreases and so does V_{gss}. So this change may increase or decrease the total R_s depending on the weight of C_c and the change of W_s.

When the sizes of the transistors and the capacitor are selected based on the consideration of chip area, V_{sh} can be used to shift the level at node A and determines the V_{gss}. However, a very high value of V_{gss} causes overshoot at the output node while it gives small R_s and a short response time. The overshoot will take quite a long time to recover, and it also needs some time to make up the lost charge

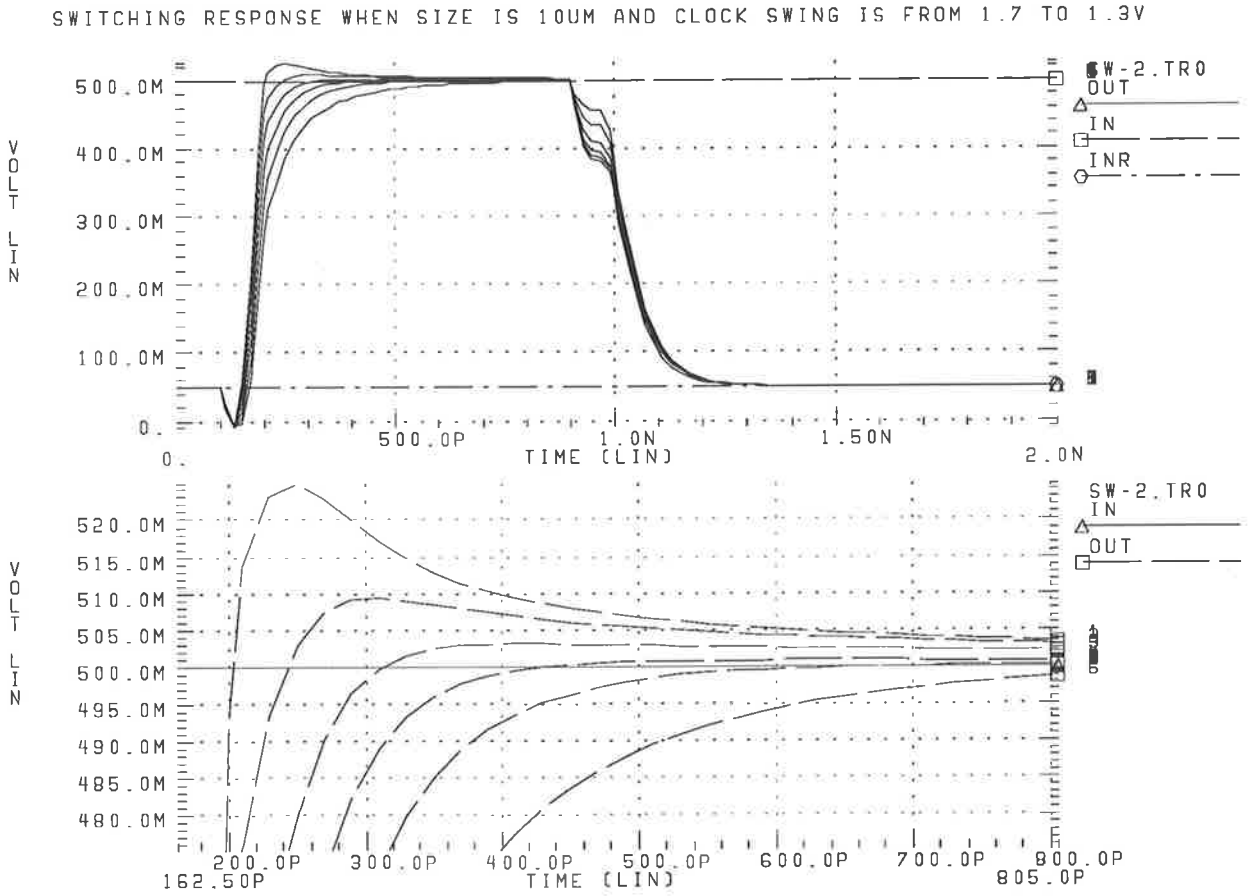


Figure 4.19: The switching response of a 10 μm wide switch when clock swing is 1.3V (bottom) - 1.7V (top)

from node A in the next cycle of operation. Figure 4.19 and figure 4.20 show the transient simulation of a switch in which C_c is 0.1 pF, clock swings vary from 1.3V to 1.7V with the high level fixed to 3.3V, V_{sh} is 0.8V, diodes are 10 μm wide and the switching transistor is 10 μm wide in figure 4.19 and 20 μm wide in figure 4.20. D1 is not included in these simulations.

A 20 μm wide transistor is chosen for the switch. Because it gives 0.5V for V_{gss}

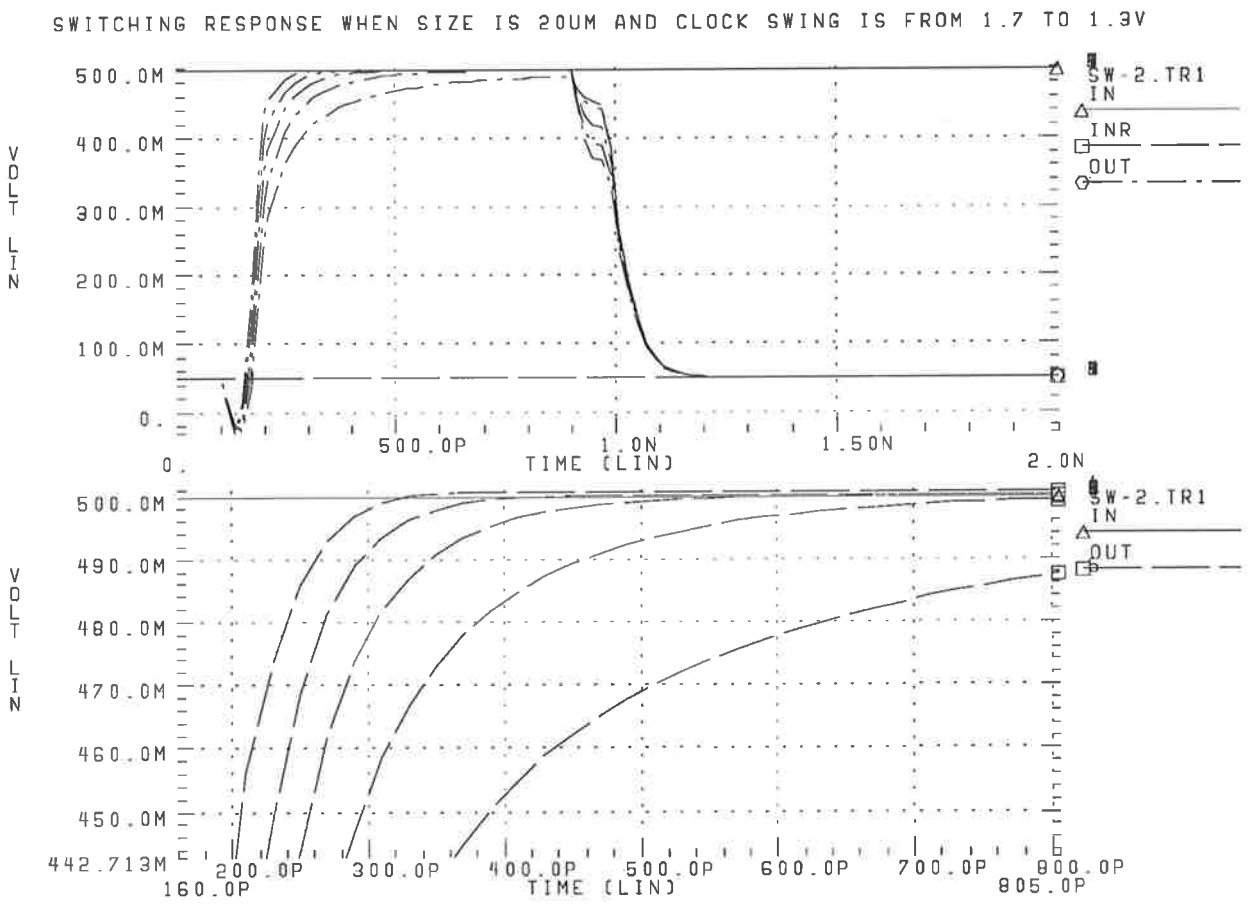


Figure 4.20: The switching response of a 20 μm wide switch when clock swing is 1.3V (bottom) - 1.7V (top)

when clock is high, and 2K-5K Ω for R_s. So the rise time can be estimated to be 200 ps for a 80 μm wide Q_f.

Changing Q_f varies C_{gdf} but not significantly, because the larger W_f is, the smaller V_{gsf} will be when I_f is fixed. Smaller V_{gsf} will reduce C_{gdf} by the widened depletion layer under the gate. So the size of Q_f is not an important factor for the switching speed. However, a very small Q_f should be avoided because it provides a large V_{gsf} and in turn increases gate leakage which degrades the input signal and causes charge loss from the gate of Q_f.

As well as being an important factor for the input gain, the source follower current I_f is also a critical variable of the input speed. Figure 4.21 shows simulation results of a cascade structure comparator. Three groups of curves are selected to demonstrated the response of the first stage of the comparator. The top group represents the switching speed. The middle group are the response of V_{in}, and the output curves representing V_{out} are the bottom group. The simulation file is attached in Appendix D (meas-3da).

Because the behaviour of V_s, V_{in} and V_{out} are independent of each other, the rise times can be calculated by using following equation [Millman],

$$Tr = 1.1\sqrt{T_r1^2 + T_r2^2 + T_r3^2 \cdots} \tag{4.4}$$

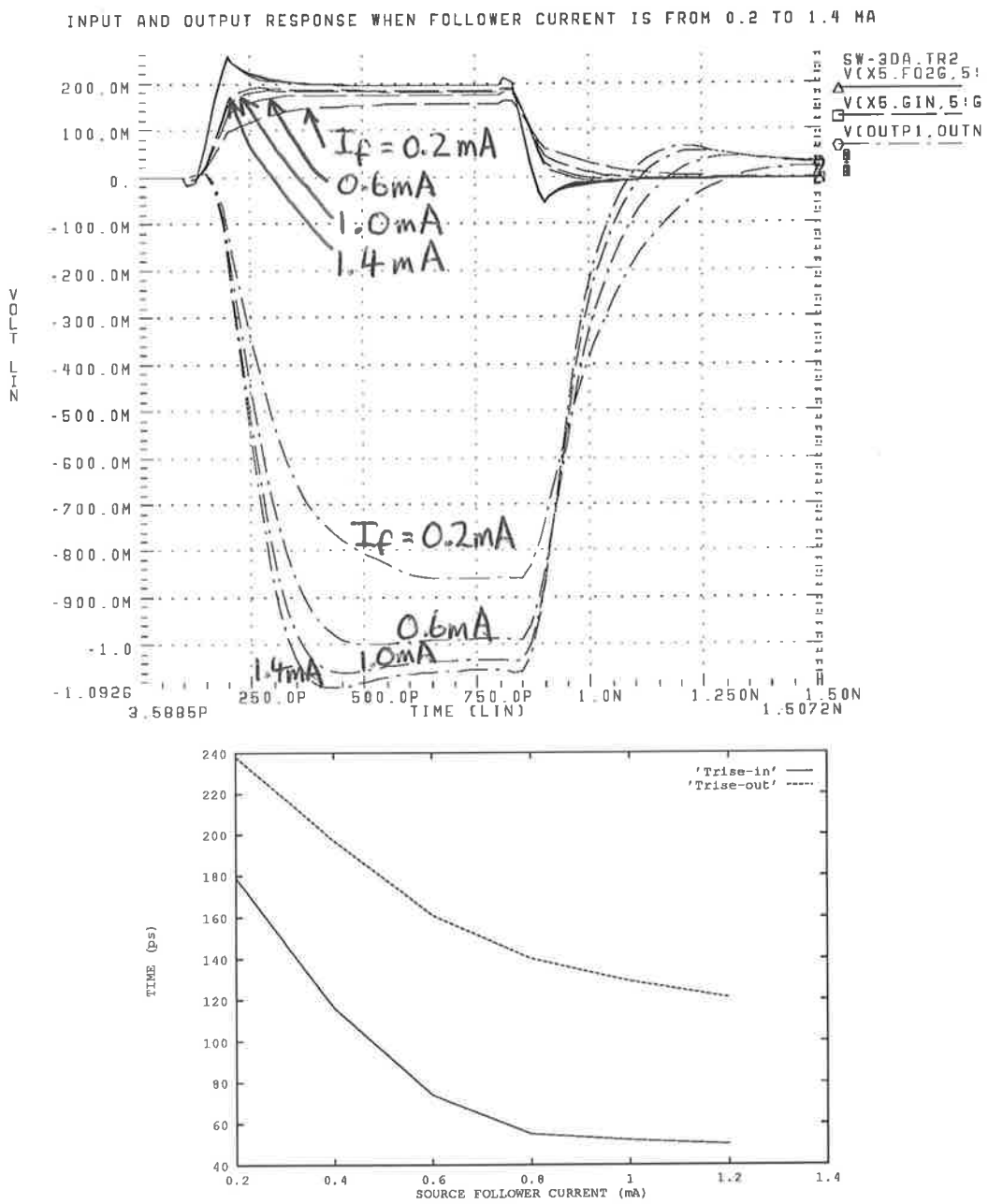


Figure 4.21: The response and rise time versus source follower current

when a comparator stage is analyzed a series of non-interacting modules.

Figure 4.21 show that switching speed is not affected by changing I_f while the input speed is dramatically improved by a high value of I_f. The fact of hardly changed switching speed is also seen in other simulations. Since the output rise time is the sum of the input response time and the output response time (equation 4.4), the decline of output rise time here is due to the reduction of input rise time rather than the decrease of output rise time itself. It is also found that the effect of I_f is much more significant when I_f is small.

When I_f is very small the slew rate becomes the main factor of the slow input speed. Moreover, the associated small values of G_{mf} and G_o also pull s_{p2} to a low frequency when a larger I_f incurs large G_{mf} and G_o which generates a large value of s_{p2}. Nonetheless, a very large value of I_f does not improve the performance indefinitely, because the change of G_{mf} is limited by the V_{gs} of Q_f assuming W_f is fixed. Figure 4.21 also shows the rise time measured when the source follower current is changing. Although, a larger size of Q_f and high value of I_f can further improve the input speed, the improvement is relatively small and the switching speed will degrade after some time. So there is no much benefit to over all response time for a large source follower.

The size of the transistors, which form the differential amplifier, plays a significant

role in determining the input speed. In the expression of s_{p2} (Eq.4.3), the gate to drain capacitance multiplied by the output gain (Miller effect) plus two times the gate to source capacitance creates the major part of Cm. The transistor size W_m therefore plays a critical role in the input speed.

In addition, W_m is also an important variable for output response because the C_{gdm} of Q_m in the expression of s_{p3} (Eq.4.3) is directly related to W_m when C_{dsm} is negligible. Since both input and output rise time increase with increasing W_m, the two curves of rise times in figure 4.22 display a increasing gap between them.

Another major factor in determining the speed is the resistive load R_l. It can be very easily seen that s_{p3} is directly proportional to R_l while R_l does not influence input speed at all. This is shown in figure 4.23. It is also found in the study that the amplifier current I_m and the V_{gs} of Q_m has very little effect on the response time. The data measured for the figures of rise time are displayed in Appendix D: data

One contributor to the response time is coupling which can be found in the path from the input capacitor to node *gin* or *gre* (figure 4.6). They appear when a voltage change is applied to either input node of the comparator. It can be coupled through the stray capacitances in the circuit or through the power rail to the other side of the comparator. It reduces the amplitude of the differential input voltage and takes

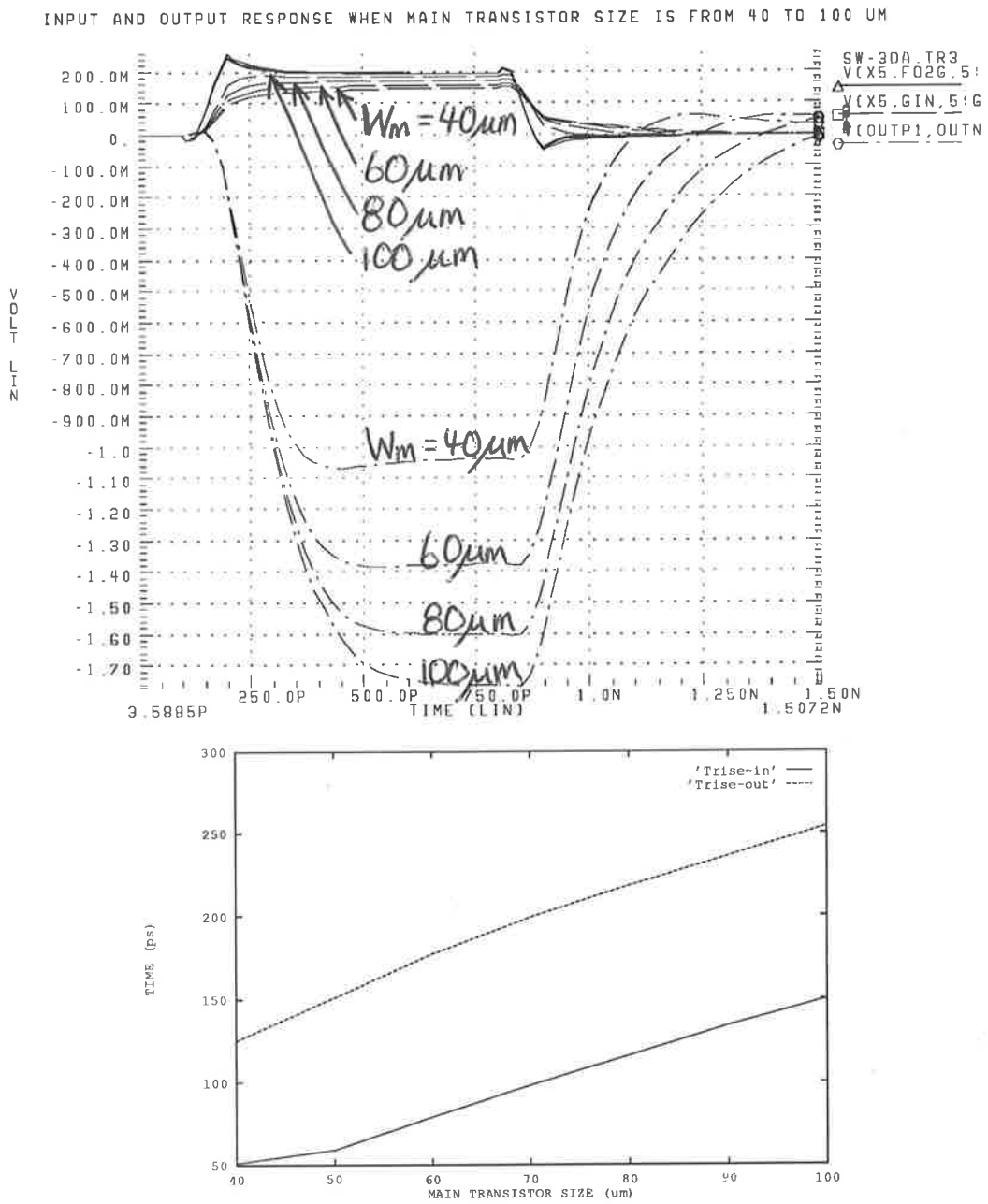


Figure 4.22: The response and rise time versus main transistor width

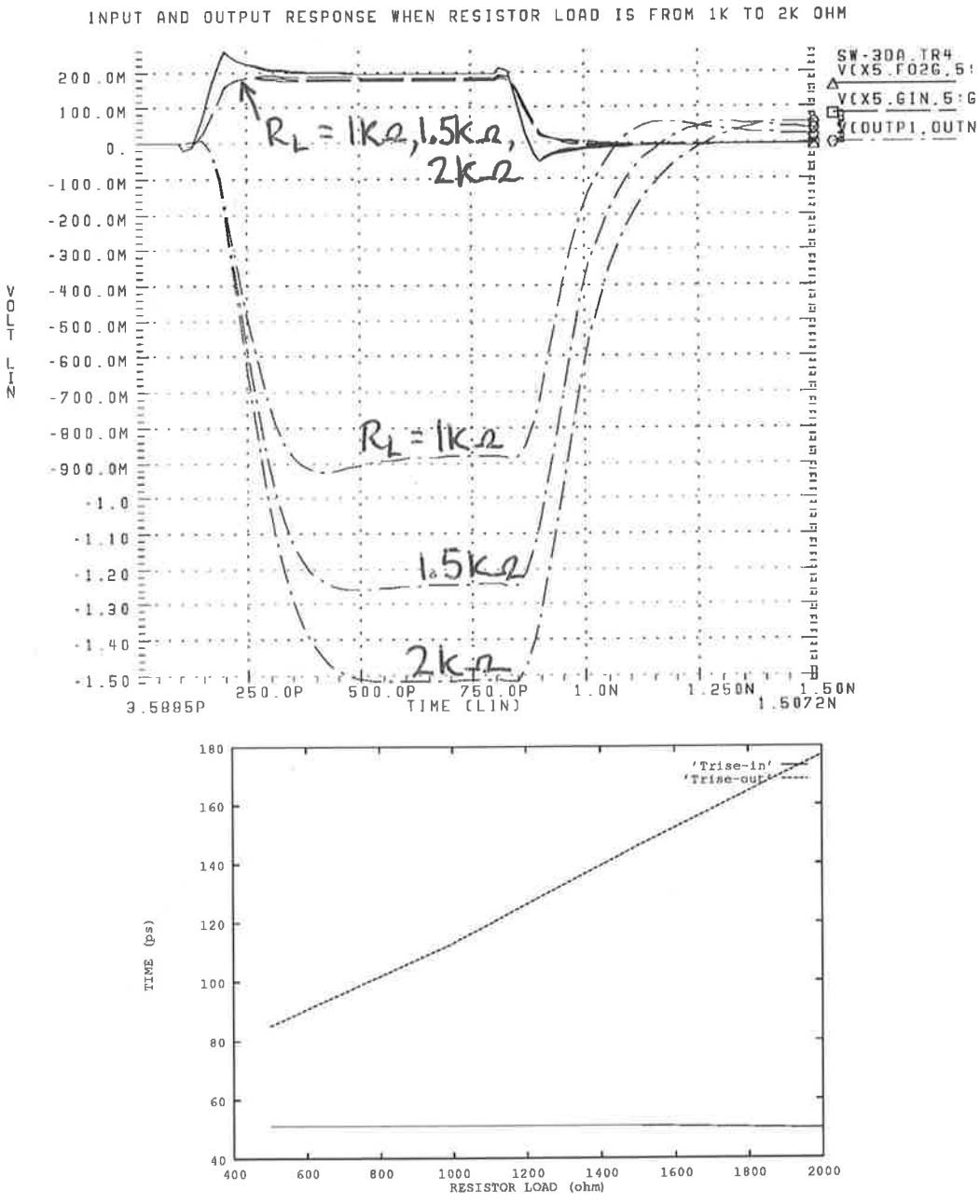


Figure 4.23: The response and rise time versus resistive load

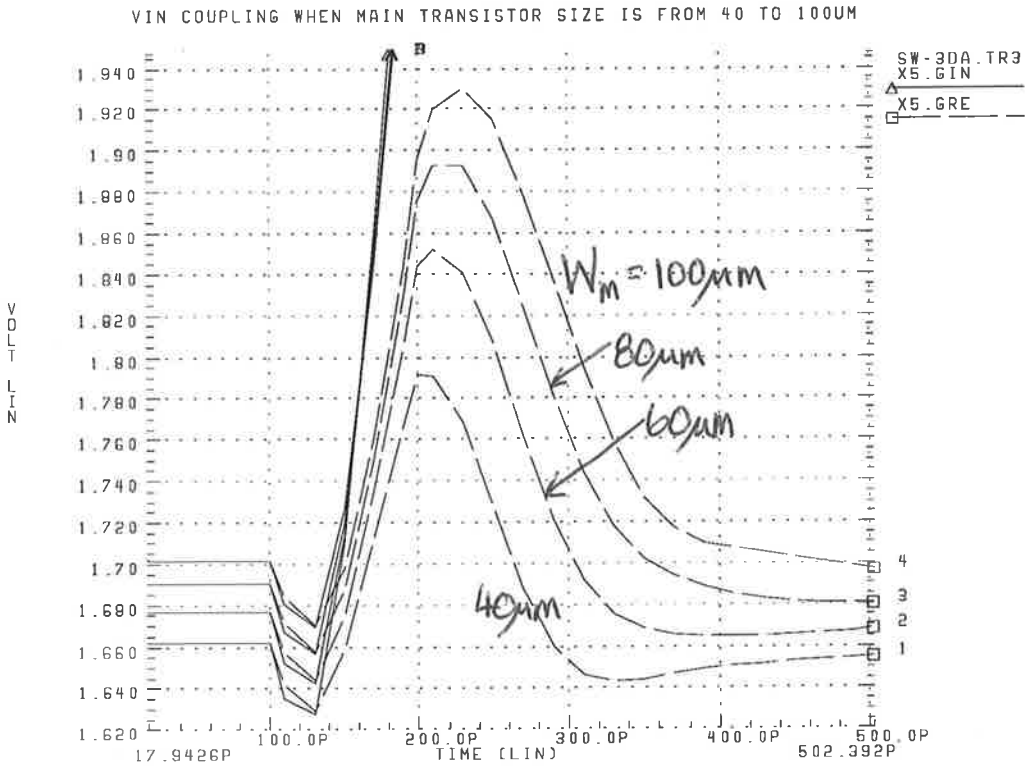


Figure 4.24: Coupling at V_{in} versus main transistor width

time to reach a stable level. Coupling is a function of stray capacitances and the amplitude of input voltage changes. Figure 4.24 shows the coupling detected at node *gre* when 700 mV is applied to node *gin*. The amplitude of the coupled signal is proportional to the size of the transistors of the amplifier and the time needed for the coupled signal to settle also increases with the transistor size. Fortunately, the current in the source follower I_f can reduce both the amplitude and the settling time of the coupled signal (figure 4.25). Coupling is also found at the input capacitors. This can be minimised by reducing the resistance of the input switches.

Self calibration is a major time consumer in the operation. It starts when the

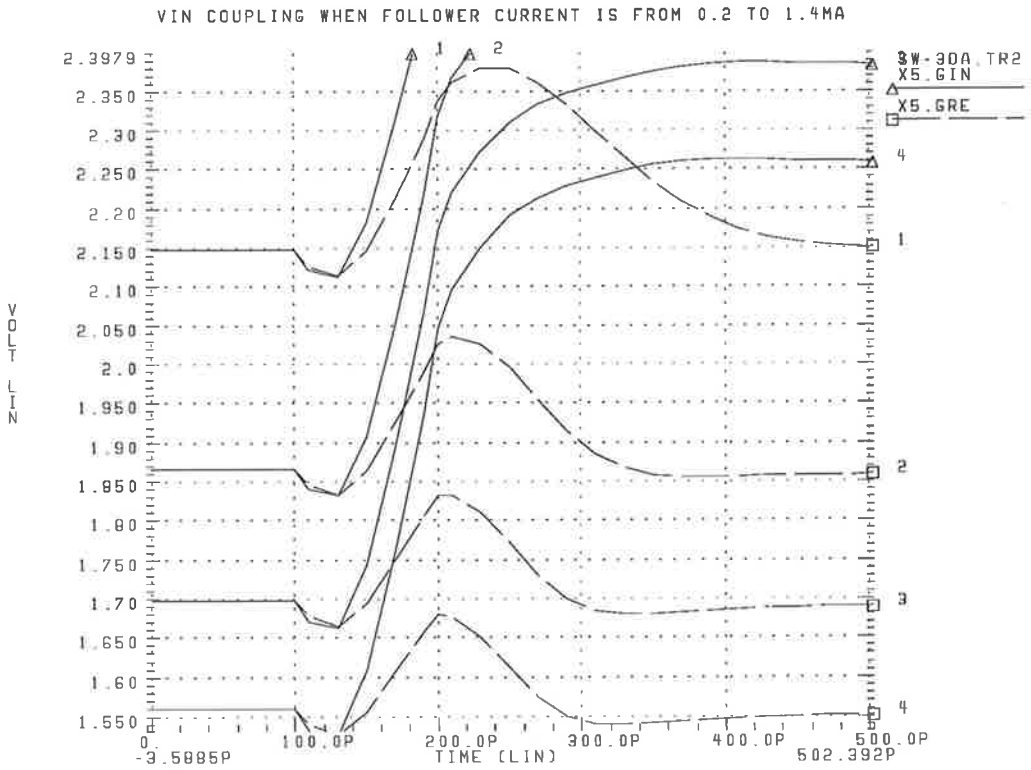


Figure 4.25: Coupling at V_{in} versus source follower current

feedback switches of the amplifier are closed until the output voltage of each amplifier stage is stable. The comparator becomes unstable when a feedback loop is formed by the switches and ringing effect shows during self calibration period. This is believed to be caused by the close proximity of the poles [Millman] [SEDRA]. As shown in figure 4.26 and figure 4.27 the time needed for the ringing to settle heavily depends on the size of input switch, W_s and the main transistor, W_m. It is also found that the ringing effect will disappear when input switches are replaced by ideal voltage sources. The nonideal switches therefore contribute to ringing effect and the efforts for minimising this effect is in line with that for high speed operation. Consequently, in our design it takes 500 to 600 ps for the ringing to settle to less than 5 mV.

The conclusions for the choices for improved response speed are

- large source follower current
- small main transistors width
- small value of resistive load
- small size of Q_f but should avoid $V_{gss} > 0.4V$.
- suitable size of switch, according to the capacitance ratio and the clock swing.

A 20 μm wide transistor is selected for the design.

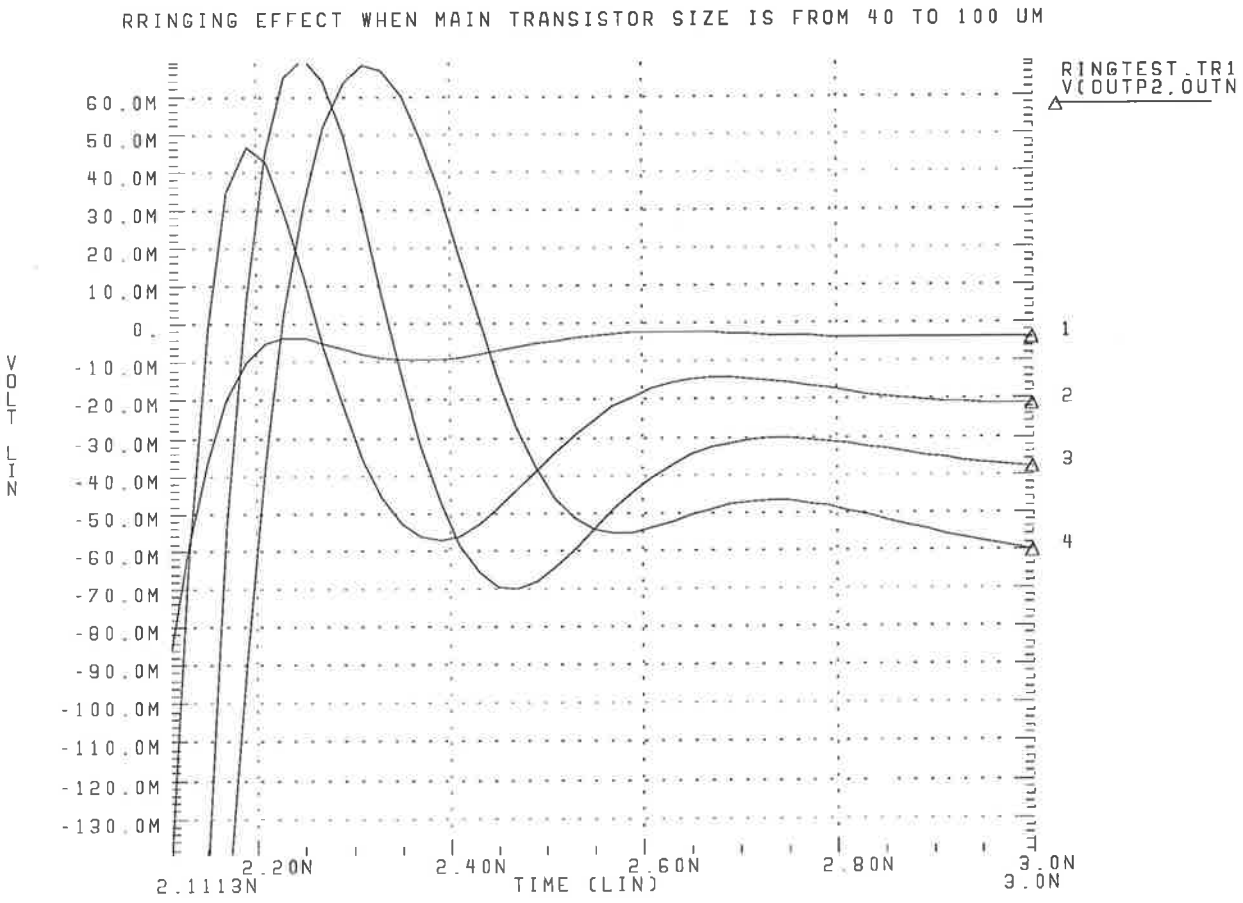


Figure 4.26: The ringing effect versus main transistor size. Mark 1-4 represent W_m value from 40-100μm

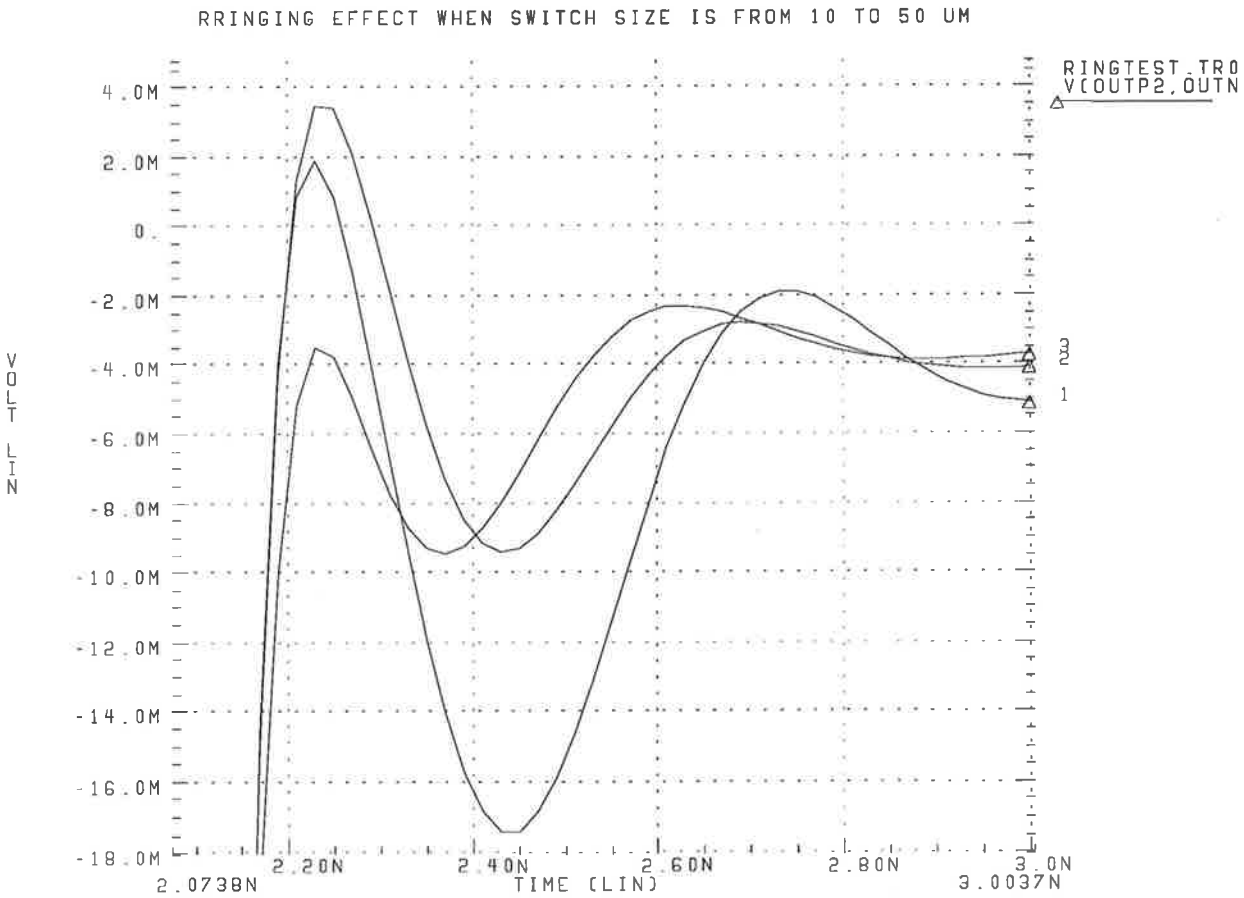


Figure 4.27: The ringing effect versus switch size. Mark 1-3 represent W_s value from 10-50 μm

4.4 Comparator parameters

From the discussions in previous sections, the final choice of device parameters may be done. As explained in section 4.2, a single stage comparator is not suitable for our design. This conclusion is also confirmed in the consideration of speed because to achieve the required gain and proper operating conditions, a transistor greater than 1 mm wide is needed. The responding time is estimated to be around a few nanoseconds.

If two cascaded stages are used, the transistor size used in the amplifier is around 110 μm wide and the output rise time for a stage is 470 ps by extrapolation. The formula for a cascaded structure of identical stages must be applied to calculate the total rise time of the comparator. [Millman]

$$\frac{f_H^*}{f_H} = \sqrt{2^{1/n} - 1}$$

where

f_H is the high 3dB frequency of a single stage

f_H^* is the high 3dB frequency of the cascaded stages

n is the number of stages.

From $Tr = 0.35/f_H$ we have

$$Tr^* = Tr/\sqrt{2^{1/n} - 1}$$

So, the total rise time for a two stage structure is estimated to be 712 ps. There are two rise times and a self calibration included in one completed conversion cycle. This removes the possibility of using a two stage comparator to reach 1G conversions per second. In the three stage structure, the transistor size W_m is about 50 μm. Thus the output rise time for an individual stage is estimated to be 180 ps, and the overall rise time is about 360 ps. Multiplying the rise time by two and adding the time needed for self calibration, a completed cycle needs 1.3 ns. To drive the amplifier faster, smaller transistors must be used. This will push V_{gs} higher, which incurs more gate leakage and sacrifices the output gain by enlarged $V_{gs} - V_t$. However, larger current can be drawn to make up the gain loss. Moreover, the high value of V_{gs} is acceptable as long as the output differential voltage at 1V input is much greater than the initial differential voltage at the end of self calibration. Therefore, 40 μm transistors are used with the gate to source voltage pushed up to 0.55V. Figure 4.28 demonstrates the simulation results at the outputs of the three stages of the comparator. A total cycle time of 1.4 ns is obtained. The simulation file is similar to the file meas-3da for speed measurement except there are no measuring instructions.

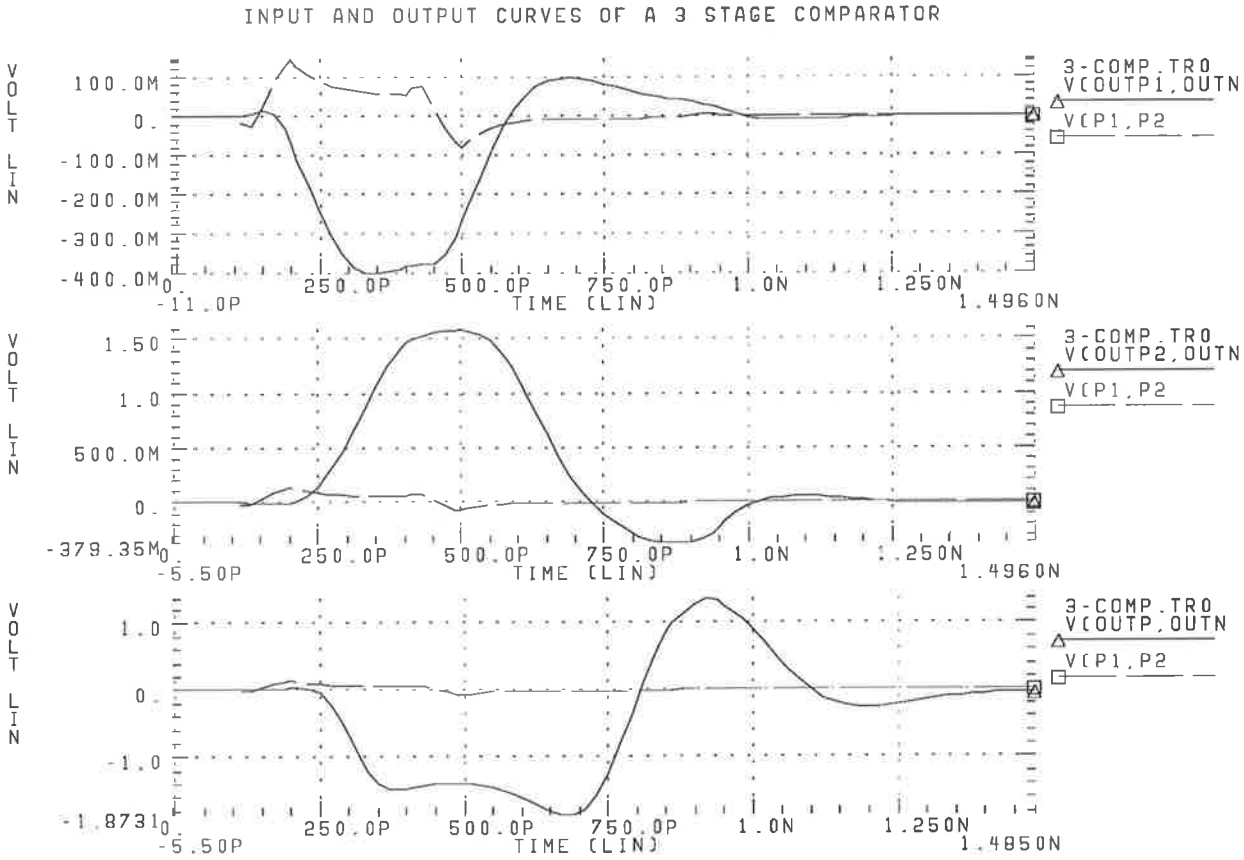


Figure 4.28: Simulation of a three stage comparator

Chapter 5

The layout of the ADC

Layout is the procedure to convert circuit specifications into a series of patterns which will then be placed on a set of masks for IC fabrication. A layout rule is the link between the circuit designer and the process engineer during the manufacturing phase. Over the years, there have been several approaches used to describe design rules. The most commonly used rules are the lambda-based and micron-based rules. Lambda rule were made popular by Mead and Conway for silicon, which characterizes the lines width and resolution of the chip. But due to the degradation in circuit performance, lambda-based rules are not suitable for GaAs processes [ESHR]. Micron-based rules specify directly the minimum required spacing, width, overlap $\cdots$ etc. which can be applied immediately for mask making.

The main objective associated with the layout rule is to obtain the circuit with optimum yield with as small geometry as possible without compromising the reliability. An aggressive rule increases the probability of improvements in circuit performance at the cost of yield when a conservative rule tends to assure the functioning of the integrated circuit. So, usually the rule is a compromise of process yield and circuit performance and very often the rule is determined by process designers and the manufacturing equipment. A layout rule suitable for 0.7 μm gate length process is provided by Philips Microwave Limiel (PML) foundry for this project.

5.1 Layout tools

Layout rules have been implemented using Magic version 6 CAD software. Based on the Mead-Conway style of design, Magic is developed by UCB and Western Research Laboratory in U.S. It uses simplified design rules and circuit structures. For example, Magic permits only vertical and horizontal edges of the geometries (Manhattan design). The conservative rules make it easier to do circuit design at the cost of 5-10% density loss. Like many other layout tools, Magic uses boxes as the base to build cells and interconnects. Magic is hierarchical, performs on line DRC, produces CIF etc etc ... Magic's normal extraction is to lump resistances on a node

into a single value. In branch networks this approximation is often not available. It includes accurate path length extraction which is an important feature when dealing with high speed circuits.

Layout normally needs to capture both layer and topology information. The advances that are taking place in GaAs are very complex and some what inhibit the visualization of all the mask levels used in the fabrication process. Color coding and symbolic presentation removes much of the complexity associated with a given design. The color coding used in Magic is described briefly.

Green: implant or diffusion layer

Blue: first metal layer (metal 1)

Purple: second metal layer (metal 2)

Red: shallow n- layer

Gray: contact metal

Brown: gate metal

Black cross: via between metal 1 and metal 2

Yellow: the metal layer for the top plate of capacitors.

- Green color identify all the active regions which eventually forms DFET, EFET, active loads, Schottky diodes and implant resistors.
- Green inside red layer forms n- channel for EFETs.

- Brown overlap green forms Schottky gate.
- Implant resistors are formed with the same structure as transistors without gate metal.
- Capacitors are built with Blue on the bottom, Yellow layer for the top plate Purple on the top and a via to connect the top plate and metal 2.

5.2 General layout considerations

In addition to the specified widths and spacings for building cells and blocks of an IC, some general but important conventions should be implemented in the layout to reduce the possible and unexpected errors in the performance of the IC after the fabrication.

First the communication paths between cells and positioning of power and ground buses have significant influence upon the performance of high speed VLSI systems. For example, in high frequency switching operation, the clock lines are usually the noise makers. Through the parasitic capacitance between parallel lines, the noise in clock lines will be coupled to their neighbours. Therefore, an unshield power rail will carry the noise to every where in the circuit. This is especially true for GaAs ICs since they are usually used in high frequency operation. Thus, long signals and global control paths are conveniently run in parallel, with a ground bus located in

between the two to reduce the fast transient coupled to V_{dd}.

Second, the layout is required to be as symmetry as possible over the chip. Since this circuit uses fully differential architecture and the accuracy is a major concern of this design, the electrical differences caused by the physical asymmetry should be avoided. This includes the variation of capacitive load incurred by different lengths of interconnections and the influence from the adjacent environment. In the building of cells, active devices are usually placed in the center.

Third, there are power supply and ground line distribution rules. The prime prerequisite for power and ground lines are to provide constant and equal voltage to all the devices on a chip. However, the issues which will determine the performance are [ESHR].

- metal migration
- voltage drop

If the current density in a metal line exceeds a threshold value, the metal atoms begin to move in the direction of current flow. When there is a constriction in the line, metal atoms move at a faster rate which subsequently result in constriction to blow like a fuse. For the PML process, the limit of the current density of metal 1 with fixed thickness is 3 mA/μm and 6 mA/μm for metal 2.

Voltage drop associated with the ground bus deteriorates the noise margin of logic gates. The variations in ground potential is determined by the product of the current in the bus and the resistance of the section of conductor which can be calculated by using

$$R = \frac{\rho L}{A} = \frac{\rho}{t}(\frac{L}{W})$$

where ρ is resistivity (Ω-cm)

L is length in cm

t is thickness in cm

W is width in cm

A is area in cm_2

The resistance can be rewritten as

$$R = R_s(\frac{L}{W})$$

where R_s is sheet resistance ($\Omega/\square$) and a $\square$ is defined as L/W of the conductor. To minimise the ground potential variation, the resistance of the ground bus should be minimised. It is also recommended by PML that the voltage difference between metal lines should be kept below 1.5 V/μm to avoid possible damage of the bulk GaAs and unexpected backgating. As for the width of signal buses, the resistance is inversely proportional to the width. However, the capacitance is proportional to its width. The RC value is nearly constant and independent of line width. So the layout of signal lines just follow the minimum width and spacing rules.

In addition to the size and spacing rules which are in common with silicon ICs, a special requirement for GaAs layout is that all the gates of MESFETs must be in one direction. Aligning substrate to give maximum gain. GaAs exhibits different transconductance in different directions due to lattice structure of material. Another main difference from the rules for silicon ICs is the space between gate contact and source or drain (S/D) contact. Due to no native gate oxide isolating the gate from S/D a space is required to assure acceptable reverse breakdown voltage for the Schottky barrier. And also to minimise the influence of parasitic capacitance.[ESHR]

5.3 Thermal design

Thermal considerations are a critical issue in layout. Because the temperature raise due to the heat generated and accumulated in the chip, will enhance all failure mechanisms. First, the threshold voltage and carrier mobility decrease. So the switching speed of transistors degrade. Then, electron migration and hot electron injection effects worsen, junction leakage increases and corrosion mechanisms accelerate. Also structure problems will appear at the interfaces of different materials because of different temperature coefficients. Therefore, in the thermal consideration the heat generated in the chip must be conducted away by the packaging, and its effects on the circuit performance must be minimised by using the techniques of circuit design and layout.

Minimizing the effects of heat can be achieved through

(1) reducing heat generation by using low voltage power supply and low current.

(2) designing a less temperature sensitive circuit.

(3) properly distribute the heat over the chip. The first two tasks must be done at the design phase and the third one can be achieved by careful placement of the heat sources of the circuit. Described in *"Thermal modeling of MOS Integrated Circuit"*[NOSH], the thermal effects and interaction in DAC operation are activated through

- The self heating effect of heat generating elements
- The thermal interaction of the heat generators
- The thermal effect of heat generator on non-heat generating elements

The concept is expressed mathematically as

$$T_i = T_i^{self} + \sum_{j=1}^{N} T_{j \to i}$$

The heat generators are the current sources in this case. The actual temperature rise is a function of the number of current sources, their separation and power consump-

tion. Placing the counterparts of differential structures symmetrically to the heat source can reduce the effect by common mode rejection. Another solution is to place the sources at a large separation from each other at the expense of area "real estate".

5.4 Some layout techniques

The performance of an IC is heavily dependent on process variations . While this problem is not yet able to be eliminated by process technology (if ever), design may somewhat reduce the damage through design and layout techniques. In this section, some techniques used in IC layout to minimize the influence of process non-uniformity are discussed. [PML][EPFL1]

5.4.1 Control of absolute value

In silicon technology, transistors are defined by a diffusion region surrounded by other types of diffusion. At the ends, contacts are installed to build the low resistance interconnection. Due to the different shapes of the resistor and the contact, the resistance is not the same as in the uniform part of the resistor. Therefore heavily doped low resistivity diffusion regions are used to terminate the ends of the resistor

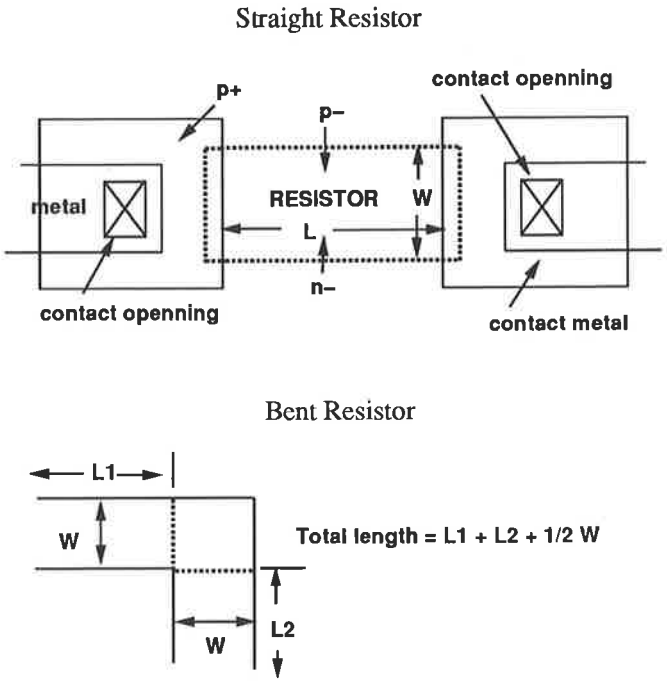


Figure 5.1: Resistor layout

(figure 5.1).

The value of the resistor is calculated between the edges of the heavily doped diffusion regions. In GaAs, contact metals are placed at the ends of the diffusion regions for transistors and resistors, and the edges of the contact metals the the edges of diffusion to produce a good termination. Another uncertain resistance occurs in the bends of a resistor. Although the resistance of the bent area can be estimated as a $\square/2$, it should be avoided at any possibility for a better control of the resistance.

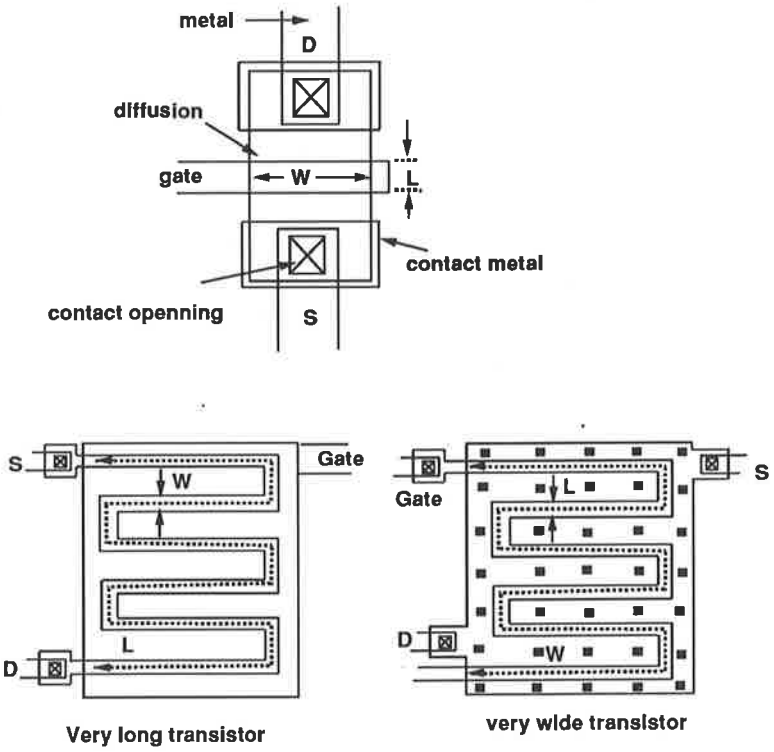


Figure 5.2: Layout of transistors

5.4.2 The layout of very large transistors

Figure 5.2 shows the basic structure of a transistor. In some cases very large transistors are needed in an IC either very long or very wide. To minimize the area used for large transistors, they are drawn in finger shapes. Very often contacts are placed in the fingers to reduce the source and drain series resistance.

5.4.3 Matching structure

Device matching is especially important for GaAs differential circuits. Because the GaAs process is not as mature as silicon, the difference between devices heavily rely on the locations and how they are drawn. So, extra care must be taken to ensure the best matching of the counterparts of the differential structure of the ADC amplifiers and between comparators. Matching structure is to design the same type of device with one structure. For example, the diodes in the source follower of the ADC comparator should use either diode connected transistors or simple Schottky junction diodes, but not both.

5.4.4 Matching thermal effects

To minimize the mismatch caused by the influence of temperature, the matched devices must be placed symmetrically to the heat source.

5.4.5 Matching shape and size

The same shapes and sizes must be used to draw the matched devices. Although the required performance can be achieved by the ratio ($R = R_s \frac{L}{W}$) or the product ($C = C_{unitarea} \cdot L \cdot W$), the variations of sizes are not proportional to the absolute values. Therefore, differences will occur to the devices with different shape or size.

5.4.6 Minimum distance for matched devices

In order to minimize parameter differences between matched devices caused by process variation and non-uniformity, the matched devices must be placed in close proximity. In doing this the process sensitive and temperature sensitive devices are the priorities.

5.4.7 Matching common-centroid geometries

Quad structured transistors is an example of this technique to compensate the constant gradients. In this structure, four transistors are placed in a group and are connected diagonally to form a pair of larger transistors. Due to the cross placement the counterparts share the location related variation to each other. However,

this structure increases the complexity of routing and takes much more chip area.

5.4.8 Matching orientation

Aligning FET gates in the same direction is mandatory for GaAs devices while it is a good approach for silicon ICs to eliminate the dissymmetries of unisotropic substrate, unisotropic process steps, and stress after packaging.

5.4.9 Matching the surroundings

Due to various possible reasons, which are not yet clear, devices with different surroundings generate variations in their performance. Thus, dummy devices are used to create identical surroundings for matched devices (figure 5.3).

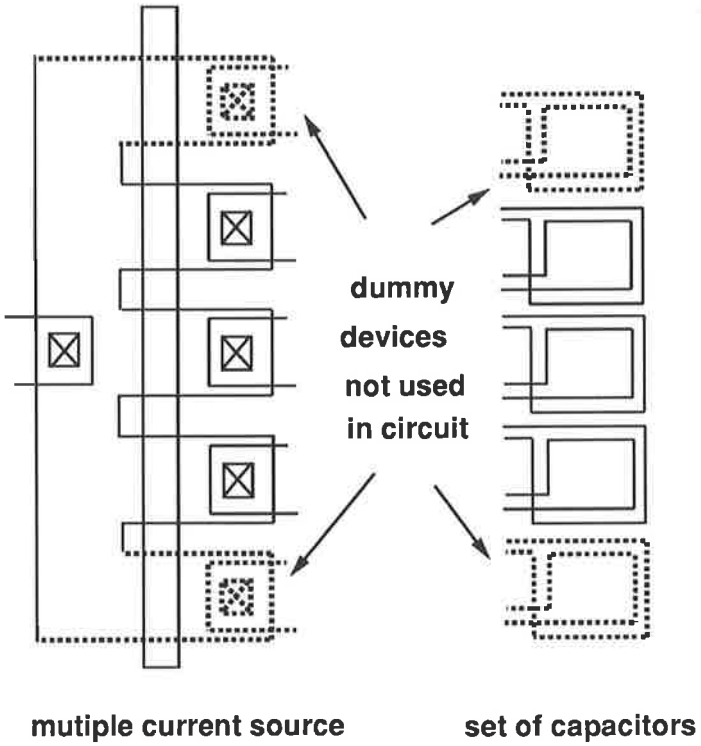


Figure 5.3: Matching surroundings

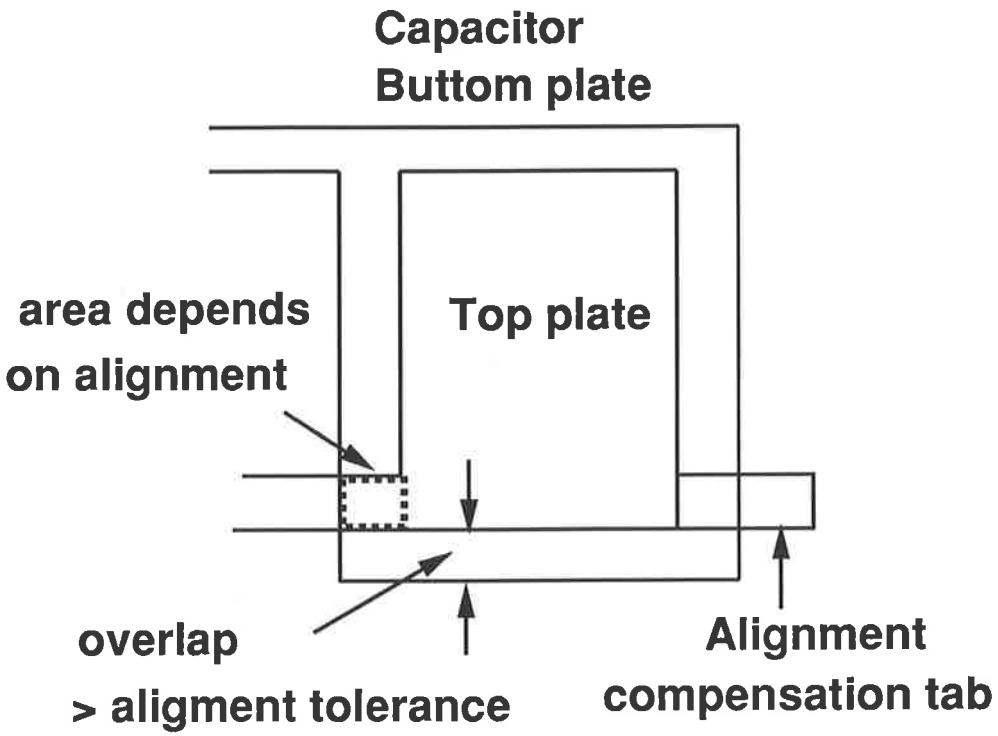


Figure 5.4: Compensation tab for interconnect

5.4.10 Compensation for interconnect

Figure 5.4 shows that the capacitance of a capacitor will be changed by changing the alignment, and a tab can included to compensate for the variation.

5.5 The layout of the ADC

The normal procedure of implementing a layout starts from a floor plan, then modules, composition cells and leaf cells [ROWS][ESHR2]. Leaf cells define the physical layout of the circuit. Composition cells contain only instances of other cells (leaf and composition). Different modules contain cells that are structurally unrelated. Following this procedure the circuit layout is designed and presented. However, this project covers the design of the analog part of an ADC, only the cells and modules involved are built.

5.5.1 The floor plan

First, the floor plan is designed (figure 5.5) based on the functional blocks shown below. The bonding pads are placed at the most convenient locations to connect to the related function blocks. A 40 lead Quad Flat Pack (QFP) is assumed to be the packing type, there are 20 pads. Due to process limitations the chip size should not exceed 5 mm by 5 mm, and a length to width ratio greater than 3 should be avoided [PML].

- four terminals for two reference voltage sources (one for the generation of 256 reference voltages, the other for the voltage shift used to bias the switches)
- one input signal terminal
- one voltage source for the bias of current sources for the comparators
- four pads for two power supplies, one for the logic and one for the analog circuit
- two clock input pads, one for the generation of internal switching clock and the other one for the timing control of this circuit
- eight output pads.

As per tradition and for safety reasons, the power pads are placed on the opposite side to ground pads.

5.5.2 The comparator modules

Following the floor plan, the modules for the comparators are designed. Displayed in figure 5.6, the DC buses are laid out first. The power rails and bias buses are placed in the middle, and ground (GND) is placed to separate them from the out most clock bus. For symmetry and easy access, the same buses are placed on both sides of the comparator modules as mirror images. To lay out the comparator module, symmetry is an important consideration, the comparator modules can be made pointing up with two branches of differential amplifier on two sides. This

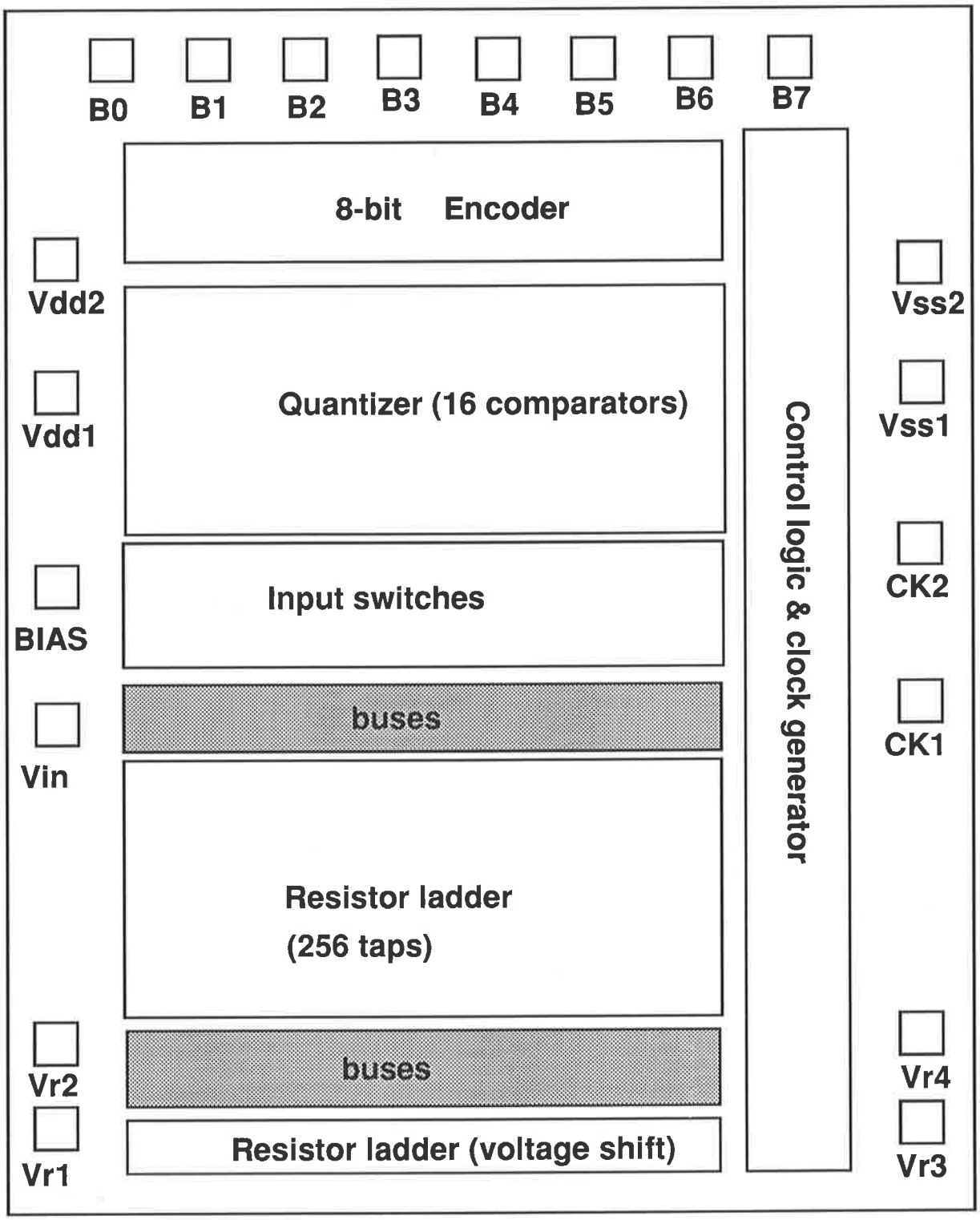


Figure 5.5: The floor plan of the ADC

will cause the signal buses to cross all the DC buses along the length of the three stage comparator. Moreover, the input switches can not be placed near the first stage, because it will create asymmetry to the differential amplifier. Therefore, a comparator whose center line is parallel to the DC buses is designed. The branches of the amplifiers are placed on the top and the bottom symmetrically.

Ideally, the resistor ladder should match the pitch of comparators and the reference voltages can be fed directly into each comparator without the vertical buses running between them. However, it will make the resistor ladder very large and waste a lot of precious chip area. Therefore, 16 lines to transfer the reference voltages plus one line for input signal are placed between the resistor ladder and the quantizer. To balance the capacitive load of each reference voltage line, each of the 16 lines must be the same length, whether the bus connects to the nearest comparator or the farthest.

5.5.3 Layout of the switch

The layout of the analog switch is quite straight forward, placing the desired transistors with minimum spacing between them. Four terminals must be provided for interconnection. The layout (figure 5.7) of this switch is not suitable for use at the ends of each 16 resistor chain. However, flipping the structure horizontally creates the switch for this need.

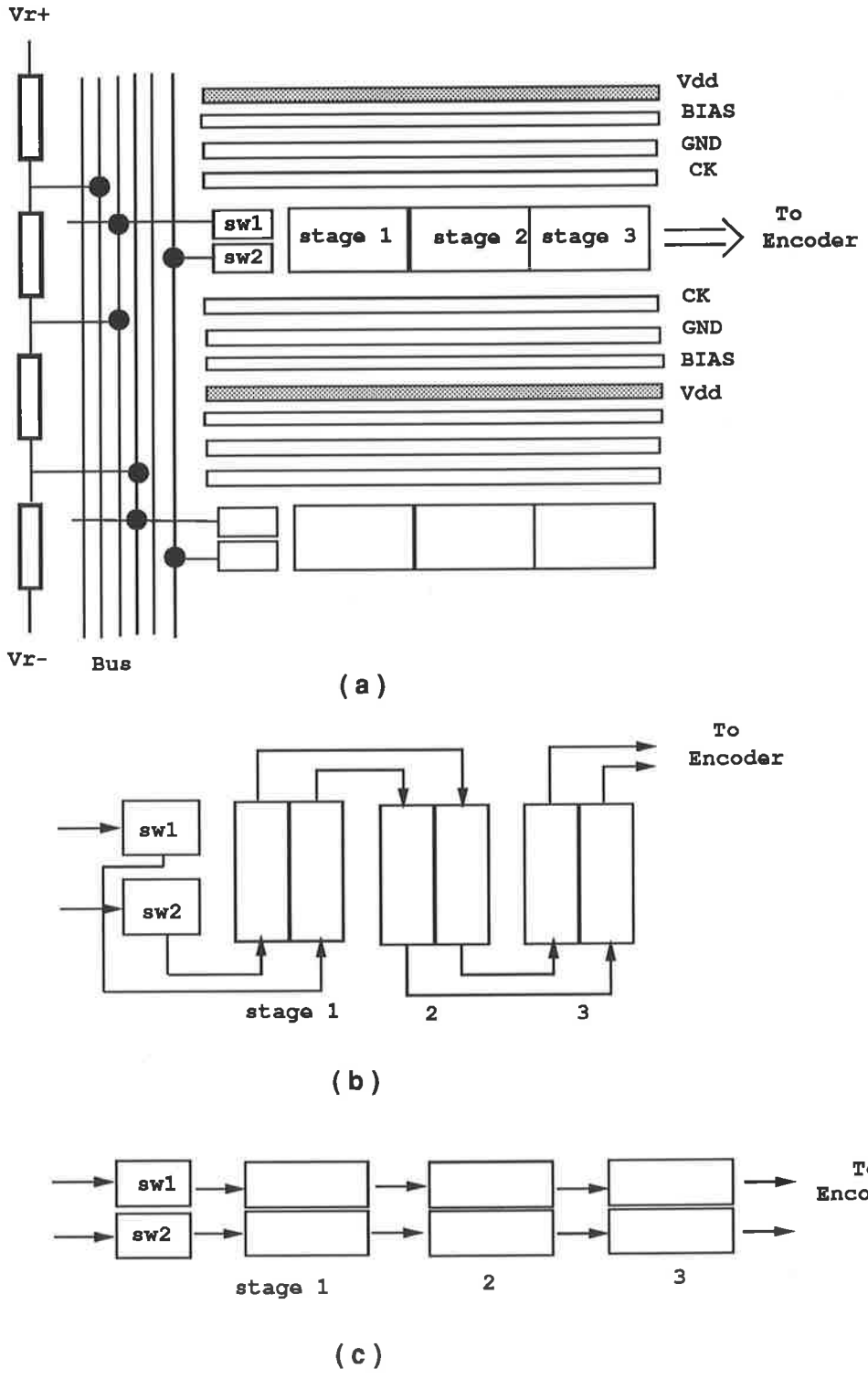


Figure 5.6: The comparator modules

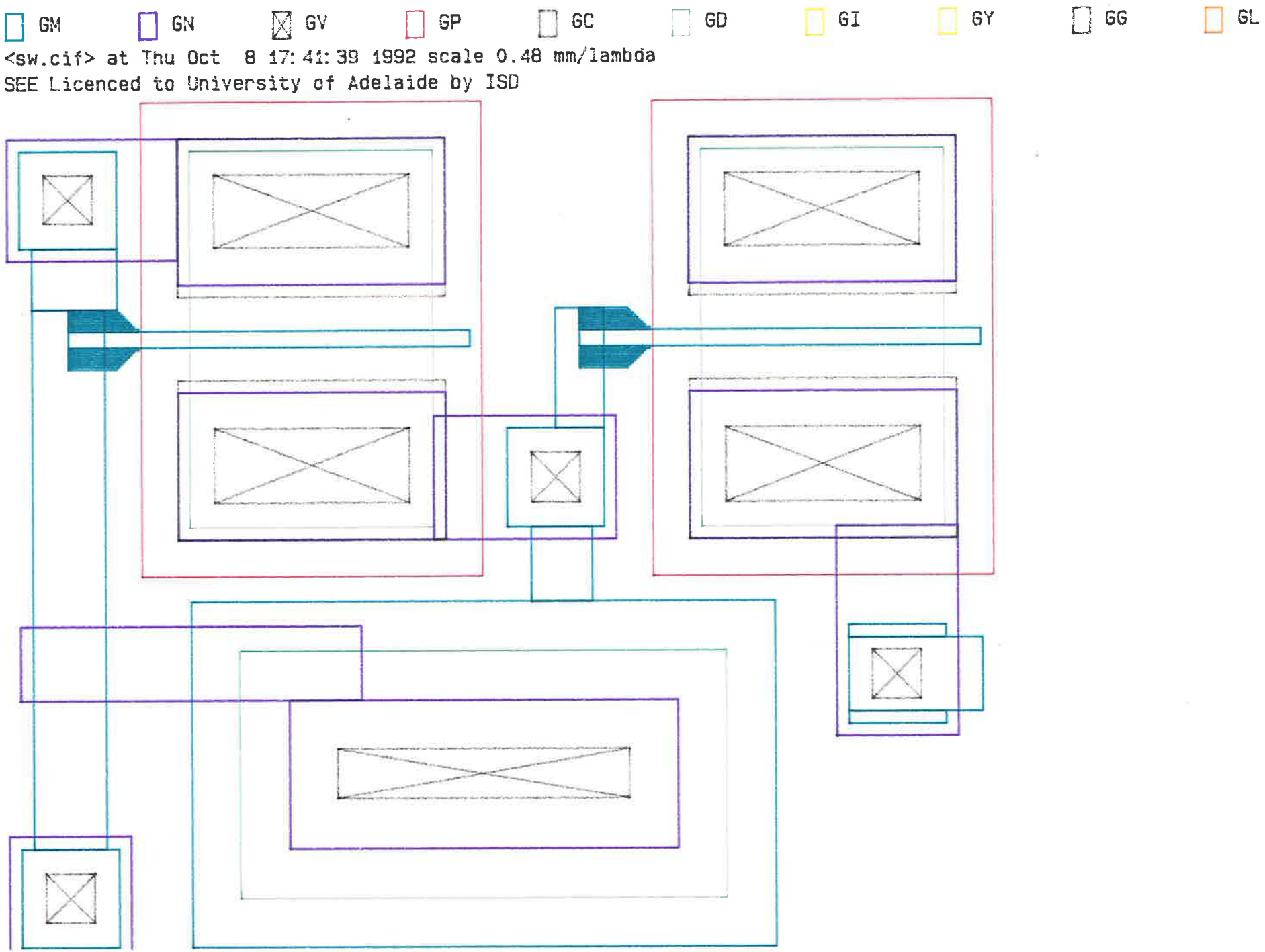
Material	Sheet resistance	Max. current density
diffusion	550 $\Omega/\square$	0.25 mA/μm
metal 1	0.075 $\Omega/\square$	3 mA/μm
metal 2	0.03 $\Omega/\square$	6 mA/μm

Table 5.1: The comparison of resistor materials

5.5.4 Layout of the resistor ladder

The resistor ladder generates the reference voltages for the ADC. The accuracy of the resistance between each tap is directly related to the linearity of the circuit. Therefore, the design of the ladder is extremely important in the design of the ADC. Before the layout is carried out, three materials which can be used to make resistors are prepared.

In order to offer very high speed operation, the total resistance of the 256 resistors is specified in the range of 10-30 *ohm*. Thus, every resistor is about 0.1 ohm. It is impractical to use a diffusion resistor in this scheme, since the ratio of the width over length will be about 5500 for each tap while it is 1.1 in metal 1 material and 3.3 in metal 2. When the full scan range (1 volt) is applied to the two ends of the ladder, 50 mA will flow through each resistor. If metal 1 is selected, the width of the resistor must be over 17 μm so not to exceed the limit of current density, and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the length will be close to 19 μm. In the case of using metal 2, the minimum width is 8.4 μm and the length is 28 μm. It is nearly impossible to build any shape other than a square where the width equals the length. A square shape is not suitable to build the ladder. This will be explained in the following text. Metal 2 interconnect is the candidate material for the resistor ladder.

Apart from the same value of resistance in each tap, main objective in the design of the resistor ladder is to keep the pattern of current flow in each tap of the resistor ladder identical. The variations in current patterns will cause a variation in voltage drop across each tap. Since 256 resistors placed in a straight line is impractical, and folding is necessary, this problem will be worsened at the end of the ladder or the corner where the resistor chain change direction. Figure 5.8 shows the different current patterns of a resistor ladder using simple rectangular or square shape resistors. An L shape resistor with equivalent vertical and horizontal arms can be used to form the ladder in which every resistor offers identical patterns of current and assures the minimization of the fluctuation of voltage drop no matter how the resistors are connected.

This structure was not used because a large area was wasted along the vertical arms of the L shape resistors. Instead, a modified L shaped resistor is designed based on this idea. Demonstrated in figure 5.9, the contacts of the resistor tap are placed in two asymmetrical positions. This offers an identical current pattern over the

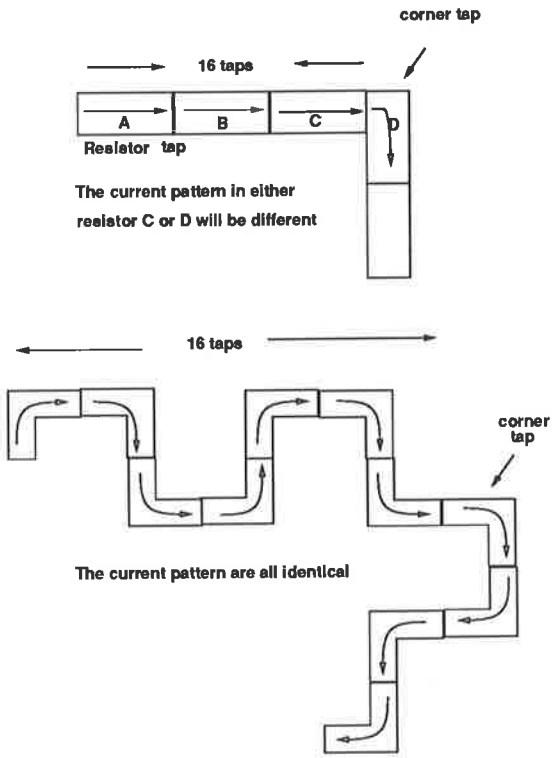

Figure 5.8: The different current pattern in the corner tap

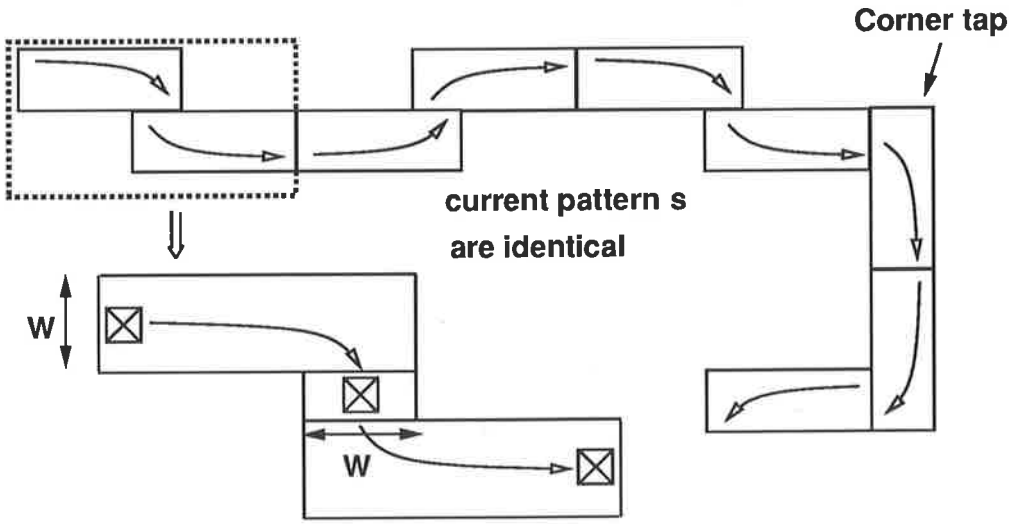

Figure 5.9: The modified L shape resistor tap

resistor ladder, including the corners. Since one analog switch will be attached to each resistor to transfer the voltage level to the quantizer, the actual length of each tap should match the length of the switch and so the distances of interconnects can be minimized.

As long as the resistance of the ladder is small, the absolute value is not an important issue. However, the uniformity along the full length of the resistor chain is very critical to the accuracy of the ADC. In the design of this resistor ladder, an unbroken piece of metal line is used and no contact resistance is involved in the current path. Contacts appear in the ladder only to pick up the voltage levels and no current will flow through the contacts. This assures minimum disturbance to the generated reference voltages.

Putting together the designs of the resistor ladder and the switches in which the sizes are matched, is shown in figure 5.10, a module of the resistor ladder. By duplicating this module eight times the resistor ladder and the control switches are in place. Then 16 buses for the coarse reference voltages and 16 for the fine are running from side to side of the ladder. Each row of 16 switches are connected to a signal line, which controls the selection of the row of taps, and a shifted voltage level to bias the switches. This shifted voltage is generated by a second resistor string. An important consideration in this part of the layout is to balance the RC constants of each tap. This constant is determined by the capacitive load of the buses used to transfer the reference voltages and the resistance of the switches. In order to minimise the difference of the RC value, the length of the 16 buses for the coarse reference voltages must be identical, and so are the lengths of the 16 lines for the fine reference voltage.

At the ends of each 16 taps, the space is not enough for the switches to be placed in line with the other 14. Due to the orientation of the resistors connected, two switches must be placed in different direction and the structure of the switches is made by flipping the original design horizontally. The extra length of the lines must be as small as possible.

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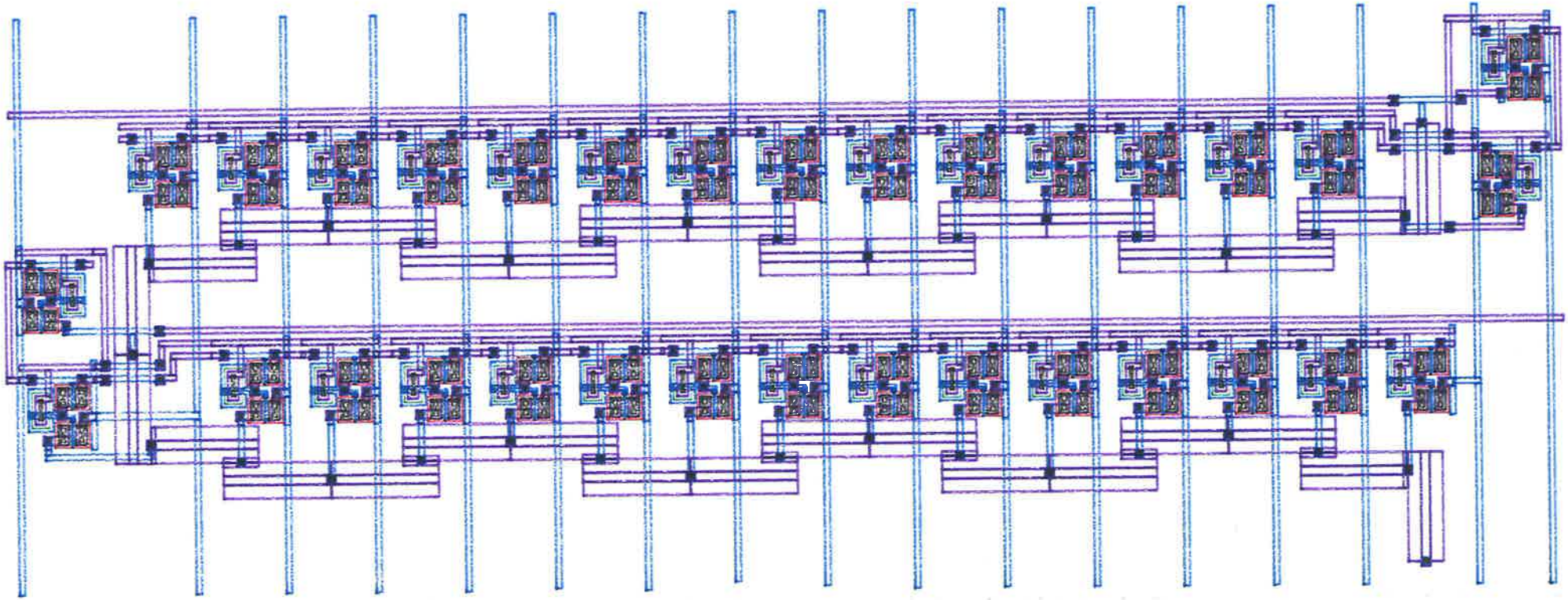

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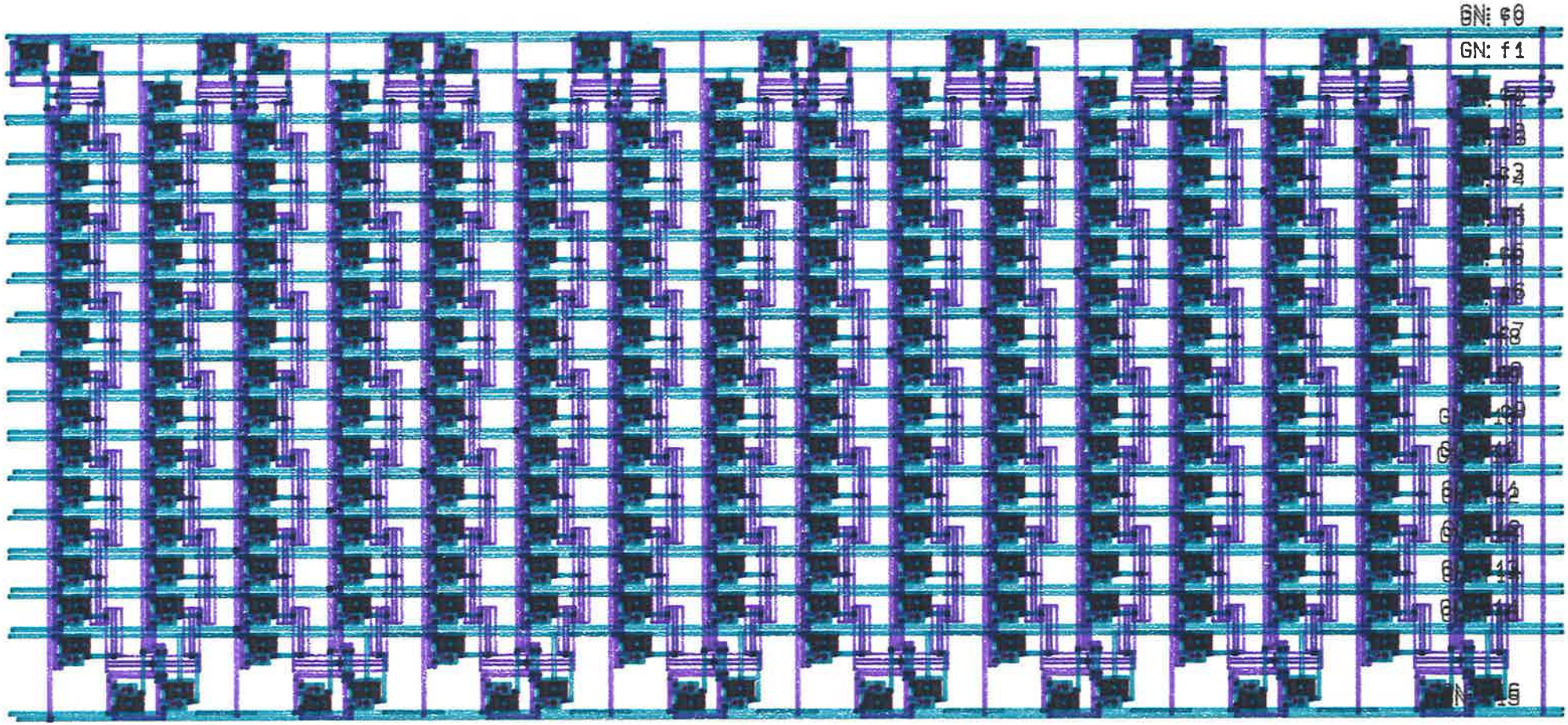

5.6 Comparator layout

The layout of the comparator is a critical part of the circuit. A totally symmetrical structure is necessary to ensure the accuracy of operation. Based on the considerations discussed in the early part of this chapter, devices are placed in close proximity to their counterparts in the comparator. Moreover, due to gate series resistance, very long gates are not used and finger transistors are used instead. Two current sources of the source followers and a current source of the differential amplifier are separated by the feedback switches. The width of the input capacitors can be adjusted for the best fit, as long as the capacitors are not too long. All the devices are placed symmetrically to the current sources and heat generators. The layout of the amplifier and the source follower are shown in figure 5.12 and figure 5.13.

Four switches controlled by three clock lines are required to manipulate the reference voltages and the input signal fed into the comparator. Two switches are connected to the coarse reference voltage and are controlled by a clock signal while the other switches are connected to the fine reference voltage and input signal and controlled by two separated clock buses. Again for symmetry reasons the two clock lines are used to pass the clock signal from the input control switches to the feedback switches in the comparator, though they transfer the same signal. The circuit needs only one source follower attached to the input path to provide the voltage shift for the switches in all comparators for the selection of input signal.

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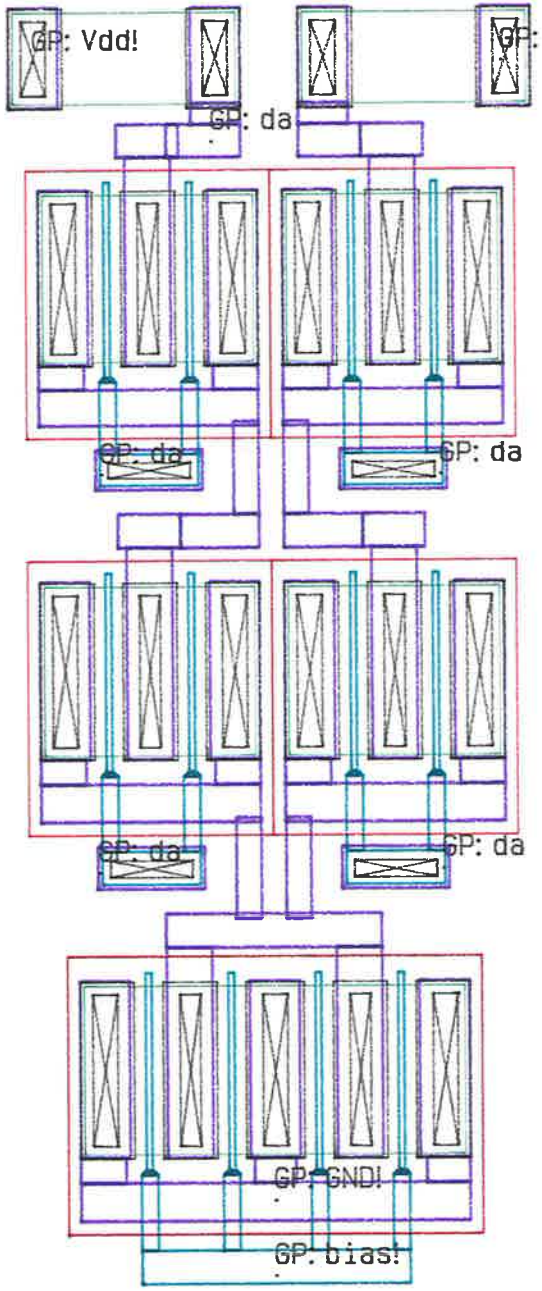

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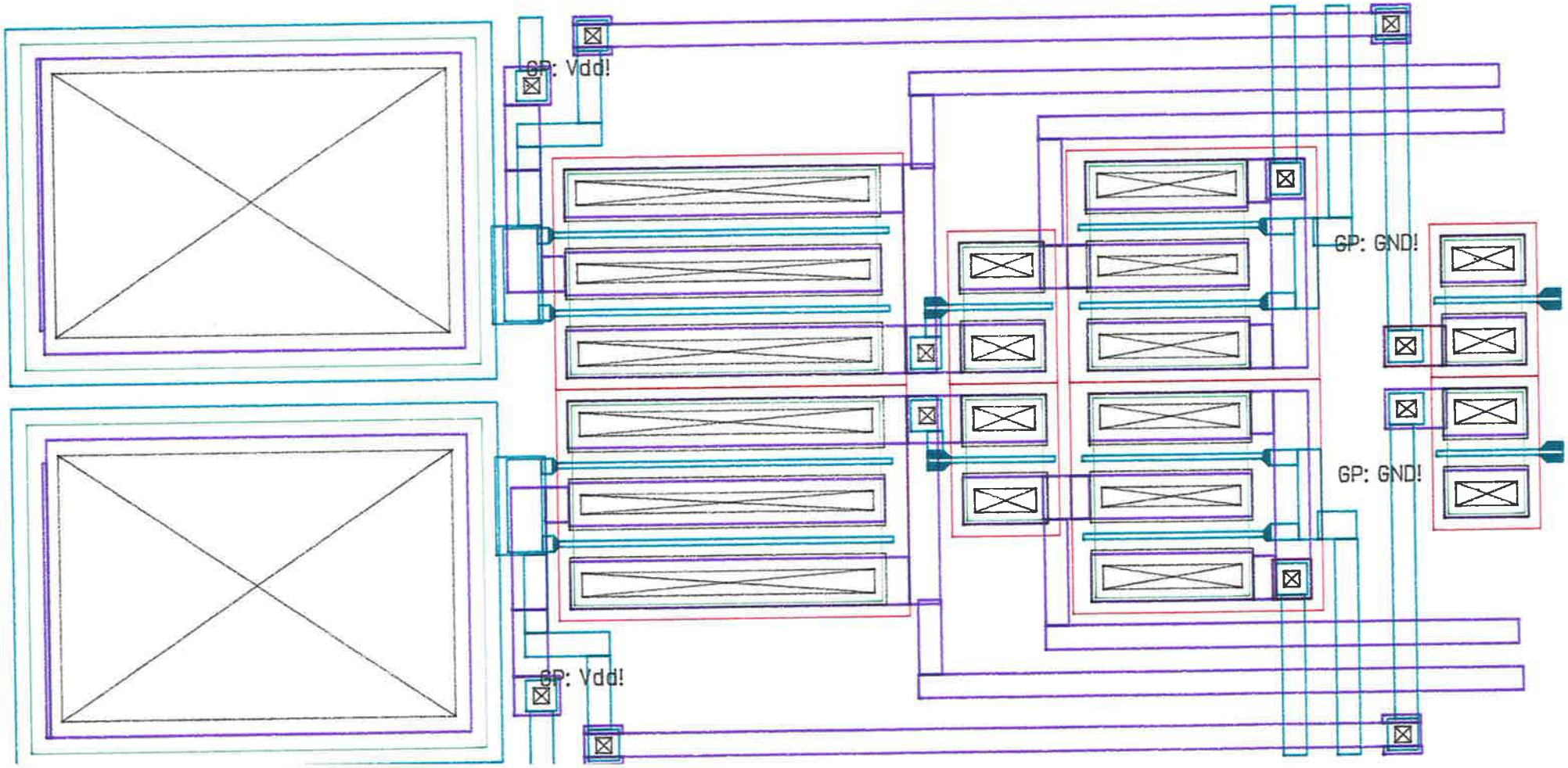

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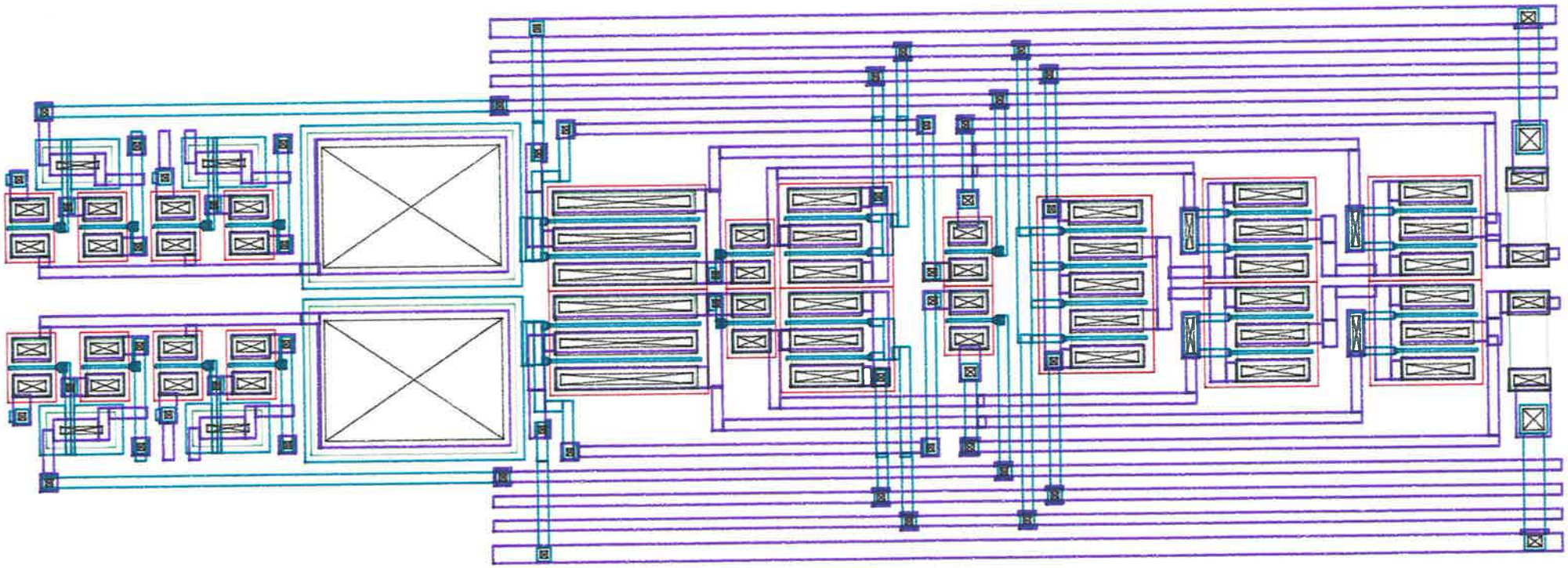

5.7 The layout of a bit slice and a test chip

The last part of the layout work is to duplicate the the comparator twice and connect them in series to form a three stage comparator. Displayed in figure 5.15 is the complete comparator circuit with four switches in front of it and a source follower to provide a shifted voltage for the switch of the input signal. This layout is shown with bonding pads. It can be fabricated as a vehicle to measure the performance of this design. In order to facilitate the test and monitor the response at each node, a single stage amplifier is also laid out with and without the switches in front of it.

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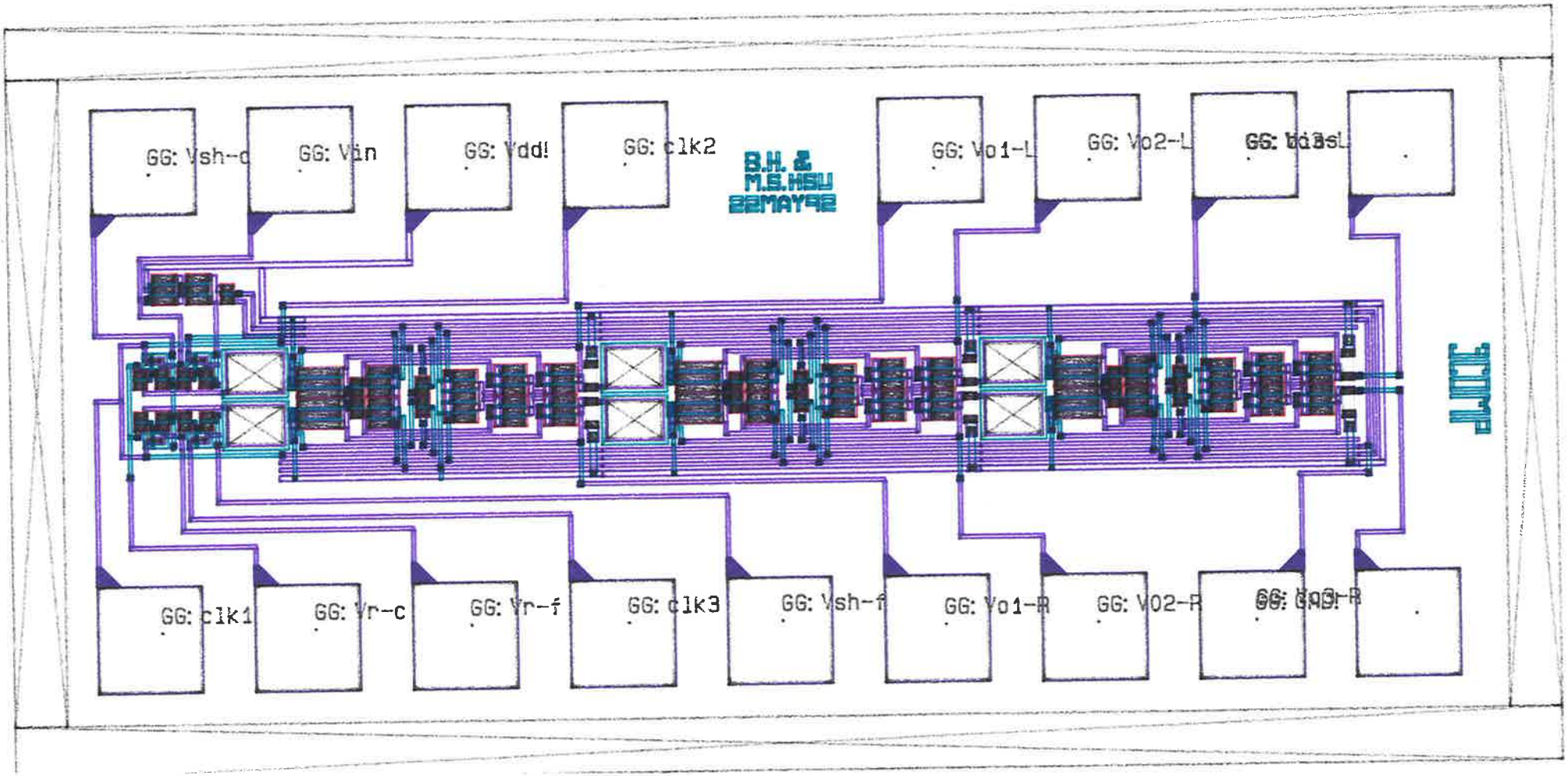

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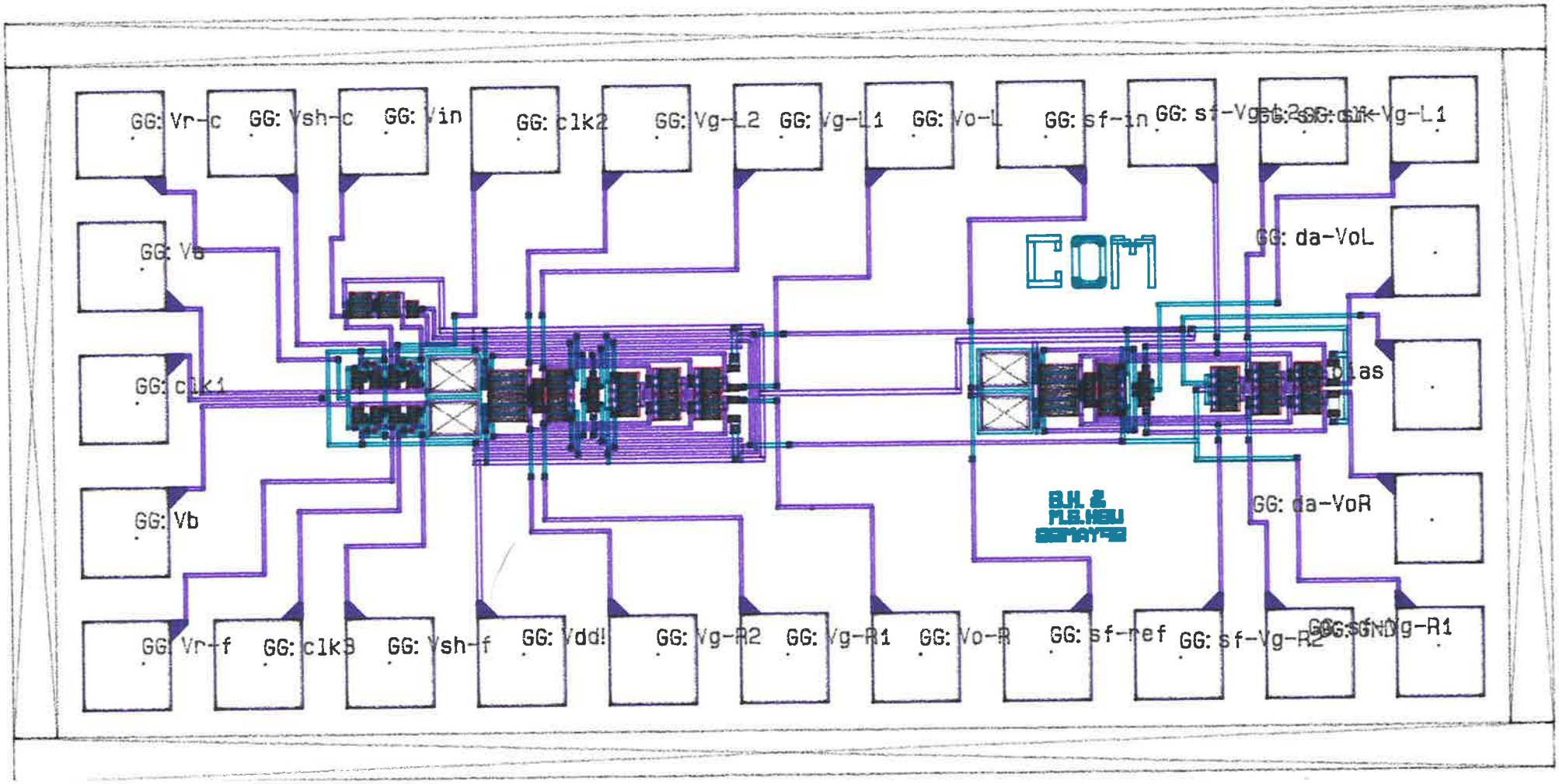

Chapter 6

Discussion and future work

6.1 The error sources in the design

The simulation of the ADC circuit shows a satisfactory result. However, the study so far assumes no disturbances to the currents, voltages, resistances and capacitances in the circuit. In real operation, the performance of the devices may vary by the operating conditions, fabrication process variation, and age. All of these factors will cause degradation to the accuracy of the circuit. In this chapter, the possible sources which may produce accuracy problems will be discussed.

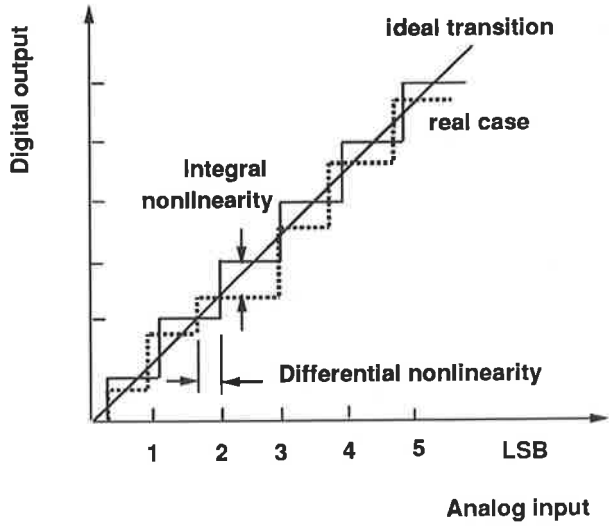

Figure 6.1: The definition of nonlinearity

In the study of accuracy, "nonlinearity" is the indicator used to show the extent of the inaccuracy of an ADC. Nonlinearity can be divided into two components, defined as: [ALLEN2]

- **differential nonlinearity** - the variation of the analog value between adjacent pairs of digital numbers over the full range of digital output.

- **integral nonlinearity** - the maximum deviation of the output digital codes from a straight line drawn through zero and full scale (figure 6.1).

Nonlinearity is the combined result of almost all kinds of error, including hysteresis, offset voltage, noise, mismatch, power supply fluctuation, reference voltage inaccuracy, aperture error ...etc. Errors like $1/f$ and thermal noise which are very small

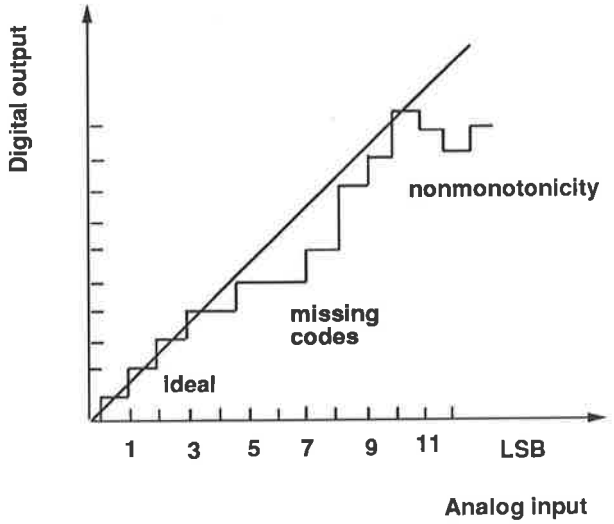

Figure 6.2: Missing codes and nonmonotonicity

compared to 1 LSB will not be discussed here. When nonlinearity exceeds $\frac{1}{2}$LSB, missing codes or nonmonotonicity will occur and a false digital output word will be given (figure 6.2). Therefore all possible errors should be restricted to within this limit.

6.1.1 Hysteresis and offset voltage

In the design, comparator offset is mostly nulled by the feedback switches during the self calibration period, only a very small amount of residual offset will remain. The effects of unbalanced offsets are isolated by the coupling capacitors between comparator stages. The differential output voltage produced by the residual offsets at the last stage is about 20 mV and is equivalent to 0.2 mV of input offset when

total gain is 100. Therefore the offset will not cause an accuracy problem.

Hysteresis in the differential amplifier of the comparators is reduced to a negligible level by the use of bootstrapping configuration which restricts the variation of V_{ds}. In the source followers of the comparators, hysteresis still exists. However, the hysteresis is proportional to the V_{ds} variation which is not greater than the specified full scale range (1V) in this circuit. As a reference, the biased cascoded configuration in [DUCO2] (with PML technology) offers the same order of V_{ds} swing as our ADC and about 10 mV of hysteresis was measured. Therefore, the hysteresis in our design is expected to be in 10 mV range.

The power supply noise is cancelled by the differential structure of the comparator. However, a power supply fluctuation which is greater than 1V will cause insufficient V_{ds} bias to the current source of the comparator which is originally biased to 1.5V. Consequently, the current and voltage gain will degrade.

One major reason for reference voltage error is the inaccuracy of the applied reference voltage source. This will cause an output offset between the ideal and actual transition levels. The mismatch of the effective resistance of the resistor tap will cause a variation of the voltage difference between two adjacent transition levels over the full input range. This eventually causes the differential nonlinearity. The mismatch of the effective tap resistance can be introduced by process variation and

different current patterns in each tap. Since the layout produced identical current patterns in every tap, we assume process variation is the main contributor to the error. Based on PML's statistics, the variation metal line resistance is less than 5%. It is too small to generate problem.

A major cause of aperture error is clock jitter. This problem is of great concern in high speed ADCs, especially for those using a flash architecture. A sample and hold (S/H) circuit is an effective solution to this problem although the offset of the S/H will increase the nonlinearity, however, S/H will not be discussed in detail.

The voltages sensed at the input and reference terminals will be affected by the RC constant of the buses and the input coupling capacitors. In addition to the parasitic capacitances of the bus which is made identical for each reference voltage bus, the channel resistance of the switch is another main factor of the RC constant. In the resistor ladder, every 16 switches in a row uses a shifted voltage from the first tap to bias the gates of the switching transistors. Meanwhile, their source ends are connected to 16 taps separately. Therefore the difference of the source voltage between the first and the last switch in the row is 15 LSB (60 mV). This means the V_{gs} of the switches has a voltage difference of 60 mV plus the threshold variation. Consequently, the speed of the resistor ladder is determined by the by the least biased switch. However, this affects only the time required to recharge the input capacitors which is not of much concern assuming the charge stored in the

capacitors are conserved during operation.

The process variation may cause a 5% difference in the values between the two input capacitors. This will induce the same ratio of voltage difference between the input and the reference side of the comparator and induces an offset to the transition levels. Other normal error sources such as glitch and clock feedthrough are suppressed by the differential structure and the small switches used.

6.2 Future work

In this research we do not cover the design of a S/H circuit, the logic and clock generator. Thus, to complete the full ADC design, they must be included. Furthermore, the simulation parameters and the model of the depletion MESFET was not available at the time the design was implemented. Therefore, the advantages of depletion MESFET over enhancement MESFET was not utilized in the design. It is expected to improve the performance of the ADC in the future work. Here are some hints when this design will be carried out further.

6.2.1 Error correction algorithm

An error correction algorithm can be used in this design to increase the accuracy and reduce the coarse comparison time. In the ADC circuit, 16 comparators are used to perform the quantization. The level difference between any two coarse reference voltages is equivalent to 16 LSB. Assuming $V_{in} > V_k$ and V_k is equivalent to the digital word 1110 0000, the circuit will seek for a conclusion from the range 1110 0000 to 1110 1111 in the coarse comparison. When V_{in} is sensed to be less than 0.5 LSB above V_k at the end of sampling period and the comparator is unable to resolve the difference between the two, an error result saying $V_{in} < V_k$ may be concluded from the coarse comparison. Therefore, the maximum result of the fine comparison will be 1101 1111, one LSB away from what it should be.

If 18 comparators instead of 16 are used in the circuit, and all are used for fine comparison, two extra comparators will cover one LSB above and one below the selected range for fine comparison. When the problem occurs at coarse comparison, the result of fine comparison will still be 1110 0000 and the error is avoided. Naturally, the logic involved will be more complex. In the case of including many more comparators, a wider range of error can be corrected in the fine comparison. This means a larger error can be tolerated in coarse comparison so the circuit does not need to wait until the sampled signal has settled before the fine comparison can be started. So the time for coarse comparison can be reduced.

6.3 The elimination of self calibration

Since consumes about a half of the operation time, the circuit should be able to work at twice the speed if the self calibration time can be eliminated. This can possibly achieved through three ways. The first, to cancel the performance of self calibration. Due to the use of coupling capacitors and low voltage gain in each of the three stages, the initial output differential voltage is much smaller than the output swing, and the coupling capacitors isolated the offset voltage in each stage. So the offset is not a major concern in the operation. However, the charges in the input capacitors needed to be refreshed periodically. Therefore, a modified design without feedback switch but with recharging function can possibly achieve double operating speed.

The second way of doing this is to use another set of 16 comparators. When one set is working on the comparison, the other set can do the self calibration and then rotate. Because the charge loss from the input capacitors is very small, if the gate-source voltage is kept below 0.4V, the self calibration and recharging can be performed in every two or more operation cycles. This gives more time for the spare quantizer to complete the self calibration and be ready for its next mission and allow higher speed at the cost of a larger chip size and higher power consumption.

The last proposal is to use a cyclic autozeroing scheme[MASS]. This method allows

the 16 comparators to perform the self calibration one after the other while they are in operation with a 17 LSB maximum worst case error which occurs when V_{in} is above V_k within 0.5 LSB and the cyclic autozeroing is taking place at the $(k-1)$th comparator. The result of the coarse comparison may say $V_{in} > V_{k-2}$, and the final result is $V_{in} = V_{k-1}$ - 1 LSB, however the overall accuracy of this scheme should be estimated by using statistics.

6.3.1 The use of a depletion mode MESFET

The advantages of depletion MESFET over an enhancement MESFET are mainly the higher transconductance, g_m and higher driving capability while the larger C_{gs} is a drawback. A comparison of the basic electrical characteristics of the two is given [PML].

For $V_{ds} = 2$V, $V_{gs} = 0.4$V, $W = 1000$ μm

EMESFET $I_{dss} = 60$ mA, $I_{ds} = 10.8$ mA, $C_{gs} = 1087$ fF, $C_{gd} = 185$ fF, $g_m = 87$ mS

DMESFET $I_{dss} = 200$ mA, $I_{ds} = 26$ mA, $C_{gs} = 1739$ fF, $C_{gd} = 119$ fF, $g_m = 222$ mS

The application of DMESFETs in the design will introduce substantial advantages

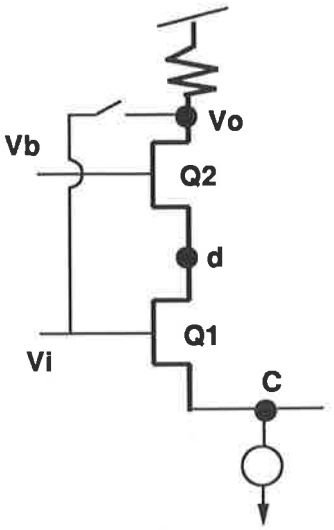

Figure 6.3: The restricted input range

to the performance;

1) Speed improvement. If DMESFETs are used in the comparator with the same power and current the channel width W can be reduced by a factor of 3.3 because of the I_{dss}, but the capacitance of $C_{gs} + C_{gd}$ per unit length is also magnified by 1.5. So the capacitance of the DMESFET will be 2.2 times smaller than an EMESFET, and so is the response time.

2) With the use of DMESFETs in the differential amplifiers, the source followers may be eliminated. In the current design, if the output nodes are connected to the input gates without buffers during the self calibration, the input dynamic range will be severely restricted. This is explained in the following discussion.

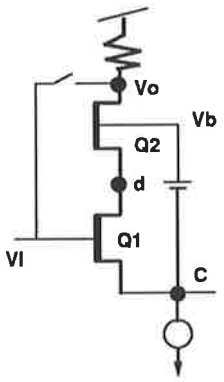

Figure 6.4: Modified circuit with DMESFET

Initially $V_o - V_d \geq V_b - V_d - V_t$ (figure 6.3), so $V_o \geq V_b - V_t$ must be satisfied to saturate Q2. Thus $V_o + V_t \geq V_b$. Also $V_b \geq V_d + V_t$ is needed to turn on Q2 and $V_d \geq V_o - V_t$ is required to saturate Q1. So $V_d + V_t \geq V_o$ and $V_b \geq V_d + V_t \geq V_o$. Consequently, the voltage level at the initial state is set to $V_o + V_t \geq V_b \geq V_o \geq V_d \geq V_o - V_t$. Then if a positive $2\Delta V$ is applied, V_d will go down by ΔV as explained on page 95, and V_o will go down by $\Delta V \cdot Av$. So $V_b - V_o \geq V_t + \Delta V \cdot Av$ which is limited to 0.7V by the Schottky gate junction. Thus, $V_o - \Delta V \cdot Av > V_d - \Delta V$ and $V_o - V_d > -\Delta V(Av+1) > -V_t$. Therefore, $\Delta V < \frac{V_t}{Av+1}$, the input is limited to very small range. To prevent this problem, source followers are included to provide level shift.

With the use of DMESFETs, due to the negative V_t this problem will not occur, so the output can be connected directly to the input for self calibration. Moreover, the bias voltage of the bootstrapping can be a fixed voltage above the common mode level. The modified design is illustrated in figure 6.4.

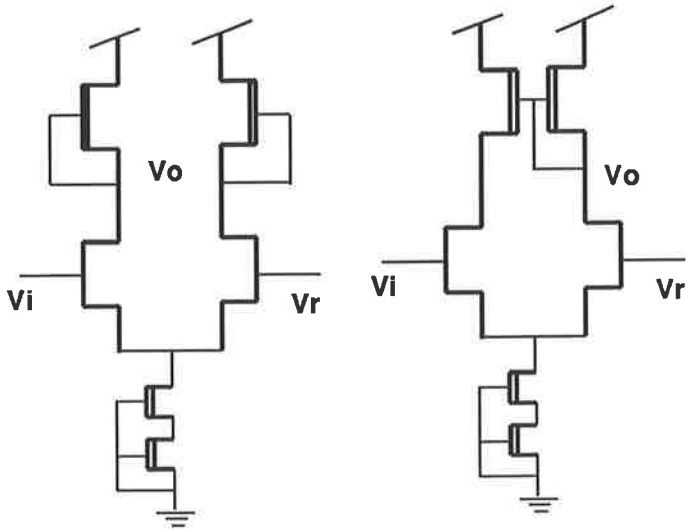

Figure 6.5: The use of DMESFETs as loads and current sources

3) With DMESFETs in the current source of the source followers and amplifiers a self bootstrapping configuration can be used to eliminate the bias voltage and the associated fluctuation (figure 6.5). DMESFETs can also be used as active loads to increase gain [TEMES].

6.4 Conclusion

In this research, the design techniques for silicon ADCs are studied. The achievable improvements and the limitations of scaling silicon MOS devices are investigated

to understand their performance in extreme conditions. Due to the physical limitations, silicon devices are unable to provide high speed operation at low power consumption with the current process technology. In contrast, GaAs is attracting more attention recently for its superior characteristics and the potential in the application of high speed conversions.

Designs of an ADC operating in the GHz region have been reported, yet the hysteresis and the offset associated with GaAs devices restricts the accuracy of the circuits. The design of an 8 bit ADC in this research introduces a simple comparator structure in which a reference sampling scheme is used to reduce the time needed for input sampling, a bootstrapping structure is used for hysteresis reduction, feedback switches are used to perform the self calibration and refreshing the input capacitors and a differential structure is used to suppress common mode noise.

The simulation results show that this circuit can offer 8 bit resolution ideally at about 700 MHz with only 256 mW power dissipation for the quantizer. However, the temperature effect is not simulated and the hysteresis effect needs to be further investigated and reduced. Further improvement in speed and simplicity can be achieved by using DMESFETs. Also a measurement of the realised chip of this circuit will help to understand the actual performance and the shortcomings of the design. A genuine 8 bit, 1 GHz ADC should not be far away.

Appendix A

Analysis of the self calibration time

Due to the unavailability of a high voltage gain, the comparator is designed using cascaded stages and each stage is connected through a capacitive coupling. In classical architectures, the speed limitation during the self calibration phase occurs only in the first stage. When using a differential comparator as is illustrated in figure A.1, both channels behave in the same manner.

Figure A.2 shows a simplified model of a half section of the first stage with its input

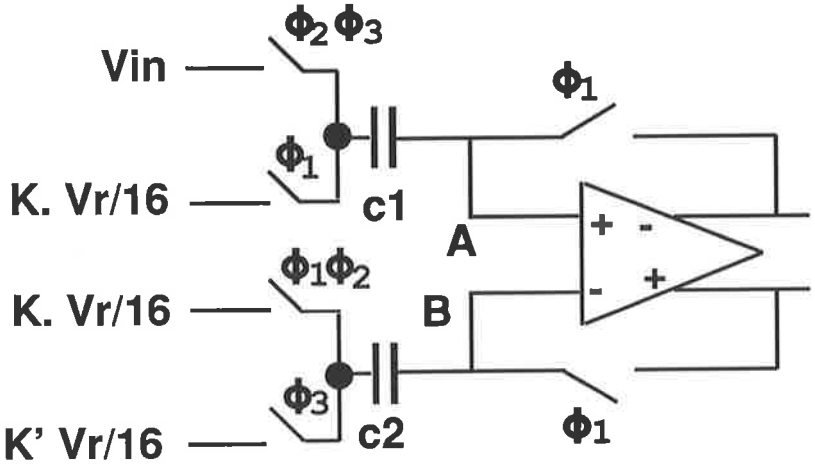

Figure A.1: The reference sampling structure

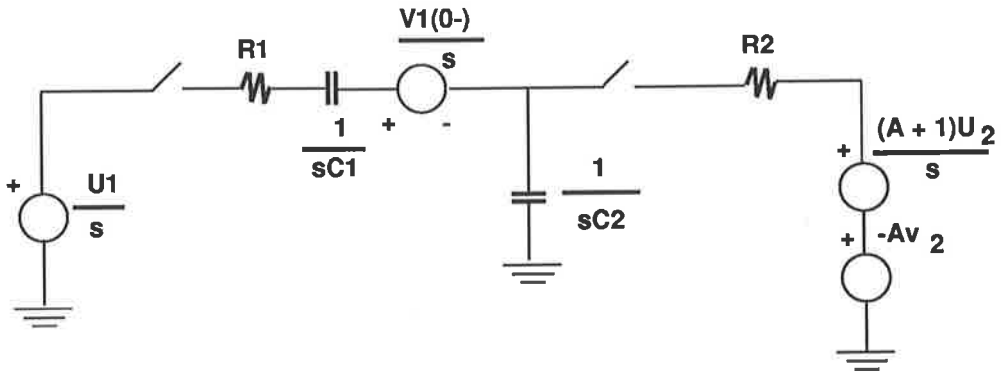

Figure A.2: Simplified model of one comparator channel

switch connected to the reference voltage $U-1$. C_1 is the sampling capacitance, C_2 is the comparator input capacitance including the Miller capacitance. R_1 is the sum of the input switch resistance and the output resistance of the resistive ladder. R_2 is the resistance of the feedback switch, which also includes the output resistance of the amplifier stage. The DC characteristics of the stage which is assumed to be similar to that of an inverter with threshold voltage U_2, is given by:

$$V_{out}(t) = A \cdot (U_2 - V_2(t)) + U_2 = (A+1) \cdot U_2 - A \cdot V_2(t) \tag{A.1}$$

When this stage is connected in closed loop, its input and output converge toward the threshold voltage U_2. In the Laplace domain, when the switch is closed the constant term $(A+1) \cdot U_2$ in equation A.1 is divided by s. In figure A.2, $v_1(0-)$ represents the initial voltage across capacitor C_1. The voltage v_2 across capacitor C_2 is given by:

$$v_2(s) = \frac{(1+sR_1C_1) \cdot U_2 + sR_2^*C_1(U_1 - v_1(0-))}{s \cdot ((1+sR_1C_1) \cdot (1+sR_2^*C_2) + sR_2^*C_1)} \tag{A.2}$$

where $R_2^* = \frac{R_2}{A+1}$

Usually, C_1 is much larger than C_2, and hence $v_2(s)$ may be rewritten as:

$$v_2(s) = \frac{(1+sR_1C_1) \cdot U_2 + sR_2^*C_1 \cdot (U_1 - v_1(0-))}{s \cdot (1+s(R_1//R_2^*)C_2) \cdot (1+s(R_1+R_2^*)C_1)} \tag{A.3}$$

where $R_1//R_2^*$ is the value of parallelled R_1 and R_2^*.

The final value of v_2 with increasing time is U_2:

$$\lim_{t\to\infty} v_2(t) = \lim_{s\to 0} s \cdot v_2(s) = U_2$$

At the beginning of the operations, C_1 is discharged and the slowest time constant is $(R_1 + R_2^*) \cdot C_1$. Consequently, the first self calibration is slow, but it occurs only once at the initial stage. When the voltage across C_1 is $(U_1 - U_2)$, it may be assumed constant. Then $v_2(s)$ is given by:

$$v_2(s) = \frac{1 + s(R_1 + R_2^*)C_1}{s(1 + s(R_1//R_2^*)C_2 \cdot (1 + s(R_1 + R_2^*)C_1)} \cdot U_2 = \frac{1}{s \cdot (1 + s(R_1//R_2^*)C_2)} \cdot U_2 \tag{A.4}$$

and we see that the only time constant is $(R_1//R_2^*) \cdot C_2$. Usually, the gain per stage is less than 10, and $(R_1//R_2^*) \cdot C_1$ may be approximated to $R_1 \cdot C_2$

Appendix B

Low frequency analysis of the source follower

The circuit of the source follower can be drawn as the small signal equivalent circuit in figure B.1. Then

$$V_{o2} \cdot sC2 + V_{o2} \cdot G_o = (V_{o1} - V_{o2}) \cdot G_b G_m \cdot (V_i - V_{o1}) = V_{o1} \cdot G_d + (V_{o1} - V_{o2}) \cdot G_b + V_{o1} \cdot sC1 \tag{B.1}$$

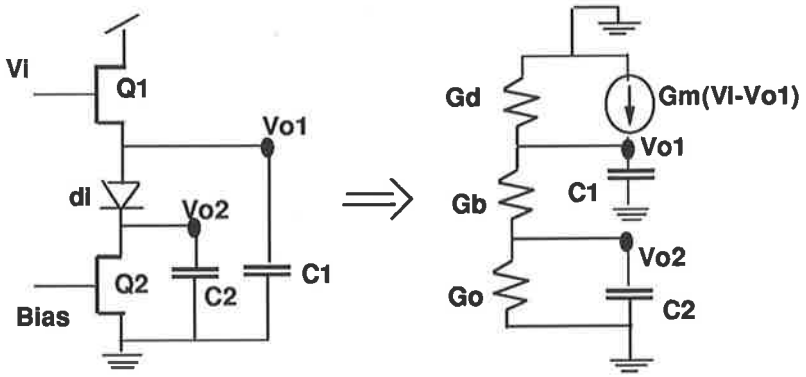

Figure B.1: The small signal equivalent circuit

where

G_m is the transconductance of Q1

G_d is the output conductance of Q1

G_b is the output conductance of the diode di

G_o is the output conductance of the current source Q2

The equation B.1 can be transformed into

$$V_{o2} = \frac{V_{o1} \cdot G_b}{G_b + G_d + sC2} = \frac{V_{o1}}{1 + \frac{1}{G_b} \cdot (G_o + sC2)} \tag{B.2}$$

Applied equation B.2 to equation B.1, we can have

$$V_{o1} \cdot (G_d + G_b + G_m - \frac{G_b}{1 + \frac{1}{G_b} \cdot (G_o + sC1)} = V_i \cdot G_m \tag{B.3}$$

then

$$V_o1 = \frac{G_m \cdot Vi}{Gd + G_m + Gb - Gb \cdot 11 + \frac{Go+sC1}{Gb}} \tag{B.4}$$

Usually, G_o is small when the transistor operates in saturation region, and Gb can be made much greater than Go by imposing a large current. Therefore, $G_b \gg G_o + sC2$ is valid at mid or low frequency or low output capacitive load and $V_{o1} = V_{o2}$ can be achieved with very little tolerance. In our design sC2 is very small, so this condition can be presumed true, and the source follower is treated as a typical source follower without the diode. So, the gain of this stage is

$$Av_{in} = \frac{V_{o1}}{V_i} = \frac{G_m}{G_m + G_d} \tag{B.5}$$

B.1 Differential amplifier low frequency analysis

A basic differential amplifier connects the sources of two inverters together (figure B.2.a) and each one responds to half of the input voltage in opposite direction. If we neglect the fluctuation of the common mode level at node C, the amplifier can be treated as an inverter with the input equal to $V_i - V_r$ (figure B.2.b).

Applying this argument to the designed amplifier, the bootstrapping structure can be simplified as in figure B.3.a. For further analysis, the simplified circuit is redrawn as a small signal equivalent circuit as shown in figure B.3.b.

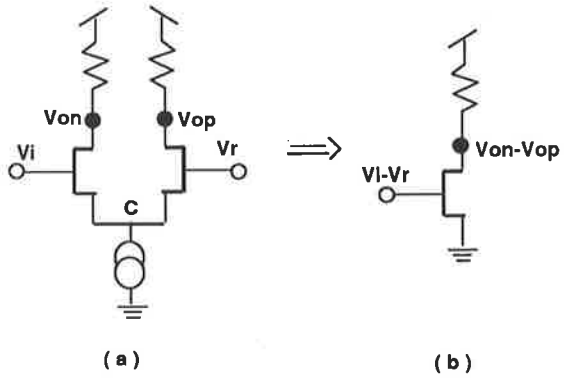

Figure B.2: The simplified circuit of the comparator

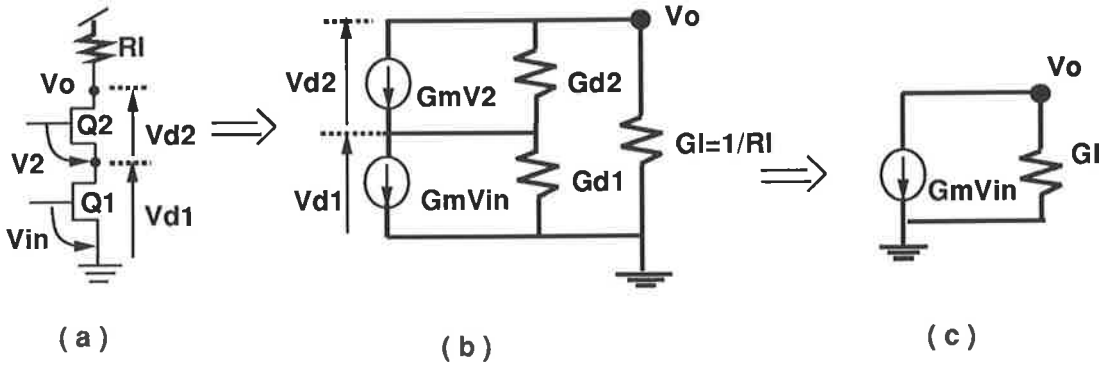

Figure B.3: Simplified equivalent circuit of the differential amplifier

Then

$$G_{m1} \cdot V_{in} + G_{d1} \cdot V_{d1} = G_{m2} \cdot V_2 + G_{d2} \cdot V_{d2} = -G_l \cdot V_o \tag{B.6}$$

where

G_{m1} and G_{m2} are the transconductances of Q1 and Q2 respectively

G_{d1} and G_{d2} are the output conductances of Q1 and Q2 respectively

and

$$Vdi + V_{d2} = V_o$$

$$V_{in} = V_2 + V_{d1}$$

so

$$V_o = V_{in} - V_2 + V_{d2} \tag{B.7}$$

From equation B.6 we have

$$G_{m1} \cdot V_2 + G_{d2}(V_2 - V_{in} + V_o) = -G_l \cdot V_o G_{m1} \cdot V_{in} + G_{d1}(V_{in} - V_2) = -G_l \cdot V_o \tag{B.8}$$

solving equation B.8 we get

$$V_2 = \frac{(G_{m1} + G_{d1})V_{in} + G_l \cdot V_o}{G_{d1}} \tag{B.9}$$

Since Q1 and Q2 are chosen identical, $G_{m1} = G_{m2} = G_m$. Rearranging Eq. B.8 and applying above result to it yields

$$(G_m + G_{d2})V_2 - G_{d2} \cdot V_{in} + (G_{d2} + G_l)V_o = 0 \tag{B.10}$$

$$\frac{(G_m + G_{d2})[(G_m + G_{d1})V_{in} + G_l \cdot V_o]}{G_{d1}} - G_{d2} \cdot V_{in} + (G_{d2} + G_l)V_o = 0 \tag{B.11}$$

then we have

$$(G_m \cdot G_m + G_m \cdot G_{d1} + G_m \cdot G_{d2})V_{in} + (G_m \cdot G_l + G_{d2} \cdot G_l + G_{d1} \cdot G_{d2} + G_{d1} \cdot G_l)V_o = 0 \tag{B.12}$$

Consequently, the voltage gain is given by

$$\frac{V_o}{V_{in}} = -\frac{G_m(G_m + G_{d1} + G_{d2})}{G_l(G_m + G_{d1} + G_{d2} + \frac{G_{d1} \cdot G_{d2}}{G_l})} \tag{B.13}$$

Since it is easy to make $G_m + G_{d1} + G_{d2} \gg (G_{d1} \cdot G_{d2})/G_l$. Therefore, the gain of this amplifier is expressed as

$$\frac{V_o}{V_{in}} = -\frac{G_m}{G_l} \tag{B.14}$$

Finally the equivalent circuit of the differential amplifier can be further simplified as an ideal inverter with no output conductance G_d (figure B.3.c).

Appendix C

High frequency analysis of the comparator

Following the results obtained in Appendix B, the simplified equivalent circuits of the source follower and the amplifier are used in the analysis of high frequency behaviour of the comparator. At high frequency the effects of the stray capacitances, which are ignored in low frequency analysis, must be included. Thus, the small signal equivalent circuit is redrawn in figure C.1.

where

R_s is the input resistance

C_{gdf} is the gate to drain capacitance of Qf

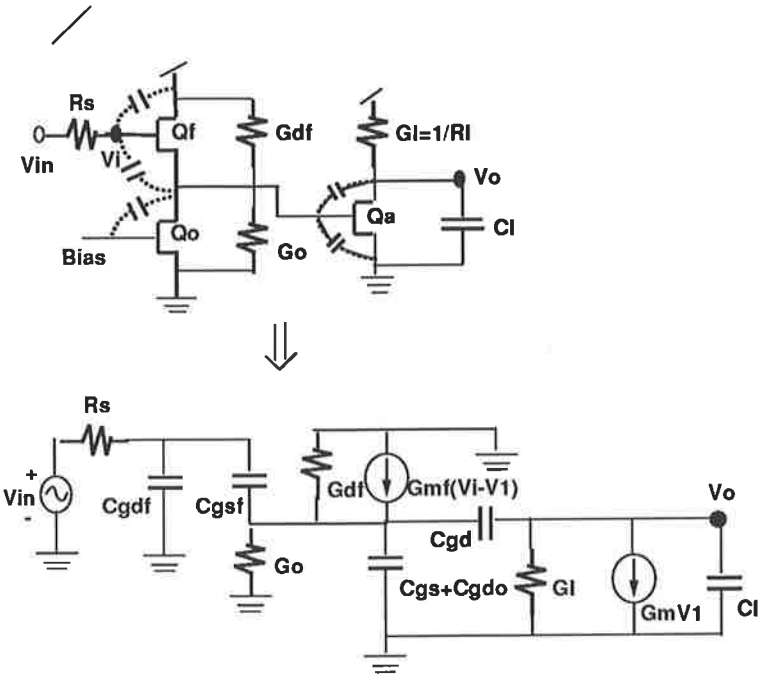

Figure C.1: The simplified high frequency equivalent circuit

C_{gsf} is the gate to source capacitance of Qf

C_{gd} is the gate to drain capacitance of Qa

C_{gs} is the gate to source capacitance of Qa

C_{gdo} is the gate to drain capacitance of Qo

G_{df} is the output conductance of Qf

G_o is the output conductance of Qo

G_{mf} is the transconductance of Qf

G_m is the transconductance of Qa

$A = -G_m/(G_l + sC_{gd})$ is the gain of the inverter

The source to drain capacitances are very small compared with gate to drain and gate to source capacitances, so they are neglected in the analysis. In the design, R_s is mainly introduced by the channel resistance of the input switch, and C_l is the

C_{gdf} of the following stage.

$$(V_{in} - V_i)G_s = (V_i - V1)sC_{gsf} + V_i \cdot sC_{gdf} \tag{C.1}$$

$$(V_i - V1)(sC_{gsf} + G_{mf}) = V1(G_{df} + G_o + s(C_{gdo} + C_{gs} + C_{gd}(1 + A))) \tag{C.2}$$

$$V_o(G_l + s(C_l + C_{gd})) = -G_m \cdot V1 \tag{C.3}$$

from equation C.2 and equation C.3

$$\frac{V_o}{V1} = -\frac{G_m}{G_l + sC_l + sC_{gd}} V_i(G_{mf}+sC_{gsf}) = V1[(G_{mf}+G_{df}+G_o)+s(C_{gdo}+C_{gsf}+C_{gs}+C_{gd} \tag{C.4}$$

then we have

$$\frac{V1}{V_i} = \frac{G_{mf} + sC_{gsf}}{G_{mf} + G_{df} + G_o + s(C_{gd}s + C_{gsf} + C_{gs} + C_{gd}(1 + A))} = Av_{in} \tag{C.5}$$

Applying the equation C.5 to equation C.1 yields

$$V_{in} \cdot G_s = V_i(G_s + s(C_{gsf} + C_{gdf} - Av_{in} \cdot C_{gsf})) \tag{C.6}$$

For good source follower the gain, Av_{in} is very close to unity. So, the capacitance C_{gsf} is cancelled, then

$$\frac{V_i}{V_{in}} = \frac{G_s}{G_s + sC_{gdf}} \tag{C.7}$$

The final equation is

$$\frac{V_o}{V_{in}} = \frac{V_o}{V1} \cdot \frac{V1}{V_i} \cdot V_i V_{in} = \frac{-G_s(G_{mf} + sC_{gsf})G_m}{(G_s + sC_{gdf})[(G_{mf} + G_{df} + G_o) + s(C_{gdo} + C_{gsf} + C_{gs} + (1 + A)$$

(C.8)

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