

Phase retrieval of programmable photonic integrated circuits based on an on-chip fractional-delay reference path

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Programmable photonic integrated circuits (PICs), offering diverse signal processing functions within a single chip, are promising solutions for applications ranging from optical communications to artificial intelligence. While the scale and complexity of programmable PICs are increasing, their characterization, and thus calibration, becomes increasingly challenging. Here we demonstrate a phase retrieval method for programmable PICs using an on-chip fractional-delay reference path. The impulse response of the chip can be uniquely and precisely identified from only the insertion loss using a standard complex Fourier transform. We demonstrate our approach experimentally with a four-tap finite-impulse-response chip. The results match well with expectations and verify our approach as effective for individually determining the taps' weights without the need for additional ports or photodiodes. © 2022 Optica Publishing Group under the terms of the Optica Open Access Publishing Agreement

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1. INTRODUCTION

Programmable photonic integrated circuits (PICs), which are assemblies of reconfigurable integrated optical elements, support the high bandwidths needed for signal processing [1–8]. Being empowered by the reconfigurability of optical building blocks, they enable diverse functions within a single chip, such as routing, switching, and equalizing for optical communications, and spectrum slicing and filtering for signal processing; thus, they are promising for a wide range of applications, including optical communications and signal processing [9–16], quantum computing [17], and artificial intelligence [18].

The specific functionality of a linear PIC is dictated by its transfer function (i.e., frequency response) or equivalently, its temporal impulse response. Owing to the difficulties in maintaining sub-wavelength accuracies during fabrication [19], adaptive post-production tuning is commonly necessary to deliver a desired frequency response. Furthermore, calibrated tuning can support tunable filtering and routing. While the scale and complexity of programmable PICs is increasing, supported by maturing fabrication processes, the difficulties in accurately characterizing and thus controlling programmable PICs is becoming a severe limitation to their practical application. This is mainly due to the challenge in accurately calibrating the phase response of an optical

chip, especially when the optical chip is included in an external interferometer such as a two-port optical analyzer, and connected via flexible patch leads.

Recently, we proposed an approach to accurately calibrate the phase response of an optical chip that builds an on-chip interferometer by adding an on-chip reference path, around the desired signal processing core (SPC) [20]. The reference path could be an additional arm of a finite-impulse-response (FIR) filter, for example, but with the shortest delay. The added reference path enables the Kramers–Kronig relationship [21–25] to be used to recover the phase information of the chip from its power response; this response is easy to measure using a tunable laser source (which is ubiquitous in wavelength-division multiplexing communications systems) and a photodiode, both of which could be on-chip or off-chip, in which case, the technique is immune to phase variations in the patch leads. Our demonstrated chip calibration technique provides a stable and accurate approach for the characterization of the chip's full frequency response, including optical phase, under various tuning conditions. However, the Kramers–Kronig phase retrieval requires certain conditions for it to be valid, often stated as the minimum phase condition. This condition can be guaranteed by using a very strong signal in the reference path, or more precisely, a signal stronger in power than the signal in the SPC. Although the

minimum phase condition can be straightforwardly implemented for generic applications, the relatively weak optical power allocation to the SPC could lead to limitations on the signal-to-noise ratio (SNR) for calibration.

In this paper, we demonstrate a phase retrieval method for programmable PICs based on adding an on-chip fractional-delay reference path. We show that if the reference path has half the delay of the delay increments in the SPC, the phase and amplitude weights of every delay path in the chip can be uniquely and precisely identified from only the power response (i.e., containing no phase information) using a standard complex Fourier transform. In contrast to our previous work that used Kramers–Kronig relations, this method removes the optical power restrictions brought about by the minimum phase condition, thus enabling a potentially higher SNR in the signal path for calibration; and eliminates the need for Hilbert transforms and nonlinear functions to reduce the computational complexities of the calibration system. We performed detailed theoretical simulations of three generic signal

processing functions, including a 32-tap FIR filter, a micro-ring resonator (MRR), and cascaded MRRs; and experimental demonstrations using a four-tap FIR filter integrated on a chip. The results match well with expectations and verify our approach as effective for the calibration of programmable PICs.

2. THEORY

As shown in Fig. 1, our custom PIC consists of an SPC coupled in parallel with a reference path that has the shortest delay on the chip. The SPC can be implemented in diverse forms such as FIR filters and infinite-impulse-response (IIR) filters [2], with a frequency response of H_{SPC} and a discrete impulse response of h_{SPC} .

The operation of the phase extraction consists of two steps. In the first step, the insertion loss (i.e., magnitude-squared amplitude response, or power response) within the calibrating free spectral ranges (FSRs) is measured with a wavelength-swept laser and an optical power meter, via the optical ports accessing both the SPC and the reference path. We shall show that this measurement is

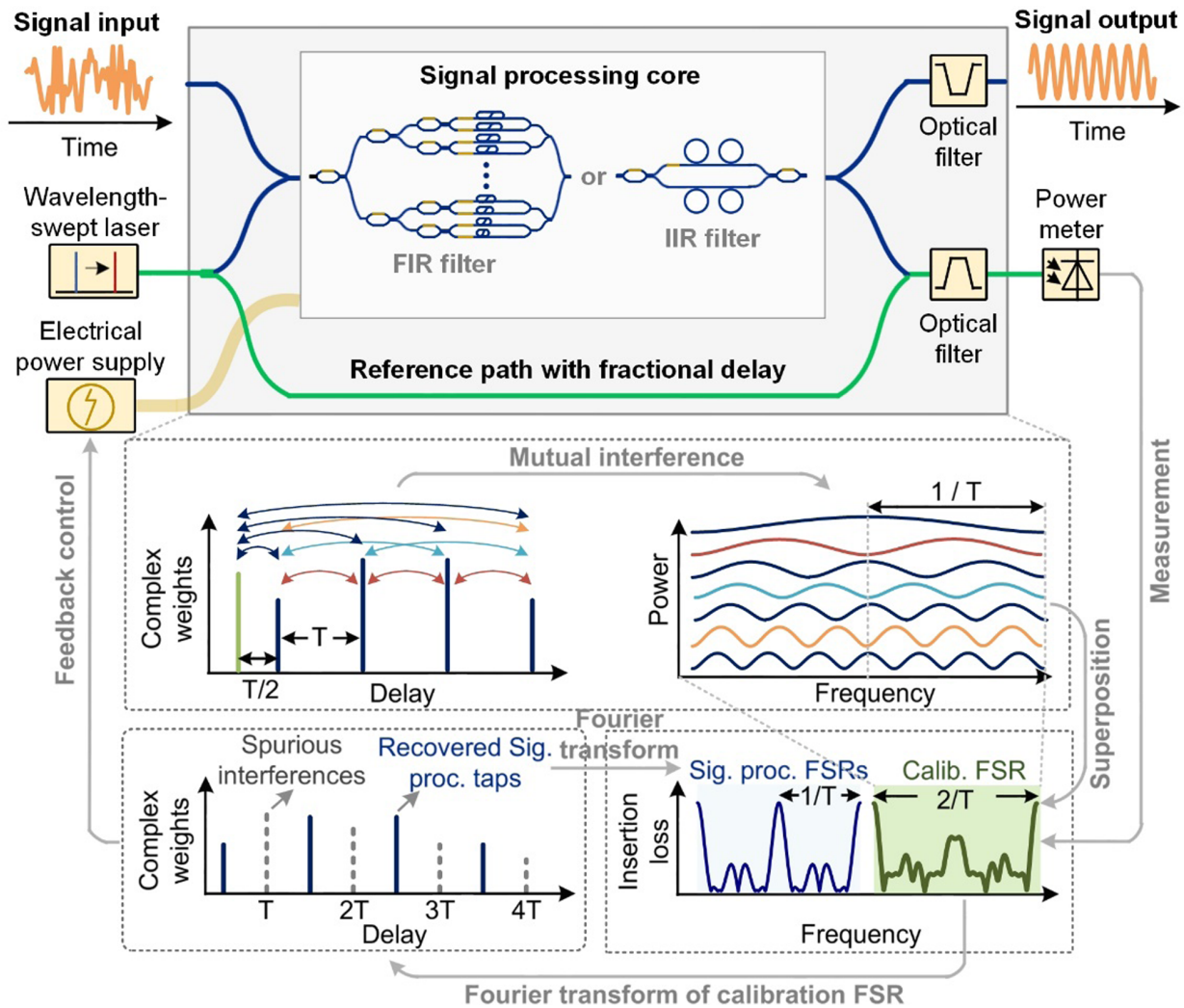


Fig. 1. Conceptual diagram of the phase recovery approach based on a fractional-delay reference path. The chip consists of a signal processing core and a reference path with fractional delay. The signal processing core can be implemented with diverse structures such as FIR or IIR filters. The chip features two pairs of optical input and output ports, including the top pair for signal processing (blue line) and the bottom pair for calibration (green line). A wavelength-swept laser and an optical power meter are used to measure the power response of the whole chip within two FSRs (denoted as $2/T$), while the remaining FSRs are used for signal processing, guaranteed by the optical filters. The power response of the chip can be regarded as the superposition of frequency-domain raised-sinusoidal responses originating from internal interferences among all taps. The signal processing core's tap coefficients are recovered via a Fourier transform, then used for error calculation and feedback control of the electrical power applied onto the chip.

sufficient to recover the phase and amplitude weights of each delay path relative to the reference, and thus the frequency and impulse responses of the SPC. In the second step, after the chip is calibrated/reconfigured, the SPC can be used for subsequent applications via the signal input/output ports, in FSRs other than those used for calibration.

The power response $|H_{\text{chip}}|^2$ of the whole chip (i.e., the insertion loss spectrum that is straightforward to measure) can be regarded as the superposition of frequency-domain raised-sinusoidal responses originating from: (i) “internal” interferences between pairs of the SPC’s taps (i.e., discrete complex impulse response); and (ii) the “external” interferences between the reference path and each of the SPC’s taps.

By performing Fourier transform of $|H_{\text{chip}}|^2$, a temporal series h_{rec} can be obtained, which contains: impulse response information of the SPC corresponding to external interferences (ii), and interfered spurious terms corresponding to internal interferences (i). We show that by choosing the delay of the reference path carefully, we can separate components (i) and (ii) and so isolate the impulse response of the SPC using an inverse Fourier transform of the intensity response spectrum.

Specifically, the temporal interval between the reference path and the shortest delay of the SPC is set as $T/2$, where T is the minimum temporal interval (i.e., delay step) of h_{SPC} . This indicates

that the delays between the SPC’s paths and the reference path are $(n + 0.5)T$, where n is an integer, and the SPC’s discrete impulse responses, or taps, locate at $(n + 0.5)T$, as shown in Fig. 1, and all spurious signals fall at nT . We note that two FSRs (each given by $1/T$) of the SPC are needed for phase retrieval, as the introduced reference path features a fractional delay of $T/2$, thus making the FSR of the whole chip $2/T$.

Because of the choice of our reference delay, the internal interferences (i) will fall at different delays to the wanted external interferences (ii), and so can be rejected. The recovered SPC’s taps locate at “fractional” delays of $(2n + 1)T/2 = (n + 0.5)T$, while the unwanted interferences (a) locate at integral delays of $(2n + 2)T/2 = (n + 1)T$, with $n = 0, 1, 2, \dots$, as illustrated in Fig. 1. If the zero delay is also rejected, we will be left with the complex impulse response for the SPC, which can be transformed to the SPC’s frequency responses including both the amplitude and phase information.

In this way, the SPC’s complex tap coefficients, or impulse response, can be recovered from the amplitude response of the whole chip, enabling subsequent calibration and reconfiguration of the SPC towards desired functions. The integrated reference path offers a compact and stable solution for on-chip phase recovery in programmable PICs. In contrast to our previous work, this phase recovery approach further removes the requirement for a

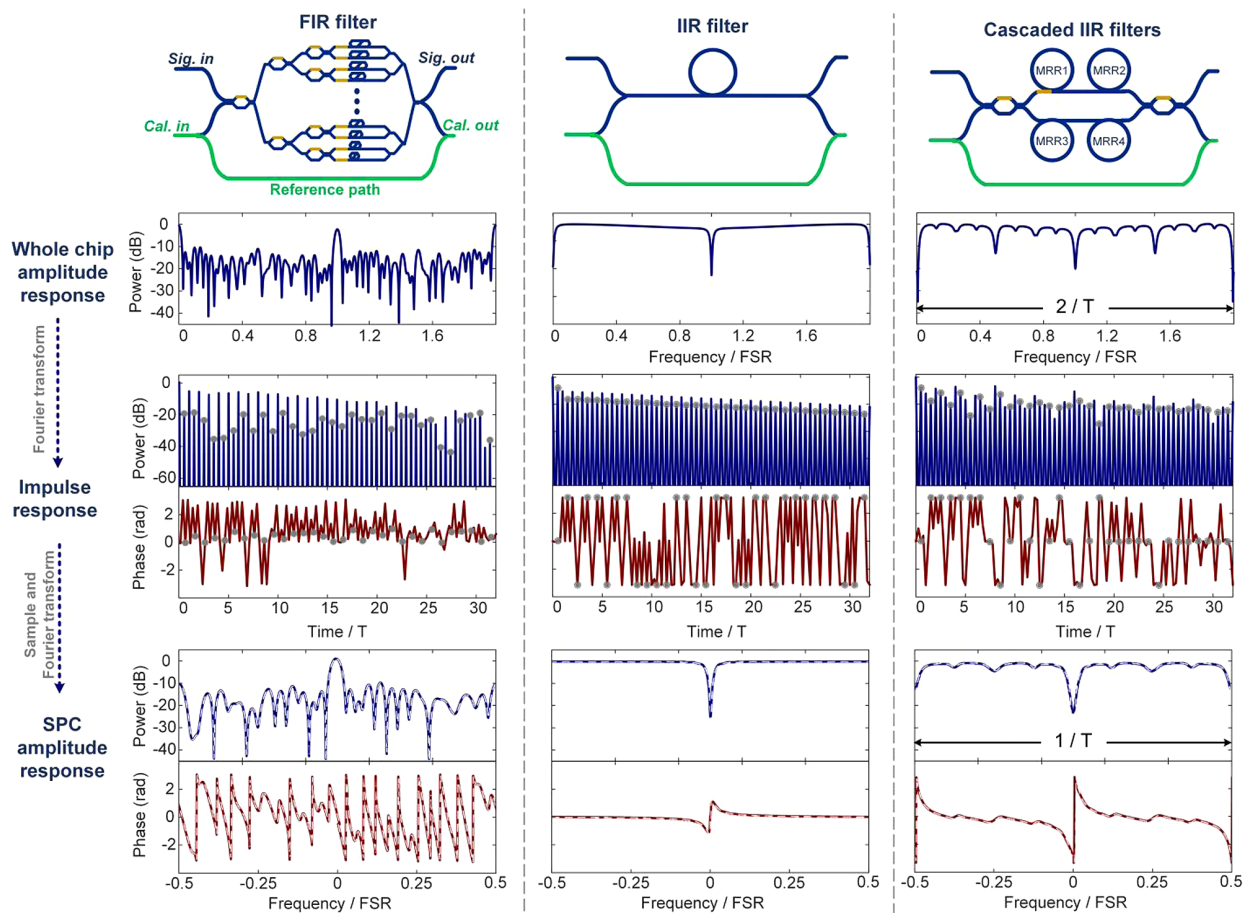


Fig. 2. Simulated phase recovery results, including three typical architectures for signal processing (top row): 32-tap FIR filter with random tap coefficients, micro-ring resonator, cascaded micro-ring resonators; corresponding amplitude response of the whole chip (second row); recovered impulse responses after Fourier transform (solid line, third row), where the gray dots and circles show the ideal and recovered values, respectively; corresponding transfer function of the signal processing core calculated from the recovered impulse responses (solid line, bottom row), where the white dashed lines, indicating ideal values calculated from ideal tap coefficients, overlap with the recovered results.

large proportion of the input power to be used for the reference path, and the need for Kramers–Kronig phase recovery including its Hilbert transform and nonlinear functions, potentially enabling more robust and faster calibration of programmable PICs.

3. RESULTS

To verify the reach of our approach, we first performed theoretical simulations of three typical on-chip signal processing building blocks, including a 32-tap FIR filter, a single MRR, and cascaded MRRs. As shown in Fig. 2, assisted by the reference path, the impulse response of the SPC can be accurately extracted from the power response via a single Fourier transform operation, verified by the close match between the recovered and ideal transfer function

of the SPC, manifesting that our approach can serve as a universal phase recovery method for generic on-chip photonic devices. We note that the power spectrum is supplied directly from the real frequency-domain input of the Fourier transform, and the imaginary part is null.

We also fabricated a four-tap FIR chip with a built-in reference on a silicon-nitride (SiN) loaded thin-film lithium niobate on insulator (Si₃N₄/LNOI) platform [26,27], as shown in Fig. 3. Electron-beam lithography and reactive ion etching were used to define the optical waveguides. Plasma enhanced chemical vapor deposition created a 2 μm thick silica cladding layer, and metal lift-off was used to define the micro thermal heaters to control the

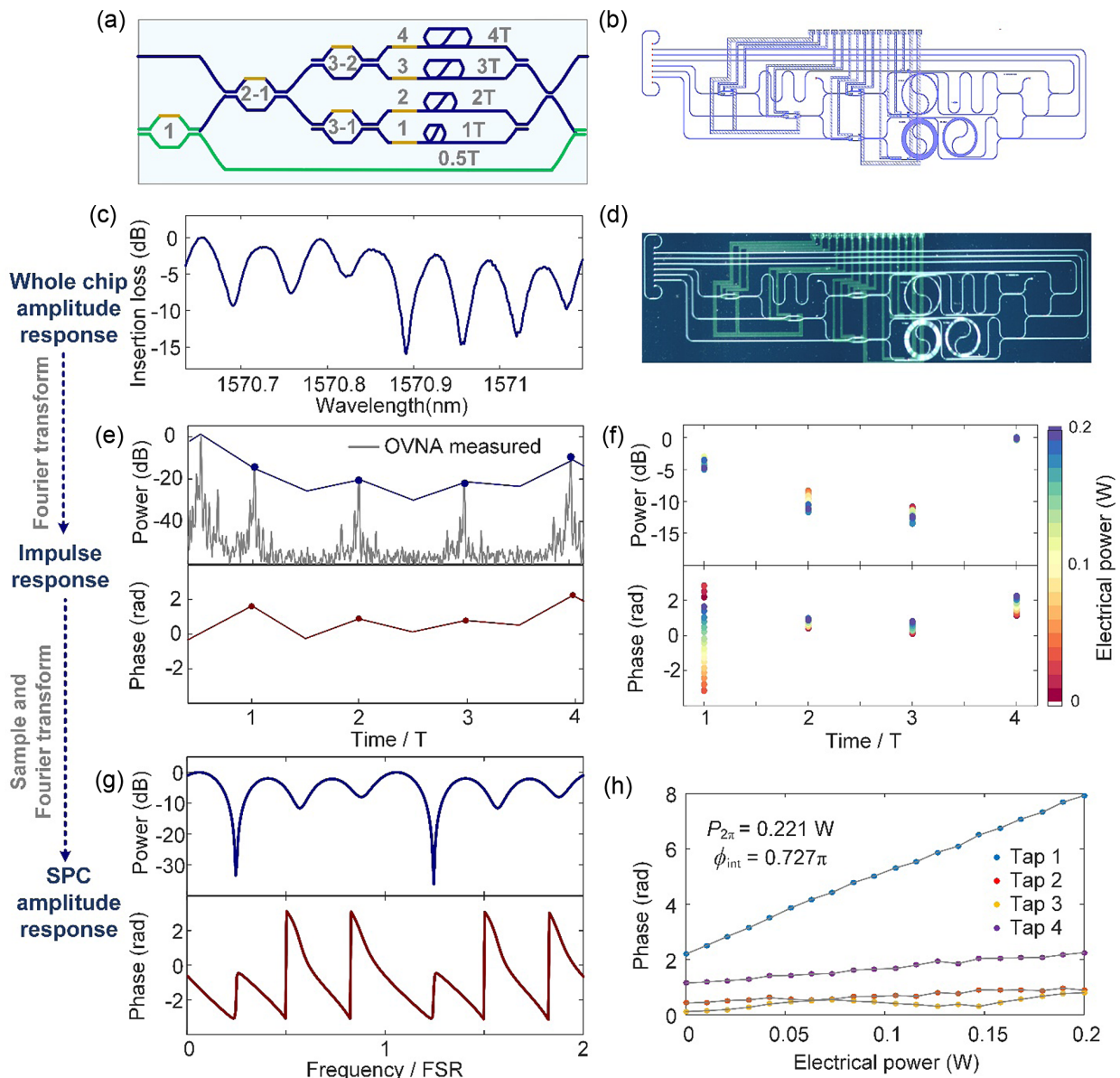


Fig. 3. Experimental phase recovery results of a four-tap FIR filter. (a) Chip architecture, where $T = 35.8$ ps, corresponding to an FSR of $1/T = 28$ GHz for the FIR filter; (b) chip layout; (c) photomicrograph. The phase recovery process for a specific set of tap coefficients is shown in (c), (e), (g); (c) measured insertion loss spectrum after normalization (i.e., power or squared amplitude response) of the whole chip—note the delay increment and the delay between the reference and first path's tap; (e) recovered impulse response (blue/red lines and dots) and measured impulse response amplitudes using commercial equipment (gray line); (g) transfer function of the FIR signal processing core calculated from the recovered impulse response. The electrical power of the first tap was swept, with the recovered impulse responses shown in (f), (h); (f) powers and phases of the four taps as a function of the electrical power applied onto phase shifter 1; (g) phases of the four taps as a function of electrical power.

power splitting of the Mach–Zehnder interferometers and the phase of the delays.

We first verified the phase recovery process for a specific set of tap coefficients (in the case when no electrical power is applied to the FIR chip). The insertion loss spectrum (i.e., squared amplitude response) of the whole chip $|H_{\text{chip}}(\omega)|^2$ was measured with an optical vector network analyzer (OVNA, Luna OVA 5000) [Fig. 3(c)], and used for the recovery of the complex impulse response [Fig. 3(e)] via the Fourier transform. The OVNA was also able to internally calculate the impulse response of the chip, including an impulse from the reference path. Figure 3(e) demonstrates the close match between the recovered (blue dots) and measured (gray line) amplitudes of the impulse response, verifying our approach experimentally. The full complex frequency response

of the FIR SPC can thus be calculated, and used to calibrate it for optical signal processing applications.

Further, we swept the electrical power onto phase shifter 1 [labeled in Fig. 3(a), corresponding to the phase of the FIR filter's first tap] from 0 to 0.2 W. As shown in Figs. 3(f) and 3(h), while the first tap's phase increases linearly with applied power, the amplitudes and phases of the remaining taps are almost constant, albeit with minor variations due to thermal cross talk. These variations could be calibrated out with a suitable intelligent control algorithm. The initial phase of tap 1 was extracted as 0.272π , and the electrical power needed to achieve a 2π phase shift is 0.221 W.

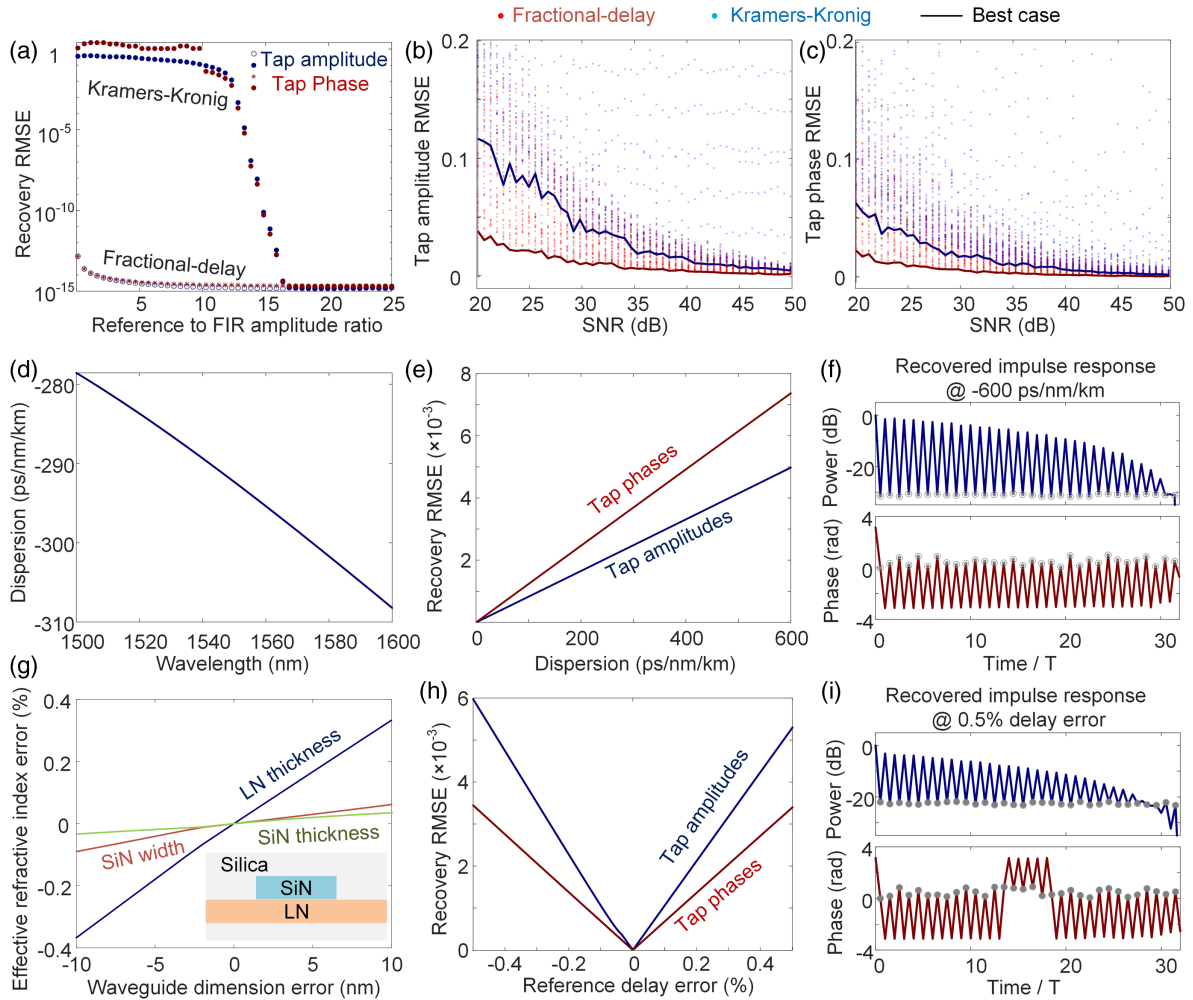


Fig. 4. Performance analysis of a 32-tap FIR chip with normalized tap amplitudes (within [0.8, 1]) and phases (within $[0, \pi]$). (a)–(c) Comparison of performance of phase recovery based on the Kramers–Kronig relationship and fractional-delay method. (a) RMSE of recovered tap coefficients versus the amplitude ratio between the reference path and the FIR filter. Note that the recovery RMSEs are in the same units as the recovered tap coefficients (i.e., rad for recovered tap phases). (b), (c) RMSEs of recovered tap coefficients versus SNR, for reference to FIR amplitude ratios within [1, 50]. (d)–(f) Impact of waveguide dispersion on the performance of phase recovery using the fractional-delay method. (d) Simulated waveguide dispersion. (e) RMSEs of recovered tap coefficients with different waveguide dispersions within [0, 600] ps/nm/km. (f) Recovered impulse response in the worst case (solid line: recovered impulse responses after Fourier transform; gray dots and circles: ideal and recovered values, respectively; note that the recovered impulse responses at integral time indices represent internal interferences that are to be discarded, while the values at fractional time indices represent external interferences kept as the tap coefficients, which is an expected consequence of using the fractional delay). (g)–(i) Impact of reference delay error on the performance of phase recovery using the fractional-delay method. (g) Simulated effective refractive index error with different waveguide dimension errors. (h) RMSEs of recovered tap coefficients with different reference delay errors within $[-0.5\%, 0.5\%]$. (i) Recovered impulse response in the worst case (solid line: recovered impulse responses after Fourier transform; gray dots and circles: ideal and recovered tap coefficients, respectively).

4. DISCUSSION

The Kramers–Kronig relationship has been sufficiently verified as effective for phase recovery of generic two-port photonic integrated devices [20]. In contrast, the proposed fractional-delay method is tailored for phase recovery of programmable PICs with discrete impulse responses, which are sufficient to implement optical functions inspired by digital signal processing (such as FIR, IIR, and waveguide meshes). The key advantages of the latter include: (a) avoiding the relatively weak optical power allocation to the SPC, introduced by the minimum phase condition [20], which could lead to limitations onto the SNR for calibration; (b) eliminating the need for Hilbert transform and log operations used in Kramers–Kronig phase recovery, thus potentially enabling a faster calibration process.

Here we provide numerical analysis for the case of a 32-tap FIR filter with randomly generated tap coefficients (note that to guarantee sufficient intensity distribution of each tap for the evaluation of recovered phases, we employed a sets of tap amplitudes ranging from 0.8 to one) and compare two phase recovery methods based on the Kramers–Kronig relationship and the fractional-delay approach proposed in this work. Figure 4(a) shows the RMSE of recovered tap coefficients with different reference to FIR amplitude ratio within [0.1, 25], which clearly reveals the constraints introduced by the minimum phase condition: the power allocation to the reference path needs to be significantly larger than the tap amplitudes of the FIR filter to sustain the Kramers–Kronig relationship. Figures 4(b) and 4(c) show the RMSE of recovered tap coefficients with additive Gaussian white noise loaded onto the amplitude response of the full chip, emulating the case of practical measurements. The SNR is swept from 20 to 50 dB (horizontal axis), and the reference to FIR amplitude ratio is swept from one to 50 (superimposed dots). As can be seen, the fractional-delay method shows better performance under noise loading.

To analyze the impact of waveguide dispersion and reference delay errors, we simulated the case of a 32-tap FIR filter. Our waveguide structure comprises a 300 nm thick SiN waveguide loaded on 300 nm thin-film LN sitting on a silica box layer with a 2 μm silica cover [as shown in Fig. 4(g)], which has a calculated dispersion of -293 ps/nm/km at 1550 nm [Fig. 4(d)]. During the simulation, we swept the waveguide dispersion from 0 to -600 ps/nm/km and calculated the corresponding RMSEs of the impulse response recovery, which were negligible [Figs. 4(e) and 4(f)]. We note that the delay error induced by dispersion (in proportion to the desired delay) is denoted by $\beta \cdot \omega \cdot v$, where β denotes the dispersion, ω denotes the offset angular frequency, and v denotes the speed of light in the waveguide. In our case, with $\beta = -300 \text{ ps/nm/km} \approx -3.8 \times 10^{-25} \text{ s}^2/\text{m/rad}$, maximum offset angular frequency $1.76 \times 10^{11} \text{ rad/s}$ (28 GHz), $v = 1.34 \times 10^8 \text{ m/s}$, the proportional delay error is of the order of 10^{-6} , thus having a negligible impact on phase recovery. However, for broadband applications across the full C-band, the waveguide dispersion needs to be managed using tailored near-zero-dispersion waveguide structures [28], to reduce its impacts on FSRs away from the calibration FSR. Further, we investigated the impact of delay errors in the reference arm. The desired delay difference between the reference arm and the SPC is $2400.6 \mu\text{m}$. In practice, the delay error mainly comes from the fabrication error of waveguide dimensions, which changes the refractive index and therefore the effective length of the delay line [Fig. 4(g)]. The simulated results reveal a delay error of $< +/ - 0.4\%$ for

standard $+/- 10 \text{ nm}$ fabrication errors, corresponding to negligible RMSEs of < 0.007 . We swept a delay error of $+/- 0.5\%$ ($+/- 12 \mu\text{m}$), and obtained negligible RMSEs of $< 6 \times 10^{-3}$ for the recovered tap coefficients [Figs. 4(h) and 4(i)].

In addition, although our method is designed for two-port devices, recovery of the phases of multi-port devices is achievable by further tailoring the parallel coupling method with the reference path. The key to achieving this is adding external waveguide structures to convert the multi-port device into a two-port device, with different delays introduced between different pairs of input/output ports (see [20] Supplementary Materials). We note that such a design involves a trade-off: on one hand, an additional on-chip coupling tree, which introduces increased footprint and complexity, is necessary; on the other hand, the characteristic of the multi-port device can be obtained with a single sweep, avoiding multiple measurements of different pairs of input/output ports.

5. CONCLUSION

In conclusion, we have demonstrated a phase retrieval method for programmable PICs. By employing a built-in reference path with fractional delay, the impulse response of the chip can be determined from the power response via a single Fourier transform. We performed detailed theoretical simulations of three generic signal processing functions, including a 32-tap FIR filter, an MRR, and cascaded MRRs; and experimental demonstrations using a four-tap FIR filter integrated on a chip. The results verify our approach as effective for the calibration of programmable PICs, potentially enabling fast reconfiguring PICs towards applications ranging from optical computing to quantum applications.

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Data Availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

[†]These authors contributed equally to this work.

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