Colour Cameras in Standard CMOS

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Thesis submitted for the degree of

Doctor of Philosophy

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December 22, 1998

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List of Abbreviations

A/D	Analog-to-Digital (converter)
ADCT	Adaptive Discrete Cosine Transform
ADU	Analog-to-Digital converter Units
AGC	Automatic Gain Control
APS	Active Pixel Sensors
ASIC	Application Specific Integrated Circuit
BASIS	BAse Stored Image Sensor
BCCD	Buried channel CCD
CB	CrowBar
CCD	Charge-Coupled Device
CDS	Correlated-Double Sampling
CFA	Colour Filter Array
CIE	Commission Internationale de l'Eclairage
CIF	Common Intermediate Format
CMD	Charge Modulation Device
CMOS	Complementary Metal-Oxide-Semiconductor
CRT	Cathode Ray Tube
DR	Dynamic Range
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor
EPROM	Erasable Programmable Read Only Memory
FD	Floating Diffusion
FIFO	First In First Out
FPN	Fixed Pattern Noise
FSM	Finite State Machine
FIT-CCD	Frame Interline Transfer CCD
FT-CCD	Frame Transfer CCD
HAD	Hole Accumulation Diode
HDTV	High Definition Television
IEEE	Institute of Electrical and Electronic Engineers
I/O	Input/Output
IL-CCD	InterLine transfer CCD

IR	Infra-Red
IT-CCD	Interline Transfer CCD
JPL	Jet Propulsion Laboratory
JPEG	Joint Photographic Experts Group
LCD	Liquid Crystal Display
MAC	Multiply-ACcumulate
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MPEG	Moving Pictures Expert Group
MSE	Mean Squared Error
NJ	New Jersey
NTSC	National Television Systems Committee
OTA	Operational Transconductance Amplifier
PAL	Phase Alternating Line
PC	Personal Computer
PGA	Programmable Gain Amplifier
PLD	Programmable Logic Device
PRNU	Photo-Response Non-Uniformity
PSTN	Public Switched Telephone Network
RAM	Random Access Memory
RMS	Root Mean Squared
SCCD	Surface channel CCD
SF	Source Follower
S/H	Sample-and-Hold
SIT	Static Induction Transistor
SNR	Signal-to-Noise Ratio
SRAM	Static Random Access Memory
USB	Universal Serial Bus
UV	Ultra-Violet
VDA	Video Difference Amplifier
VHDL	Very high speed integrated circuit Hardware Description Language
VLSI	Very Large Scale Integration

Abstract

A recent advancement in solid-state imaging technology known as Active Pixel Sensors (APS) is poised to challenge the dominance of the established Charge-Coupled Device (CCD) technology. Traditionally CMOS imaging arrays have suffered from poor noise performance. However, the availability of CMOS with sub-micron feature dimensions has made practical the inclusion of active devices within each pixel to provide signal gain and buffering functions. Combined with techniques such as correlated-double sampling (CDS), CMOS APS image sensors have been developed that deliver image quality approaching that of CCD sensors. Unlike CCD sensors, the architecture of APS sensors are inherently low power and compatible with the integration of camera system electronics onto the same die as the imager. Consequently CMOS APS technology has the potential to reduce the power, size, and cost of solid-state cameras.

While CMOS APS image sensors are already finding their way into products, a number of important issues remain open research questions. This thesis addresses two important areas of investigation, the fundamental performance limitations of CMOS APS sensors, and the development of highly integrated camera systems. After reviewing the relevant concepts of solid-state imaging and digital colour camera technology, the performance limitations of CMOS APS image sensors are identified through the experimental evaluation of a state-of-the-art colour photogate sensor. It is demonstrated that by using two levels of CDS fixed-pattern noise (FPN) due to circuit mismatch is eliminated, and instead FPN performance becomes limited by non-uniformity of the sensor dark current, and non-uniformity of the pixel floating diffusion node capacitance. High conversion gain in the photogate pixel ensures that the temporal noise performance of the sensor is determined at the pixel level by low quantum efficiency. At low signal levels charge transfer noise and dark current shot noise also degrade performance. The colorimetric accuracy of the sensor is limited by significant pixel cross talk. It is argued that to achieve CCD-level performance or greater it will be necessary to address these issues at the device level through modification of the standard CMOS fabrication process.

The issues pertinent to camera system integration using CMOS APS technology are investigated through the development of a single-chip digital colour camera. The camera, intended for multi-media applications, features a fully digital programming interface, and a sophisticated temporal sequencing scheme to investigate the coupling of digital switching noise into analog circuits via the chip substrate and power supply buses. The architecture of the single-chip camera is described, and its performance experimentally evaluated. The camera is realized as a 740K device integrated circuit which produces 24-bit RGB pixel data of 352 ×

288 resolution at 30 frames/second while dissipating 182mW from a 3.3V supply. It is shown that contrary to expectations digital switching noise does not degrade camera system performance.

Statement of Originality

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Acknowledgements

The author would like to acknowledge the outstanding supervision of Abdesselam (Salim) Bouzerdoum, formerly of the University of Adelaide, and Bryan Ackland of Bell Laboratories; Salim for his encouragement, availability, and rigour, and Bryan for his constructive criticism, ability to see the big picture, and providing the opportunity to visit Bell Labs.

The author is deeply indebted to Marc Loinaz of Bell Laboratories who collaborated on much of this work. His enthusiasm, generosity, intellect, and support have been greatly appreciated by the author.

The author would also like to acknowledge Dick Kollarits and David Gibbon of AT&T Laboratories for their introduction to the mysteries of colour science, and to Iliana Fujimori of the Massachusetts Institute of Technology for performing the quantum efficiency measurements.

Sincere thanks are due to the past and present members of the DSP & VLSI Systems Research Department, Bell Laboratories, for their interest and encouragement, in particular Kamran Azadet, Alex Dickinson, David Inglis, Patrik Larsson, Jay O'Neil, Chris Nicol, K. J. Singh, Joe Williams, and Joe Worth.

The author has also enjoyed interaction with many colleagues at the University of Adelaide over a number of years including Sam Appleton, Said Al-Sarawi, Richard Beare, Andrew Beaumont-Smith, and Brian Ng. Special thanks must be given to Alireza Moini for his willing involvement in many hours of technical discussion, and Mike Liebelt for his sage advice.

Finally, the author would like to acknowledge his family who have always kept the faith while letting him choose his own path. Thankyou.

CHAPTER 1 Introduction

1-1. Introduction

In this chapter the background and motivation of the thesis are discussed, followed by the context and contributions claimed. The evolution of this body of work is described and collaborations with several co-workers clarified. This chapter concludes with an outline of the thesis structure.

1-2. Background and Motivation

The contributions of this thesis concern an emerging solid-state imaging technology known as *Active Pixel Sensors* (APS) that enables the manufacture of high performance image sensors in Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuit fabrication technology. To establish the background and motivation for this work the incumbent solid-state imaging technology known as Charge-Coupled Device (CCD) is introduced, and a number of its limitations discussed. Early passive MOS and CMOS image sensors are described before the architecture of CMOS APS imagers and their potential advantages are presented. This section concludes with a discussion of the opportunity APS technology has to fundamentally change the technological basis and application space of solid-state imaging.

1-2.1 CCD Imaging Technology

For the last ten years electronic image acquisition has been dominated by a silicon integrated circuit technology known as Charge-Coupled Device (CCD) [Theuwissen 1995]. In the mid-1980's CCD technology displaced the photoconducting tube as the basis of electronic imaging with superior properties in terms of size, weight, power dissipation, and cost [Flory 1985, Theuwissen 1994]. Such characteristics enabled CCD technology to take electronic imaging beyond the exclusive domain of television broadcasters and the scientific and military communities, and created a vast consumer and industrial market for portable video cameras.

1-2.1.1 CCD Sensor Architecture and Operation

A CCD image sensor consists of a two dimensional array of pixels composed of photodetectors and adjacent CCD gates [Theuwissen 1995]. The simplified architecture of an interline-transfer CCD image sensor is shown in Figure 1-1. Photons from incident light are absorbed by the silicon substrate, thereby generating charge carriers that are collected in the depletion regions of an array of photodiodes. During sensor read-out the charge accumulated by each photodiode is transferred by the CCD gates to a single output stage where it is converted into a voltage signal that represents the image.

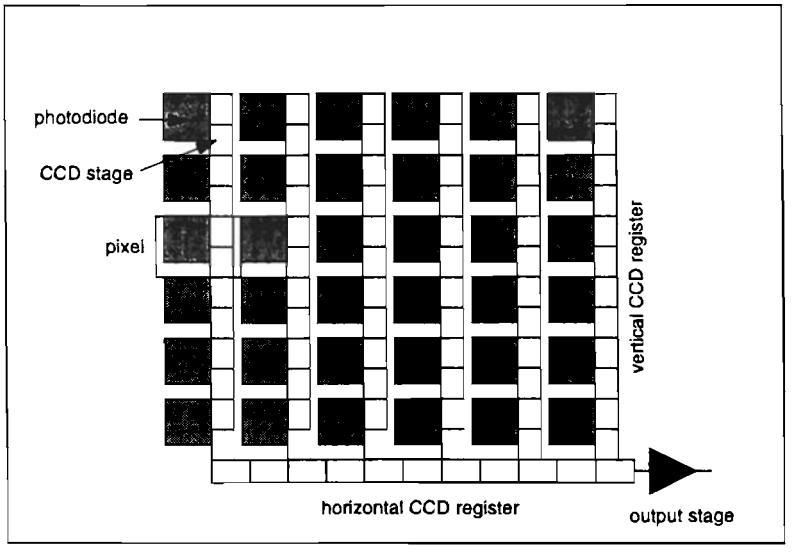


Figure 1-1. Architecture of an interline-transfer CCD image sensor.

1-2.1.2 Limitations of CCD Technology

While CCD technology has been enormously successful, some observers believe that it is not well suited to meet the demands of the next generation of solid-state imaging applications [Fossum 1993, Ackland and Dickinson 1996]. To maintain high image quality while achieving further advancements in resolution, power dissipation, and system integration at an acceptable cost pose difficult challenges for CCD technology. The concerns centre on the fundamental principle of CCD operation, the need for near perfect charge transfer.

1-2.1.3 Charge Transfer Efficiency

As the charge packet from each pixel must be transferred through a large number of CCD gates before it reaches the output stage, the performance of the sensor depends on near perfect charge transfer by each CCD gate. A quantity known as the *charge transfer efficiency,* defined as the fraction of a charge packet successfully transferred from one CCD gate to the next, is used to characterize CCD operation. If the charge transfer efficiency of a CCD sensor is denoted by ζ and the charge packet undergoes m transfers prior to reaching the output stage then the net fraction of the original signal at the output is given by:

$$net\,fraction\,of\,charge\,transferred = \zeta^m \tag{1-1}$$

The importance of high charge transfer efficiency can be clearly demonstrated using an example. If m is 2000 and ζ is 0.999, then the net fraction of charge transferred to the output is only 13.5%; however if ζ is increased to 0.99999, then the net fraction becomes 98.0%.

To achieve sufficiently high charge transfer efficiency it is necessary to minimize defects in the silicon that interact with the charge packets, and to carefully control the potential profiles under the CCD gates [Barbe 1975]. The development of the buried-channel CCD (BCCD) and advancements in process cleanliness have enabled CCD image sensors with extremely high charge transfer efficiency to be developed [Walden et al. 1972, Agwani et al. 1994]. Management of the potential profiles is accomplished by manipulating the doping concentrations used to form the CCD stages, and shaping the voltage waveforms of the clock signals driving the gates [Bosiers et al. 1991, Yamagishi et al. 1991].

1-2.1.4 Resolution

The resolution of a solid-state image sensor is given by the number of pixels in the array. For example, an image sensor in a digital video camera might have a resolution of 724 × 494 pixels, while a camera for high definition television (HDTV) might have a resolution of 1340 × 1045 pixels [Naito et al. 1995, Takemura et al. 1995]. Advancements in lithographic techniques to provide smaller feature dimensions have increased the number of pixels and CCD gates per unit sensor area. Combined with the availability of larger wafer sizes this has enabled the cost of a CCD sensor with a given resolution to fall markedly through the evolution of the technology. The trend to small feature dimensions cannot be continued indefinitely however. Optical diffraction considerations set a lower bound on the pixel size at approximately 3.5μm × 3.5μm [Satoh et al. 1997]. Furthermore, as pixel and CCD gate dimensions decrease there are corresponding losses in imager sensitivity and charge transport capacity that must be overcome [Tabei et al. 1991, Ozaki et al. 1994]. Such difficulties result in a trade-off between the image quality and cost of a CCD image sensor [Kuriyama et al. 1991].

The reliance of CCD architectures on complete charge transfer through a very large number of CCD stages makes such sensors vulnerable to defects introduced during the fabrication process or already present in the starting materials. A fault associated with a single CCD gate may create a visible pixel or column artifact in the output image [Theuwissen 1995]. The number and type of defects that can be tolerated in a sensor for a given application determine in part its cost [Holst 1996]. The manufacturing yield of a CCD imager depends on the sensor size, the number of pixels, and the physical dimensions of the pixels and CCD gates. Considerable investment in CCD fabrication technology is required to develop very high resolution imagers with acceptable yield [Kamasz et al. 1994, Farrier et al. 1997].

1-2.1.5 Power Dissipation

The power dissipation of a CCD image sensor P_{CCD} is a function of the amplitude of the clock voltage V_{clk}, the vertical and horizontal clock frequencies f_v and f_h, and the total vertical and horizontal capacitances C_v and C_h of the CCD stages that the clock signals must drive:

$$P_{CCD} \propto \left(C_v V_{clk}^2 f_v + C_h V_{clk}^2 f_h \right) \quad Watts \tag{1-2}$$

The dependence of the charge transfer efficiency and the charge handling capacity of the CCD gates on the clock voltage makes it a significant design challenge to reduce power dissipation by decreasing the clock voltage V_{clk} without adversely affecting sensor performance [Mutoh et al. 1997, Watanabe et al. 1997, Yamaguchi et al. 1997]. The sensor clock frequencies f_v and f_h are determined by the dimensions of the imaging array, the number of parallel output stages, the video or image format used, and the CCD read-out architecture. Typically f_v and f_h are integer multiples of the line and pixel rates respectively. High resolution sensors often exploit parallelism to reduce the clock frequency of the horizontal CCD registers f_h. However, this is done to minimize the noise bandwidth of the output stage and facilitate high charge transfer efficiency and does not reduce power dissipation [Nishida et al. 1988]. The need to clock each of the CCD gates a large number of times to execute sensor read-out presents the key problem in power reduction. The inherent capacitance of the CCD gates and resistance of the clock lines provide designers with significant challenges in terms of power dissipation and clock distribution. This is particularly true for high resolution sensors [Yamagishi et al. 1991, Morimoto et al. 1995].

1-2.1.6 System Integration

To achieve high imaging performance, CCD technology has diverged significantly from the mainstream integrated circuit technology known as CMOS. Almost all analog and digital integrated circuits from microprocessors to application specific integrated circuits (ASICs) are made in CMOS technology. While there are similarities between the CCD and CMOS fabrication processes, it is not possible to produce efficient CCD and CMOS devices on the same die without compromising the performance of one or both structures [Fossum 1994a]. The impracticality of integrating CMOS circuits on the same chip as a CCD image sensor imposes a bound on the level of system integration that can be achieved for a solid-state camera. Most solid-state imaging applications require hardware resources in addition to the image sensor to provide the clock signals required and to implement functions such as analog-to-digital conversion, colour processing, and image compression [Izawa et al. 1990, Onga et al. 1990, Takemura et al. 1995]. Consequently a typical solid-state camera consists of a CCD image sensor and one or more CMOS integrated circuits to realise camera system functionality. The inability

to reduce the total parts count through further integration is restrictive for compact, low cost applications in terms of the cost and physical size of the assembled camera system [Ackland and Dickinson 1996]. For this reason there has always been an interest in alternative imaging technologies that are compatible with camera integration.

1-2.2 Passive MOS Imaging Technology

The earliest solid-state image sensors were fabricated not in CCD technology, but in the mainstream integrated circuit technology of the time known as Metal-Oxide-Semiconductor (MOS) [Weckler 1967]. The architecture of a simple MOS image sensor is shown in Figure 1-2 [Koike et al. 1980, Aoki et al. 1982]. Charge carriers generated by incident light are collected by the photodiodes. During sensor read-out each row of photodiodes is selected in turn by the row decoder. While a row is active, the column decoder selects each column in turn and the collected charge from the corresponding photodiode is sensed by the output amplifier across the column bus.

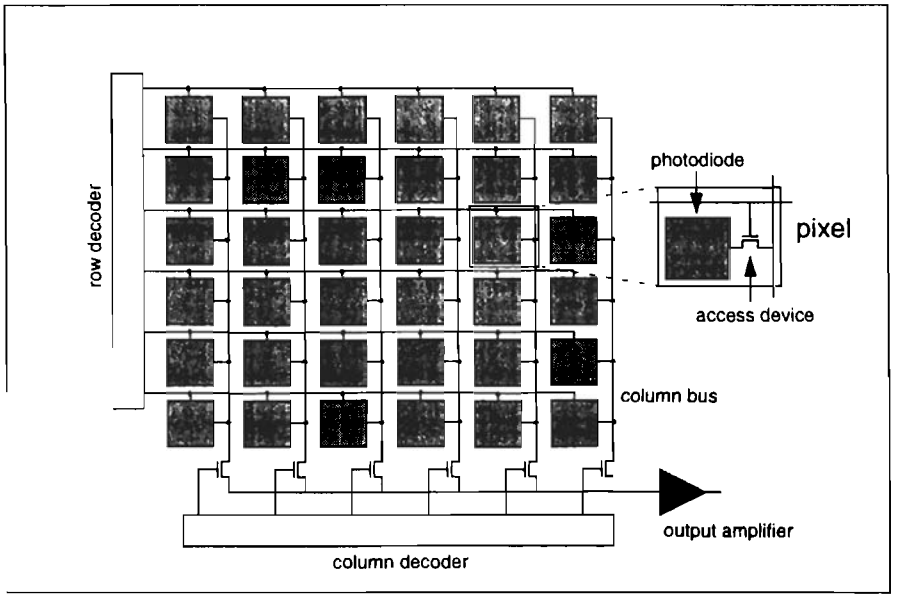


Figure 1-2. Architecture of a passive MOS image sensor.

During the 1980s mainstream integrated circuit technology evolved from MOS to CMOS. However, image sensors developed in CMOS continued to follow the passive architecture of their MOS predecessors [Renshaw et al. 1990]. Due to their architectural similarity the phrase "passive MOS sensor" in the ensuing discussion also includes passive CMOS sensors.

1-2.2.1 Advantages of Passive MOS Sensors

MOS sensors are extremely low power compared with CCD sensors due to the alternative read-out architecture employed. In a MOS sensor the charge from each pixel is directly sensed

across the column bus and not clocked through a large number of capacitive CCD gates using high supply voltages. The power dissipation of a MOS sensor P_{MOS} is a function of the column bus capacitance C_{col}, the signal swing on the column bus during read-out ΔV_{col}, the sensor supply voltage Vdd, and the line rate f_{line}:

$$P_{MOS} \propto C_{col} \Delta V_{col} Vdd \; f_{line} \tag{1-3}$$

Each of these quantities can be made small enabling MOS sensors to typically achieve power savings of more than an order of magnitude over their CCD counterparts.

The other main advantage of MOS sensor technology is its compatibility with camera system integration. As the sensor is manufactured in mainstream integrated circuit technology it is possible to realize camera electronics on the same die as the sensor enabling camera miniaturization and a fully digital camera interface [Renshaw et al. 1990].

Another useful feature of the MOS architecture is that it seemlessly supports both progressive and interlaced read-out. Furthermore, the architecture can be designed to enable random pixel access so that pixels can be addressed in any order. This is useful for certain applications.

1-2.2.2 Limitations of Passive MOS Sensors

Unfortunately the performance of passive MOS sensors is limited by substantial temporal and fixed-pattern noise (FPN) that degrades image quality [Ohba et al. 1980, Noda et al. 1986]. The principle of passive MOS sensor operation is the ability of the output amplifier to sense the signal charge collected at the photodiode over the column bus. For imaging arrays of high resolution the capacitance of the column bus becomes large with respect to the capacitance of the photodiode which makes the charge sensing operation at the required read-out rate challenging. Furthermore, the switching of the column bus capacitance during read-out contributes significant thermal noise that degrades the sensor signal-to-noise ratio (SNR). In addition, mismatch between the pixel access devices and mismatch between the offset and gain of the column circuits introduce significant FPN that is seen as visible stationary artifacts in images output from the sensor. The temporal and FPN problems associated with passive MOS sensors have allowed CCD to become established as the dominant solid-state imaging technology due to its ability to provide superior noise performance [Fossum 1997].

1-2.3 Active Pixel Sensor (APS) Imaging Technology

Recently there has been a significant advancement in CMOS imaging technology known as Active Pixel Sensors (APS) [Fossum 1993, Fossum 1997]. The architecture of an active pixel sensor is shown in Figure 1-3 and is defined as an imager with one or more active transistors located within each pixel.

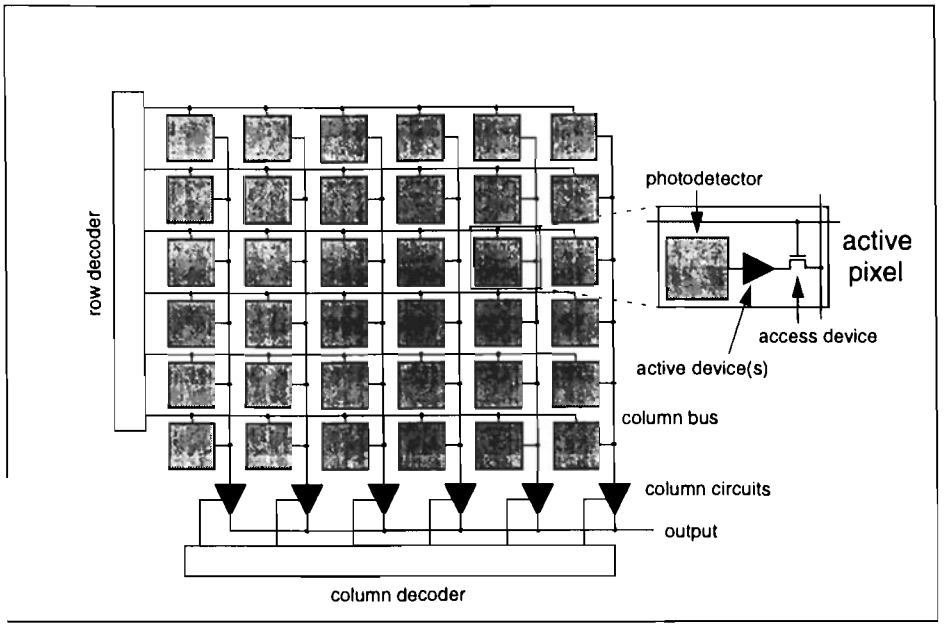


Figure 1-3. Architecture of an active pixel sensor.

APS architectures preserve the advantages of passive MOS sensors in terms of low power dissipation, random access, and the ability to integrate system functionality, but provide significant improvement in noise performance and the ability to scale to large array sizes [Dickinson et al. 1995b]. Manufacturing in a mainstream CMOS fabrication process provides potential cost savings when compared with CCD technology [Fossum 1994b].

Active pixel sensors have been made practical by the availability of CMOS technology with sub-micron feature dimensions. This has created new architectural possibilities by allowing several transistors in addition to the photodetecting device to be included in each pixel to provide additional functionality such as amplification or buffering, electronic shutter, or analog-to-digital conversion [Andoh et al. 1990, Aw and Wooley 1996, Fowler et al. 1994]. However, as the fraction of pixel area used for photodetection decreases there is a corresponding reduction in imager sensitivity [Holst 1996]. For sensors of useful resolution and pixel size this limits the number of additional devices that can be introduced. With present CMOS feature dimensions this appears to range between 3 and 5 minimum sized devices and consequently pixel functionality is typically restricted to row select, charge reset, and amplification or buffering [Mendis et al. 1997b].

1-2.3.1 In-Pixel Signal Buffering

Unlike a CCD or passive MOS sensor the successful operation of an active pixel sensor does not depend on transferring the charge collected at each photodetector to the output stage, or sensing the charge across the column bus. Rather the collected charge is converted into

either a current or a voltage by the active device in each pixel prior to read-out [McGrath et al. 1997, Mendis et al. 1997a]. This current or voltage is sampled across the column bus by the column circuits depending on whether the read-out architecture is current-mode or voltage-mode respectively. The buffering function provided by the active device greatly improves the ability of the pixel to drive the column bus and enables the architecture to be scaled to large array sizes [Dickinson 1996, Scheffer et al. 1997]. If significant signal amplification is performed at the pixel level this can minimize the relative contribution of the thermal noise from the column bus capacitance and downstream read-out circuits to the sensor signal-to-noise ratio [Blanksby et al. 1997]. The two most successful APS architectures developed employ voltage-mode read-out and are known as the active photodiode and active photogate respectively [Mendis et al. 1994b]. Low noise current-mode APS architectures have been more difficult to develop due to the non-linearity of the simple in-pixel charge to current buffers [McIlrath et al. 1997, Nakamura et al. 1997].

1-2.3.2 Fixed-Pattern Noise in APS Imagers

As with passive MOS sensors, APS imagers are subject to fixed-pattern noise due to device mismatch in the pixel and column read-out circuits. However, the architecture of APS arrays have proven compatible with effective schemes to cancel FPN at both the pixel and column level based on a technique known as correlated-double sampling (CDS) [White et al. 1974]. While CDS was originally developed to cancel reset noise in the output stage of CCD sensors, it has recently been demonstrated that CDS can also be employed with the active photogate and the photodiode architectures to significantly reduce FPN and remove several temporal noise components [Fossum 1993, Mendis et al. 1994b]. More advanced FPN correction schemes for APS sensors are possible using a frame memory and additional hardware. The improvement in image quality due to FPN management techniques is substantial, and consequently APS image sensors are finding their way into products [Hurwitz et al. 1997, Smith et al. 1998].

1-2.4 Potential Impact of APS Technology on Electronic Imaging

1-2.4.1 Technological Barrier of Entry to the Solid-State Imaging Market

At present consumer solid-state imaging is dominated by a few large vertically integrated companies that design and fabricate CCD sensors, develop the associated system components, and manufacture and sell the final product. The investment required to develop competing CCD technology creates a considerable barrier of entry that has excluded new companies from entering the market. Active pixel sensor technology seems poised to revolutionize electronic imaging by significantly lowering the technological barrier of entry to the market. If high quality images can be obtained from a sensor fabricated in standard CMOS, then anyone with

access to a CMOS foundry could be a potential player in the market. This trend is already apparent with an increasing number of CMOS design houses and foundries actively developing CMOS APS technology [Wilson 1997]. Increased competition in the market should result in savings for the consumer.

1-2.4.2 Digital Camera Technology

At present electronic imaging is in transition from analog to digital technology. Images that are represented digitally can be more easily edited, reproduced, and transmitted without loss of quality. Advancements in digital image compression has supported the introduction of digital video, and the availability of powerful desktop computing platforms and network technology have created opportunities for new multi-media products and services [Ackland and Dickinson 1996]. An important part of this trend is the emergence of digital photography [Ohno 1996, Konishi and Iwabe 1997]. As the dominant solid-state imaging technology, CCD sensors have formed the basis of almost all the digital camera products that have been released to date [Izawa et al. 1990, Chan and Youe 1995, Parulski and Jameson 1996]. However, for many of these applications CCD technology is not well suited in terms of power dissipation, system integration, and cost. The ability of CMOS APS technology to address each of these issues provides a significant opportunity for it to become established in the marketplace. Furthermore, the unique characteristics of APS technology, combined with an influx of new companies into the market has the potential to stimulate the creation of new imaging applications.

1-3. Thesis Context

To establish the context for the contributions of this thesis the history of active pixel sensors is briefly reviewed and the present state-of-the-art is identified. This leads into a discussion of open research issues in APS technology and areas where contributions remain to be made.

1-3.1 A Brief History of Active Pixel Sensors

1-3.1.1 Early Active Pixel Sensors

The term "active pixel sensor" has been coined to describe an image sensor architecture where one or more active transistors are located within each pixel [Fossum 1993]. The first image sensor that fits this definition was developed 25 years prior to the terms inception. In 1968 Noble published the architecture for a MOS image sensor array that included a source follower transistor within each pixel to buffer the photodiode [Noble 1968]. Soon after, Chamberlain expanded on this work reporting on photosensitivity and read-out architectures [Chamberlain 1969]. However, the feature dimensions of fabrication technology of the day rendered the sensor architecture impractical for mainstream imaging applications. The pixel size was

100μm × 100μm and only a 10 × 10 array was realized. Sensor performance was limited by significant FPN due to threshold voltage variations across the array.

1-3.1.2 Practical Pixel Dimensions

The active pixel sensor concept was revived in the early 1990's as the rapidly shrinking feature dimensions of semiconductor technology began to make an APS array of practical resolution and pixel size feasible. In 1990 the basic architecture of Noble and Chamberlain was used by Andoh et al. to develop a 510 × 490 image array with pixel dimensions 17.3μm × 13.5μm [Andoh et al. 1990]. Sensor FPN was suppressed by subtraction from an external frame memory. Around the same time Yadid-Pecht et al. developed a photodiode array that supported random pixel access [Yadid-Pecht et al. 1991]. Active devices were used within each pixel to provide several buffering functions as part of the signal read-out. However, the sensor performance was degraded by significant cross talk and temporal noise.

1-3.1.3 Fixed-Pattern Noise Reduction

Significant advancements in active pixel sensor technology were introduced by Fossum and his co-workers at the U.S. Jet Propulsion Laboratory (JPL) [Fossum 1993]. The first of these was the double-poly photogate active pixel which essentially realizes a single charge-coupled stage and CCD-style output amplifier within each pixel [Mendis et al. 1993b]. The photogate pixel design required two levels of polysilicon and the sensor was produced in a CMOS fabrication process specialized for analog designs. However, an important achievement of the photogate pixel was that it supported correlated-double sampling to eliminate several pixel temporal noise components and reduce pixel FPN. Subsequently, Fossum and his co-workers developed a column parallel read-out architecture implementing two levels of correlated-double sampling to suppress mismatch between columns in addition to FPN at the pixel level [Mendis et al. 1994a]. Using different timing this same column circuit architecture could also be used with an active photodiode array to suppress pixel and column FPN.

1-3.1.4 New Pixel Designs

To allow sensor fabrication in a standard digital CMOS process a photogate pixel was developed by a group working at AT&T Bell Laboratories that required only a single polysilicon layer. This led to the successful manufacture of photogate APS arrays of size 256 × 256 and 1024 × 1024 [Dickinson et al. 1995a, Dickinson et al. 1995c]. The single-poly photogate pixel design was also arrived at separately by Fossum and his co-workers at JPL [Mendis et al. 1994a]. As well as the basic active photogate and photodiode architectures, a number of derivative pixel designs have been reported including the floating gate pixel [Mendis et al. 1993a, Nakamura et al. 1995], and pixels with individual reset [Yadid-Pecht et al. 1997].

1-3.1.5 Current-Mode APS Image Sensors

In addition to the voltage-mode APS sensors a number of architectures based on a current-mode approach have been developed [Aw and Wooley 1996, McGrath et al. 1997, Nakamura et al. 1997]. The largest of these sensors features a 768×512 array and a difference mode to reduce fixed-pattern noise [McGrath et al. 1997]. As with voltage-mode APS architectures, FPN in current-mode architectures is a significant issue. However, developing effective FPN suppression techniques has proven more difficult however due to the non-linear relationship between signal charge and signal current in a current-mode architecture [McIlrath et al. 1997]. For this reason the author does not believe that current-mode APS sensors will play a significant role in the future of APS technology.

1-3.1.6 Alternative APS Technologies

To complete this discussion on APS technology it is necessary to mention a number of non-CMOS imaging architectures that have been developed that could also be described as active pixel sensors, namely the static induction transistor (SIT) [Nisizawa et al. 1979], the charge modulation device (CMD) [Nakamura et al. 1986], and the base stored image sensor (BASIS) [Tanaka et al. 1989]. The SIT, CMD, and BASIS devices all require additional processing steps during fabrication and can be considered proprietary technology in the same sense as CCD technology. While each of these architectures has potential advantages in terms of read-out sensitivity compared to CCD sensors, performance is limited at present by dark current, fixed-pattern noise, or image lag. Unless these technologies can demonstrate clear advantages over CCD technology, it is unlikely that they will be widely adopted.

1-3.2 State-of-the-Art Active Pixel Sensors

The APS architectures that are at present generating the most interest are those based on the voltage-mode photodiode and photogate active pixels. Sensors using these architectures have been successfully fabricated in a number of different CMOS fabrication processes [Dickinson et al. 1995a, Nixon et al. 1996b, Mendis et al. 1997b, Smith et al. 1997].The use of two levels of correlated-double sampling has been shown to substantially reduce fixed-pattern noise [Mendis et al. 1994a]. Furthermore many such sensors have integrated additional functionality such as analog-to-digital conversion onto the same die as the pixel array [Mendis et al. 1993a, Zhou et al. 1997]. Colour sensors have been demonstrated with a 1014×804 colour photodiode sensor being used in a consumer digital still camera [Hurwitz et al. 1997]. A 640×480 colour photodiode sensor with pixel dimensions of only $5.6\mu m \times 5.6\mu m$ has also been recently reported [Oba et al. 1997].

1-3.3 Open Research Issues

While CMOS APS image sensors are already finding their way into products, there are still important issues that remain open research questions. The most critical of these concern identifying the performance limitations of APS technology, the compatibility of APS with ongoing advances in CMOS fabrication technology, and the ability to manufacture highly integrated camera systems without performance degradation due to digital switching noise.

1-3.3.1 Identifying the Performance Limitations of APS Technology

At present there are questions regarding the level of image quality that can be delivered by a sensor manufactured in a standard digital CMOS process. While a number of researchers have reported various results, there has not yet been a detailed performance comparison between CMOS APS technology and CCD technology. In particular, the performance limitations of the present generation of APS image sensors have not been established. Available data suggests that currently CCD technology provides superior optical sensitivity and fixed-pattern noise performance. Furthermore, it has also been found that some CMOS fabrication processes produce image sensors with a large number of defective pixels due to high dark current levels [Loinaz 1996]. Without a detailed study comparing the performance of CMOS APS and CCD sensors, it is difficult to target where future improvements in image quality can be realized.

1-3.3.2 Compatibility with Standard CMOS

If a specialized CMOS fabrication process is required to address the performance limitations of APS sensors, then some of the perceived advantages of the technology will need to be re-assessed. Special fabrication requirements will clearly increase the investment required by companies wishing to use this technology to enter the image sensor market. A related issue concerns the longer-term compatibility of APS with the continual advancements in mainstream CMOS fabrication technology. Further research is required into how the performance of APS arrays will change as feature dimensions are scaled to deep sub-micron, or if mainstream CMOS moves towards a silicon-on-insulator (SOI) substrate [Wong 1996].

1-3.3.3 Camera System Integration

In addition to fundamental sensor performance issues there are also questions concerning large-scale camera system integration on the same die as the sensor itself. Although APS is promoted as being compatible with high levels of camera integration only a small number of true "single-chip cameras" have been developed to date [Loinaz et al. 1998a, Smith et al. 1998]. In particular, the potential for performance degradation due to coupling of digital switching noise into the analog circuits of the sensor through the substrate has not yet been investigated. This phenomenon has been observed with other mixed signal projects [Su et al. 1993, Blalack and Wooley 1995].

1-4. Contributions

This thesis addresses several important issues concerning the ability to produce highly integrated solid-state colour cameras in a standard CMOS fabrication process. Contributions claimed by the author are the following:

- Identifying the performance limitations of CMOS APS technology through the experimental evaluation of a colour photogate active pixel sensor.
- Demonstrating an integrated CMOS digital colour camera and quantifying the impact of digital switching noise on camera system performance.

1-4.1 Identifying CMOS APS Performance Limitations

A major contribution of this thesis is identifying and quantifying the performance limitations of CMOS APS technology through the experimental evaluation of a state-of-the-art colour photogate active pixel sensor.

1-4.1.1 CMOS APS Fixed-Pattern Noise Performance is Device Limited

It has been a widely held assumption that mismatch in the pixel and column read-out circuits is the factor limiting the fixed-pattern noise performance of CMOS image sensors, and that this provides the FPN advantage that CCD sensors hold over CMOS sensors. A major contribution of this thesis is demonstrating that with the use of two levels of correlated-double sampling all FPN in a CMOS APS sensor due to circuit mismatch is cancelled, and instead FPN performance is limited by dark current non-uniformity at low signal levels, and floating diffusion non-uniformity at high signal levels. This is significant because it establishes that the FPN performance of CMOS APS image sensors is device and not circuit limited, and that further advancements in FPN performance can only be achieved at the fabrication process level.

1-4.1.2 CMOS APS Temporal Noise Performance is Device Limited

It is shown that high conversion gain in the photogate pixel ensures that the temporal noise performance of the sensor is determined at the pixel level by photon shot noise, dark current shot noise, and charge transfer noise. Substantial advancements in temporal noise performance will only be achieved by improving the quantum efficiency, reducing dark current, and ensuring complete charge transfer within each pixel. To address each of these issues will require intervention at the fabrication process level.

1-4.1.3 CMOS APS Colorimetric Accuracy is Device Limited

The first reported investigation into the colorimetric performance of a CMOS APS sensor is presented. It is demonstrated that the colorimetric accuracy of the active photogate sensor is

limited by low quantum efficiency in the blue portion of the spectrum, and substantial pixel cross talk. Each of these shortcomings can only be addressed at the fabrication process level.

1-4.1.4 The Need for Non-Standard CMOS APS

It is argued that while there exists scope at the circuit level to increase the sensor saturation level and improve gain in the signal path, the critical sensor performance limitations in terms of temporal and fixed-pattern noise must be addressed at the device level. It is argued that present mainstream CMOS fabrication technology is only suitable for manufacturing APS image sensors intended for low-end solid-state imaging applications. To achieve image quality competitive with high-end CCD image sensors will require modifications to the standard CMOS fabrication process to reduce dark current and pixel cross talk, and improve sensor quantum efficiency. The performance of the next generation of CMOS APS sensors will be determined by the characteristics of new pixel structures that can be manufactured as part of a CMOS array.

1-4.2 APS Camera System Integration

The other major contribution of this thesis is the demonstration that complete camera system integration can be attained without loss of camera performance. This was shown through the development of an CMOS APS digital colour camera integrated on a single chip. The camera timing incorporates a sophisticated switching noise management strategy to investigate the coupling of digital switching noise into the analog circuits of the camera during sensitive operations such as sensor read-out and analog-to-digital conversion. Using this feature it was demonstrated that digital switching noise does not degrades camera performance in any measurable way, and that camera performance is only limited by that of the sensor. Consequently, future levels of camera system integration will be determined purely on an economic assessment of optimal system partioning.

1-5. Evolution

This thesis is largely the outcome of an invitation for the author to spend a year as a visitor in the DSP & VLSI Systems Research Department at Bell Laboratories, Holmdel, New Jersey. The author's interest in CMOS imaging led to his involvement in the CMOS camera project active in that department, and the development of a single-chip CMOS digital colour camera [Loinaz et al. 1998a]. On returning to the University of Adelaide the author investigated noise mechanisms in CMOS image sensors, and the application of colour science. During a second visit to Bell Laboratories an experimental evaluation of a colour CMOS photogate image sensor was performed. Analysis of this data enabled the performance limitations of the sensor to be quantified [Blanksby et al. 1997].

1-6. Collaboration with Co-workers

As much of the work that forms this thesis was performed in collaboration with a number of different co-workers, it is necessary to delineate their contributions from that of the author.

1-6.1 The Colour Photogate Image Sensor

The photogate image sensor described in Chapter 4 was designed by Sunetra Mendis, a former member of technical staff at Bell Laboratories, Holmdel NJ, and the fabrication of the colour filter array was managed by David Inglis of Bell Laboratories. The board used to characterize the sensor was designed by Marc Loinaz of Bell Laboratories. The measurements taken to characterize the photogate sensor where performed with the assistance of Marc Loinaz, with the exception of the quantum efficiency measurement which was performed by Iliana Fujimori of the Massachusetts Institute of Technology. The author developed the acquisition and analysis software and the theoretical models of sensor parameters. While discussions with Marc Loinaz contributed to the author's interpretation of the measurement data, the conclusions drawn are those of the author.

1-6.2 The Integrated CMOS Digital Colour Camera

The author devised the specification for the integrated camera described in Chapter 5 in consultation with the other group members at that time; Bryan Ackland, David Inglis, Marc Loinaz, and Joseph Worth, all of Bell Laboratories. The author developed the system level architecture of the single-chip camera and designed the digital subsystems, with the exception of the colour correction and image statistics subsystems which were developed jointly with K. J. Singh of Bell Laboratories. The synthesis of the camera digital system was performed by K. J. Singh. Marc Loinaz was responsible for the design of the camera analog system with contributions from David Inglis and Sunetra Mendis for the sensor array, and Kamran Azadet for the analog-to-digital converter. The full-custom SRAM used as part of the digital system was designed by Jay O'Neil of Bell Laboratories. Drafting assistance was provided by M. Zalonis, J. Bauman, and M. Hrubik, all of Bell Laboratories.

1-7. Thesis Structure

The thesis comprises six chapters and three appendices whose contents can be summarised as follows:

Chapter 1: Introduction

This chapter.

Chapter 2: Solid-State Imaging Technology

The basic principles of solid-state imaging are introduced and the architecture and operation of the most important CCD sensors and CMOS active pixel sensors are described. Non-idealities that limit the performance of solid-state image sensors are also discussed together with techniques available for managing them. The chapter concludes by emphasizing important differences in how high performance imaging can be achieved with CCD and CMOS technologies. This chapter contains material that can be considered prerequisite for Chapters 3, 4, and 5.

Chapter 3: Digital Camera Technology

Digital camera technology is introduced. Electronic display technology and colour science have a substantial influence on solid-state camera architecture and so are reviewed in detail. The system level requirements for realising a digital colour camera are described, and the implementation of digital cameras in terms of CCD and CMOS APS technology is discussed. This chapter contains material that can be considered prerequisite for Chapters 4 and 5.

Chapter 4: Performance Analysis of a Colour CMOS Photogate Image Sensor

A colour CMOS photogate active pixel sensor is experimentally evaluated and its performance is compared with other CMOS and CCD image sensors. The fundamental limitations of CMOS APS technology are identified and conclusions are made regarding the production of image sensors in CMOS.

Chapter 5: An Integrated CMOS Digital Colour Camera

The architecture and performance of an integrated CMOS digital colour camera is described. The single-chip camera features a sophisticated temporal sequencing scheme to determine the impact of digital switching noise on camera performance. It is shown that complete camera system integration and extremely low power dissipation can be achieved without degradation of camera performance.

Chapter 6: Conclusion

Conclusions are made concerning the development of integrated cameras using CMOS APS technology. Directions for further research are discussed.

Appendix A: Testing Environment for the Photogate Sensor

The digital acquisition system used to test the colour CMOS photogate image sensor is described together with the definitions of a number of metrics used by the author to characterize its performance.

Appendix B: Colorimetric Data and Methods for the Photogate Sensor

Tables of data and mathematical methods used to determine the colorimetric performance of the colour CMOS photogate image sensor are given.

Appendix C: Parameters of the Integrated Digital Colour Camera

The programming details of the parameters used by the single-chip CMOS digital colour camera are presented.

References

The references cited in the thesis are listed.

Colour Plates

A number of colour images are reproduced to demonstrate the performance achieved by the colour CMOS photogate sensor.

CHAPTER 2 Solid-State Imaging Technology

2-1. Introduction

This chapter introduces the basic principles of solid-state imaging, namely light as a stream of photons, the absorption of photons in a semiconducting substrate, the collection and integration of photon generated carriers, and signal read-out. CCD devices and the architecture and operation of CCD image sensors are reviewed, followed by that of the two most important CMOS active pixel sensor designs. A number of non-idealities that limit the performance of solid-state image sensors are described, together with techniques commonly used to manage them. The chapter concludes by emphasizing important differences in how high performance imaging can be achieved with CCD and CMOS technology. The material presented in this chapter can be considered prerequisite for Chapters 3, 4, and 5.

2-2. Fundamental Concepts of Solid-State Imaging

2-2.1 Light

Visible light consists of electromagnetic radiation in the portion of the spectrum which nominally ranges from 380nm to 780nm. Electromagnetic radiation with wavelengths immediately shorter or longer than this part of the spectrum are referred to as ultraviolet (UV) and infrared (IR) radiation, respectively. Although UV and IR do not play a significant role in human vision, IR is important in terms of its ability to stimulate silicon image sensors.

Due to the wave/particle duality of electromagnetic radiation it is also possible to consider light as a stream of particles known as *photons*. Each photon carries an elementary quantity of radiant energy of one frequency known as a quantum. The energy of a quantum E in *Joules* is

given by (2-1) where h is Planck's constant with a value of 6.63×10^{-34} Joules·second, and γ is the frequency in Hertz.

$$E = h\gamma \quad Joules \tag{2-1}$$

Alternatively E can be expressed in terms of the wavelength λ according to:

$$E = \frac{hc}{\lambda} \quad Joules \tag{2-2}$$

where c is the speed of light with a value of 3×10^{8} metres/second.

The photon concept plays an important role in explaining how solid-state materials interact with incident light.

2-2.2 Measuring Light

Two different systems are used to quantify light, namely the *radiometric* and *photometric* systems [Wyszecki and Stiles 1982, Hunt 1995].

2-2.2.1 The Radiometric System

The radiometric system measures light power in terms of the basic physical unit of power, the *Watt* where 1 Watt = 1 Joule/second. Radiometric quantities describe light power at a given wavelength. The corresponding spectral distribution function characterizes the variation of the radiometric quantity as a function of wavelength. The important radiometric quantities are given in the first column of Table 2-1 together with their units of measurement.

Radiometric	Photometric	Measures
radiant power P_e radiant flux F_e Watt (W)	luminous power P_v luminous flux F_v lumen (lm)	Light power emitted, transferred, or received through a surface.
radiant intensity I_e Watt per steradian (W/sr)	luminous intensity I_v candela (cd)	Light power emitted per unit solid angle.
radiance L_e Watt per steradian per square metre ($W/sr/m^2$)	luminance L_v candela per square metre (cd/m^2)	Light power emitted by unit solid angle per unit area of emitting surface.
irradiance E_e Watt per square metre (W/m^2)	illuminance E_v lux (lx)	Light power incident on a surface per unit area.

Table 2-1. Corresponding radiometric and photometric quantities.

2-2.2.2 The Photometric System

The photometric system measures light power in terms of its ability to stimulate the human visual system. It has been demonstrated that the perception of brightness for a human observer is not uniform for monochromatic stimuli of the same power across the range of the visible spectrum. The peak response of the human visual system occurs at about 555nm which is in

the yellow-green region of the spectrum and decreases for wavelengths both longer and shorter than this. The Commission Internationale de l'Eclairage (CIE) has empirically quantified this phenomena by defining the *spectral luminous efficiency function* $V(\lambda)$ for an observer with normal vision known as the *Standard Photometric Observer* [CIE 1957]. The spectral luminous efficiency function $V(\lambda)$ for normal, or *photopic*, viewing conditions is shown in Figure 2-1.

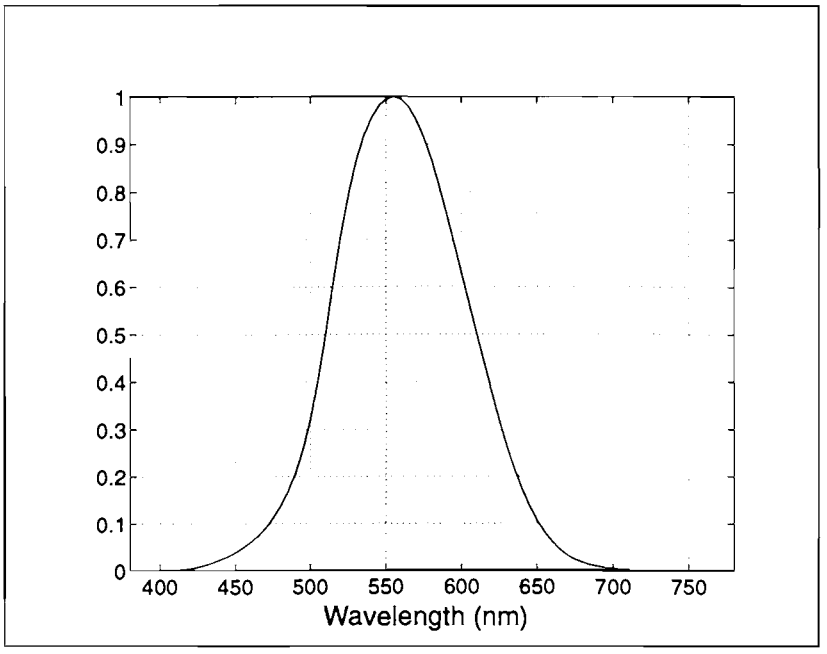


Figure 2-1. The spectral luminous efficiency function $V(\lambda)$ for photopic vision.

The spectral luminous efficiency function $V(\lambda)$ provides the link between the radiometric and photometric systems. Photometric quantities are related to the corresponding radiometric quantity by integration with the spectral luminous efficiency function $V(\lambda)$ over the visible portion of the spectrum, and multiplication by a constant K_m. The factor K_m is the *maximum luminous efficacy* and is equal to 683 lumens/Watt under photopic conditions. As an example (2-3) gives the relationship between illuminance E_v and irradiance E_e.

$$E_v = K_m \int_{\lambda} E_e(\lambda)\, V(\lambda)\, d\lambda \quad lux \tag{2-3}$$

Both the radiometric and photometric systems are used in quantifying the performance of solid-state imaging systems.

2-2.3 Photon Absorption

2-2.3.1 Generation of Electron-Hole Pairs

The light impinging on a solid-state image sensor can be considered in terms of a photon flux per unit area $\phi_0(\lambda)$ [1]. Incident photons that penetrate into the semiconducting substrate can transfer part of their energy to the substrate through the creation of electron-hole pairs as illustrated in Figure 2-2. This occurs when the energy of the photons given by (2-2) is greater than the bandgap of the semiconductor. For silicon substrates this occurs for photons with wavelengths shorter than 1000nm.

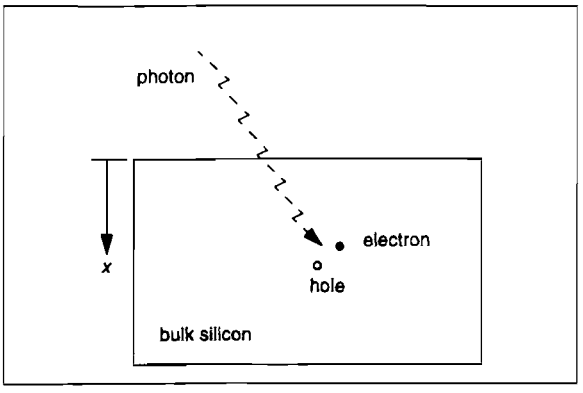


Figure 2-2. The generation of an electron-hold pair due to photon absorption at a depth x in a bulk silicon substrate.

2-2.3.2 Absorption Coefficient and Penetration Depth

The creation of electron-hole pairs reduces the magnitude of the incident light flux $\phi_0(\lambda)$ as a function of the depth x in the semiconducting substrate according to:

$$\phi(x, \lambda) = \phi_0(\lambda)\, e^{-\alpha(\lambda)x} \quad Watts/cm^2 \tag{2-4}$$

where $\alpha(\lambda)$ is the *absorption coefficient* of the substrate material [Theuwissen 1995].

The inverse of the absorption coefficient is known as the *penetration depth* $x^*(\lambda)$ which is defined as the depth at which the incident flux is reduced to $1/e$ or 37% of its original magnitude $\phi_0(\lambda)$. The absorption coefficient and penetration depth for a given material are both a function of wavelength. Example values for bulk silicon are given in Table 2-2 where it can be seen that the penetration depth for blue light is small while for infrared it is very large. The amount of charge generated in the substrate depends on the magnitude of the incident flux, its wavelength composition, and the absorption coefficient of the semiconductor.

1. This notation is used rather than E_e to be consistent with Theuwissen [Theuwissen 1995]. The units are Watts/cm^2. Note that the author has also chosen to explicitly show the wavelength dependence of this quantity.

Wavelength (nm)	Absorption Coefficient (cm^{-1})	Penetration Depth (μm)
400 (blue)	5×10^4	0.2
500 (green)	1×10^4	1
700 (red)	2000	5
1000 (infrared)	100	100

Table 2-2. Typical values for the absorption coefficient and penetration depth as a function of wavelength for bulk silicon [Theuwissen 1995].

2-2.4 Collection of Generated Carriers

2-2.4.1 Collection using a Depletion Region

To collect the photon generated carriers an electric field is required to separate the negatively charged electrons from the positively charged holes before recombination occurs. Most solid-state image sensors use the electric field of a depletion region to provide the collection site. Options include the depletion region formed by a reverse biased *p-n* junction diode, or the depletion region induced under a polysilicon gate with an appropriate voltage applied, as shown in Figure 2-3.

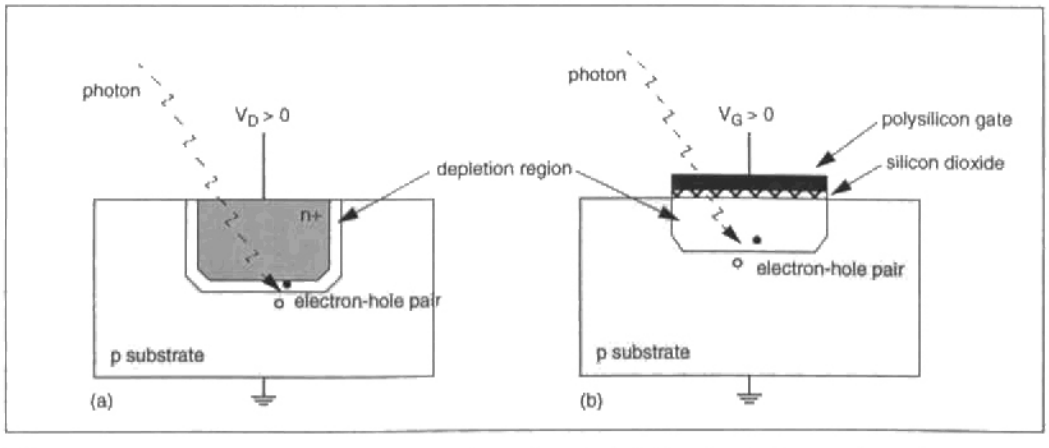


Figure 2-3. The collection of photon generated carriers in (a) the depletion region of a reverse biased *p-n* junction diode, and (b) the depletion region induced beneath a polysilicon gate.

2-2.4.2 Minority Carrier Diffusion

The dimensions and locality of the depletion region play an important role in the collection of photon generated carriers [Theuwissen 1995]. Minority carriers that are generated within the depletion region are collected with 100% efficiency. However, photons may also generate electron-hole pairs in the neutral bulk of the semiconductor substrate. To be collected by the depletion region the minority carriers must diffuse through the substrate toward the collection

site. Diffusion of minority carriers in a semiconducting substrate is characterized using the *diffusion length.* If the electron-hole pairs are formed at distances in excess of the diffusion length from the collection site they will be lost to recombination. As the wavelength of the incident light and the corresponding absorption coefficient determine the depth at which the electron-hole pairs are generated, the overall collection efficiency is highly wavelength dependent.

2-2.4.3 Charge Integration

The energy content of a single electron or hole is very small making it difficult to reliably transport to an output stage, or convert into a measurable quantity such as a current or voltage [Theuwissen 1994]. For this reason the photon generated carriers in a solid-state image sensor are locally integrated at the collection site for a certain time period to produce a charge packet. The *integration period* T_{int} is chosen to allow the collection of sufficient carriers for reliable charge read-out. For incident light of a given wavelength, the amount of charge collected is proportional to the magnitude of the light flux, and the duration of the integration period.

2-2.4.4 Quantum Efficiency

The total efficiency with which a solid-state sensor collects photon generated carriers at a given wavelength is described using the *quantum efficiency* $\eta(\lambda)$. The quantum efficiency is defined as the ratio of the number of carriers collected to the number of incident photons. For a uniform incident flux $\phi_0(\lambda)$ the number of photons impinging on each pixel in the sensor for a given wavelength during the integration period T_{int} can be calculated using:

$$N_{photons}(\lambda) = \frac{\lambda \phi_0(\lambda) A_{pixel} T_{int}}{h c} \quad photons \tag{2-5}$$

where A_{pixel} is the pixel area in square centimetres.

If the number of carriers collected by each pixel during the integration period for this flux is denoted $N_{signal}(\lambda)$, then the quantum efficiency $\eta(\lambda)$ is given by:

$$\eta(\lambda) = \frac{N_{signal}(\lambda)}{N_{photons}(\lambda)} \tag{2-6}$$

2-2.4.5 The Pixel Array

The charge collection and integration sites in a solid-state image sensor are known as *pixels.* The pixel designs employed with most solid-state image sensors are based on either the photodiode or photogate structures shown in Figure 2-3. To sample the image produced by the camera optical system the pixels are arranged in a two dimensional array. As the number of carriers collected in each pixel is proportional to the light impinging on it, the collected charge in each pixel constitutes a signal that represents the optical image.

2-2.4.6 Pixel Fill-Factor

In practical solid-state image sensors it is not possible to use all of the pixel area for the collection of photon generated carriers. For example, it is necessary to be able to physically isolate the charge packets collected in each pixel from those in neighbouring pixels. Furthermore, sensor architectures require the inclusion of additional device(s) in each pixel to enable the signal charge packet to be read-out from the pixel. The percentage of pixel area that is available for the collection of photon generated charge is known as the *fill-factor* or *aperture ratio* [Holst 1996, Theuwissen 1995].

2-2.5 Signal Read-out

2-2.5.1 Read-out Mechanisms

A solid-state image sensor must provide a means to convert the signal charge collected in each pixel into a voltage or current that can be measured at the sensor output. There are important differences in the way that signal read-out is accomplished in CCD and CMOS image sensors. In a CCD image sensor the charge collected in each pixel is transported to a common output stage to be converted into a voltage. The charge transport is effected using a large number of CCD stages. In contrast, CMOS image sensors do not perform charge transport at all. In a passive MOS sensor the charge collected at each pixel is sensed by the output stage across a column bus and converted into a voltage. CMOS active pixel sensors convert the signal charge into a voltage or current within the pixel itself, and this voltage or current is buffered and driven off-chip. The architecture and operation of CCD imagers and CMOS active pixel sensors will be described in more detail in Section 2-3 and Section 2-4, respectively.

2-2.5.2 Conversion Gain

The majority of solid-state image sensors employ voltage-mode read-out in which the signal charge is converted to a voltage prior to being driven off-chip. A quantity known as the *conversion gain* G is used to characterize the ability of a sensor to convert charge to voltage. The most common structure used for charge-to-voltage conversion is a capacitor. The voltage at the conversion node V_{CN} is related to the number of electrons N by:

$$V_{CN} = \frac{qN}{C_{CN}} \quad Volts \tag{2-7}$$

where C_{CN} is the capacitance of the conversion node and q is the electronic charge equal to 1.6×10^{-19} Coulombs.

The conversion gain, in volts per electron, at the node G_{CN} is given by:

$$G_{CN} = \frac{V_{CN}}{N} = \frac{q}{C_{CN}} \quad Volts/electron \tag{2-8}$$

To refer the conversion gain to the sensor output it must be multiplied by the combined gains of any circuits in the signal path between the conversion node and the sensor output A_0 to yield:

$$G = A_0 G_{CN} = \frac{qA_0}{C_{CN}} \quad Volts/electron \tag{2-9}$$

The conversion gain of a sensor is an important quantity because it relates the signal and noise components in terms of electrons, with the corresponding voltage magnitude of the components at the sensor output. For example, if the number of signal electrons is denoted N_{signal} then the signal voltage at the sensor output μ_{signal} is given by:

$$\mu_{signal} = G N_{signal} \quad Volts \tag{2-10}$$

Temporal and spatial variations in μ_{signal} and N_{signal} are usually defined in terms of standard deviations with units of Volts RMS and electrons RMS respectively. High conversion gain for a sensor is advantageous because it reduces signal-to-noise degradation by subsequent stages of signal processing [Theuwissen 1995]. This will be discussed further in Section 2-5.3.

2-2.5.3 Optical Sensitivity

The quantum efficiency $\eta(\lambda)$ of a sensor completely characterizes its optical performance. Equations (2-5) and (2-6) can be used to predict the number of signal electrons collected by each pixel N_{signal} for a given illuminant with flux $\phi_0(\lambda)$ using:

$$N_{signal} = \frac{A_{pixel} T_{int}}{hc} \int_{\lambda} \lambda \, \phi_0(\lambda) \, \eta(\lambda) \, d\lambda \quad electrons \tag{2-11}$$

where A_{pixel} is the pixel area, T_{int} is the integration period, and the integral is evaluated over all wavelengths λ for which the sensor quantum efficiency $\eta(\lambda)$ is non-zero. The mean signal voltage at the sensor output μ_{signal} can then be found using (2-10).

However, it is often more convenient to express the number of signal electrons as a simple function of a photometric quantity rather than as the integral of a radiometric quantity. The *optical sensitivity* of a solid-state image sensor is a measure of its response per unit exposure and integration time for a given source of illumination. If the sensor illuminance is given by E_v then the number of signal electrons can be found using:

$$N_{signal} = S_p E_v T_{int} \quad electrons \tag{2-12}$$

where S_p is defined as the mean optical sensitivity referred to the pixel.

The mean optical sensitivity S_p has units of electrons/lux·second, and describes the mean sensor response for a given illuminant. It implicitly includes the pixel area, the sensor quantum efficiency, and the spectral irradiance of the illuminant. To make fair comparisons between sensors based on the optical sensitivity requires that the illuminant used to determine S_p has the same or similar flux $\phi_0(\lambda)$. When reporting sensitivity data it is important to specify the illuminant.

The optical sensitivity is often quoted in Volts/lux·second at the sensor output rather than in electrons/lux·second at the pixel. If this formulation is denoted S_o then multiplying (2-12) by the sensor conversion gain G yields:

$$S_o = GS_p = \frac{\mu_{signal}}{E_v T_{int}} \quad Volts/lux \cdot second \tag{2-13}$$

2-3. CCD Image Sensors

In CCD image sensors the charge collected in each pixel is physically transported to a common output stage where it is converted into a voltage. The details of how this is achieved for a number of different CCD sensor architectures will now be discussed.

2-3.1 The Charge-Coupled Device

The Charge-Coupled Device (CCD) was invented by Boyle and Smith in 1970 [Boyle and Smith 1970]. The structure of a Surface channel CCD (SCCD) stage is shown in Figure 2-4(a) and consists of a polysilicon gate insulated from a silicon (Si) substrate by a thin layer of silicon dioxide (SiO_2). Most CCDs are manufactured on a p-type substrate so that electrons are the minority carriers. With the application of a positive gate voltage V_G electrons can be collected or stored by the CCD stage in the potential well established beneath the gate.

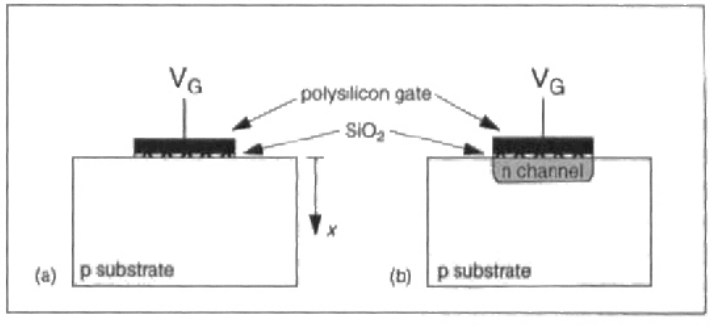


Figure 2-4. (a) A surface channel CCD (SCCD), (b) a buried channel CCD (BCCD).

2-3.1.1 The CCD Register

A CCD register is formed by spacing a number of CCD stages such that their potential wells overlap [Barbe 1975]. A number of different clocking strategies are available to allow charge to be transported along the register in a given direction including two-phase, three-phase, four-phase, and virtual phase schemes [Theuwissen 1995]. Charge transfer in a three-phase CCD register is illustrated in Figure 2-5. Separate charge packets can be transferred from left to right using the timing shown. As discussed in Section 1-2.1 the performance of a CCD register is characterized in terms of the *charge transfer efficiency* ζ, the fraction of each charge packet successfully transferred from one stage to the next.

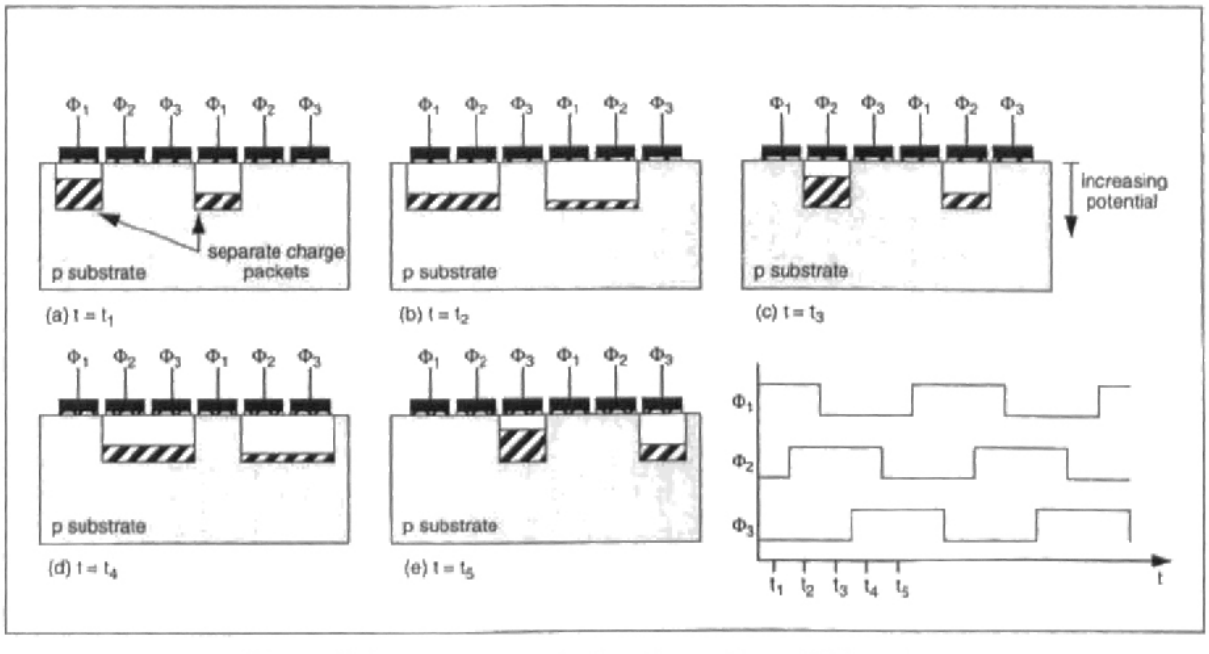


Figure 2-5. Charge transfer in a three-phase CCD register.

2-3.1.2 The Buried Channel CCD

Although diagrams such as Figure 2-5 are by convention drawn with the direction of increasing potential into the substrate, in reality the greatest potential occurs near the substrate surface. Therefore in a surface channel CCD the charge packets are transferred along the Si-SiO_2 interface as illustrated in the potential diagram of Figure 2-6(a). However, defects in the silicon crystal structure at this interface randomly trap and release electrons from the signal charge packets and degrade the charge transfer efficiency of such devices.

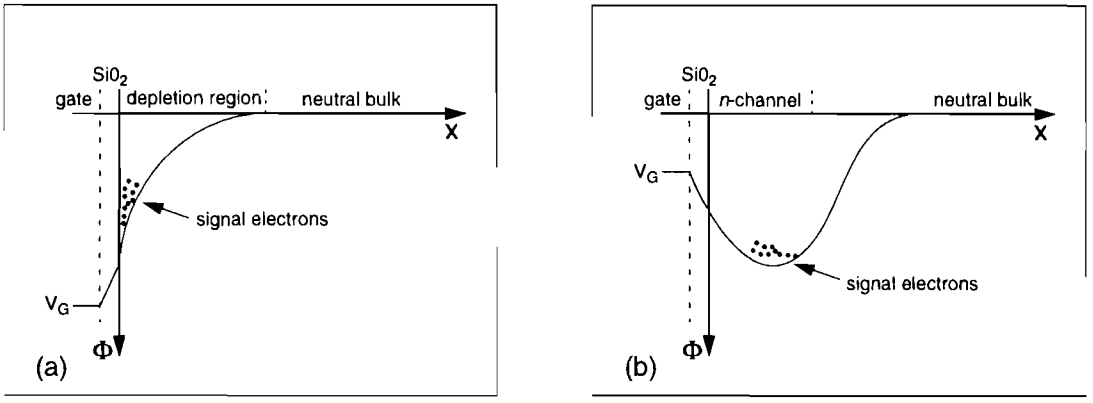


Figure 2-6. Potential diagrams of (a) a SCCD and (b) a BCCD corresponding to Figure 2-4(a) and (b) respectively. The potential is denoted Φ and the depth into the device is denoted by *x*.

To address this problem the buried channel CCD (BCCD) was developed [Walden et al. 1972]. As shown in Figure 2-4(b) an additional *n*-type implant is introduced to the CCD structure that is doped such that it remains fully depleted during CCD operation. The ionized positive ions of the n-channel transform the positive gate voltage V_G to a greater channel potential in the silicon. As illustrated in Figure 2-6(b) this results in the maximum of the potential well occurring deeper in the substrate and away from the Si-SiO_2 interface. This substantially improves the charge transfer efficiency as charge packets have less opportunity to interact with the interface states. Furthermore the charge transfer speed is increased due to greater fringing fields. While there is some loss in charge capacity when compared to the SCCD, the advantages of high charge transfer efficiency and transport speed mean that all modern CCD sensors use buried channel devices [Theuwissen 1995].

2-3.2 Frame-Transfer CCD

2-3.2.1 The CCD as a Charge Collection Site

In addition to charge transport, a CCD stage can also be used to collect photon generated charge in the manner shown in Figure 2-3(b). This allows a linear solid-state image sensor to be formed from a multi-phase CCD register. For example a three-phase CCD register configured as an image sensor is shown in Figure 2-7. Each pixel consists of three CCD stages. Dur-

ing charge integration Φ_1 and Φ_2 are held at a positive voltage and photon generated electrons are collected in the potential well. During the integration period Φ_3 is held at ground or a negative voltage to isolate the charge packet from that collected by neighbouring pixels. At the conclusion of the integration period the charge packets can be shifted to an output stage using the timing shown in Figure 2-5.

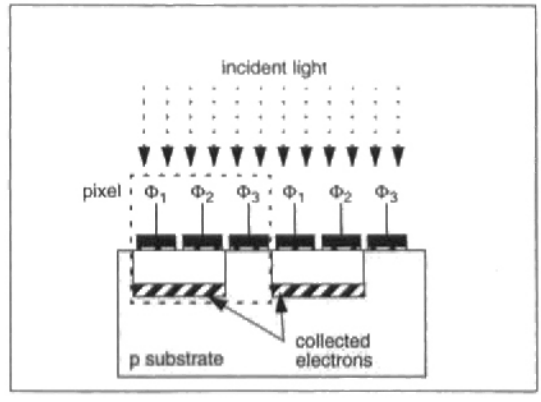


Figure 2-7. Using a three-phase CCD register as a linear image sensor.

2-3.2.2 Frame-Transfer Architecture and Operation

The frame-transfer (FT) CCD is a two dimensional image sensor based on this principle. The architecture of a FT sensor is shown in Figure 2-8 [Schaeffer et al. 1994]. It consists of a series of vertical CCD registers terminating in a horizontal CCD register with an output stage. Half of the sensor is shielded from light to form a temporary storage array. After integration the charge packets collected in the photosensitive portion of the sensor are transferred to the shielded storage area. Once the entire image has been transferred to the storage section, the transport of the charge packets to the output stage can commence. During this operation the charge packets corresponding to an image row, but in different vertical CCD registers, are transferred in turn to a single horizontal CCD register. After each row is loaded into the horizontal CCD register the charge packets are shifted to the output stage where they are converted into a voltage. While this read-out operation is occurring the photosensitive portion of the array can be integrating the next image. Hence the storage array allows the timing of the photosensitive array to be independent of the timing of the video read-out.

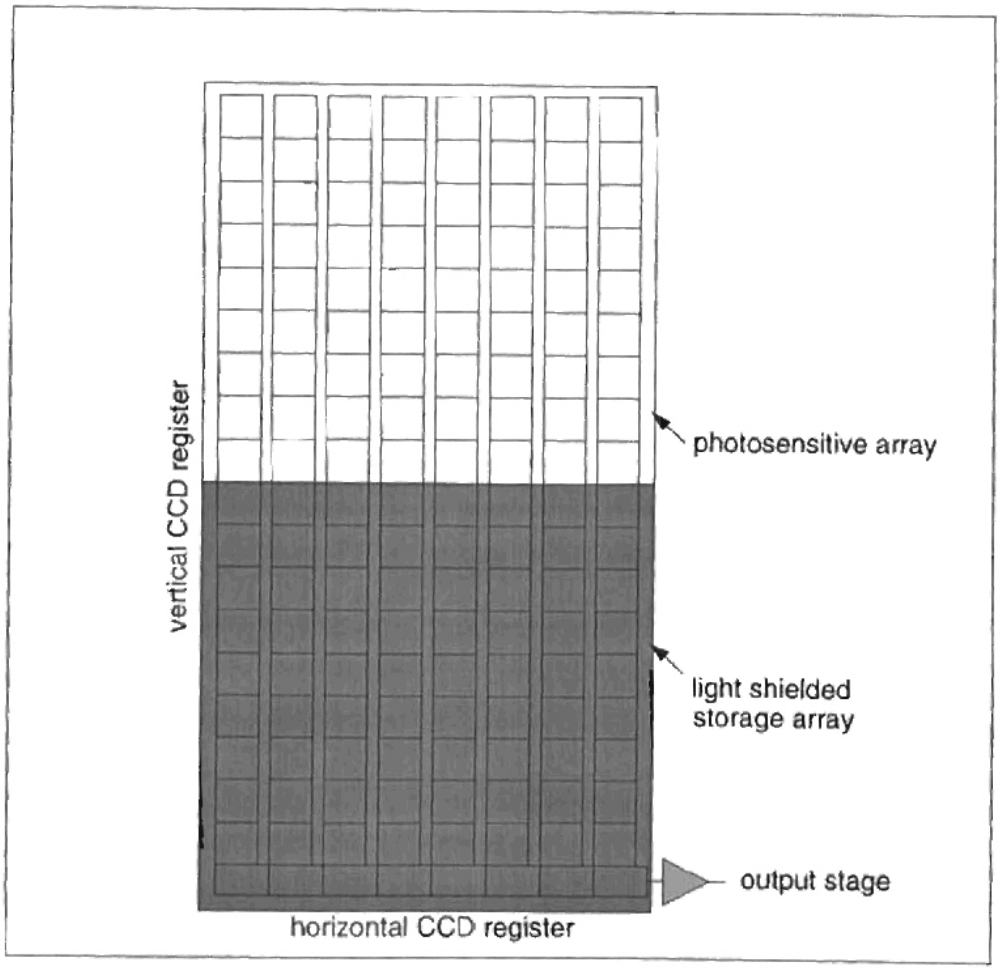


Figure 2-8. Architecture of a frame-transfer CCD.

2-3.2.3 Performance Characteristics of a Frame-Transfer CCD

The transfer of the image from the photosensitive array to the storage array must be performed as quickly as possible to reduce *smear*. Smear is produced by the photon generated charge collected by the pixels during the transfer operation. This unwanted charge is added to and corrupts the charge packets that represent the image formed during the integration period. Smear can also be minimized by the use of a mechanical shutter.

As the charge collection sites in a frame-transfer CCD are also used for charge read-out, the frame-transfer architecture allows a fill-factor of close to 100% to be realized. However, this advantage is offset by the absorption of photons in the polysilicon gates that define each CCD stage. The absorption is significant for short wavelengths and results in low quantum efficiency in the blue portion of the visible spectrum [Bosiers et al. 1991]. High end frame-transfer CCDs address this problem by thinning the substrate and exposing the backside of the sensor to the incident illumination [Levine et al. 1994, Holland et al. 1997]. While this technique provides substantial gains in quantum efficiency it makes the sensor more mechanically fragile [Holst 1996].

2-3.3 Interline-Transfer CCD

2-3.3.1 The Interline-Transfer Pixel

The pixel design used in an interline-transfer (IL or IT) CCD consists of a photodiode and a BCCD stage. An optically opaque material is used to provide a photoshield for the BCCD. A simplified cross-section of such a pixel is shown in Figure 2-9(a).

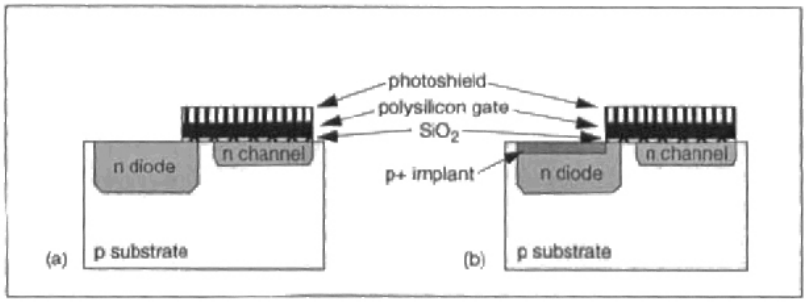


Figure 2-9. Simplified (a) photodiode, and (b) pinned photodiode pixel structures used in IL-CCDs.

Photon generated carriers are collected in the depletion region of the *p-n* photodiode during integration. At the start of image read-out the collected charge is transferred into the adjacent BCCD stage. However, for the pixel structure shown in Figure 2-9(a) a fraction of the charge is not successfully transferred to the BCCD stage and remains in the depletion region of the diode. This causes a phenomenon known as *image lag* where the image produced by the sensor is corrupted by charge collected during previous integration cycles. To address this problem a *p+* implant is normally used to modify the potential profile of the photodiode to ensure complete charge transfer [Teranishi et al. 1982, Stevens et al. 1991]. The resulting diode is known as a *pinned* photodiode because the *p+* implant pins the potential at the surface of the photodiode to that of the *p*-substrate. This also reduces dark current which will be discussed further in Section 2-5.1.5 Furthermore, the *p+* implant provides an additional depletion region in the pixel and so increases the charge storage capacity of the photodiode. A simplified cross-section of such a pixel is shown in as shown in Figure 2-9(b). Other variations on this basic pixel structure are also used [Ozaki et al. 1994].

2-3.3.2 Interline-Transfer Architecture and Operation

The architecture of an interline-transfer CCD is shown in Figure 2-10. It consists of a series of vertical CCD registers and photodiodes terminating in a horizontal CCD register with an output stage. On the commencement of sensor read-out the charge packets collected in the photodiodes are transferred into the adjacent CCD stages. Once this transfer is completed the transport of the charge packets to the output stage can commence. During this operation the charge packets corresponding to an image row, but in different vertical CCD registers, are transferred in turn to a single horizontal CCD register. After each row is loaded into the hori-

zontal CCD register the charge packets are shifted to the output stage where they are converted into a voltage.

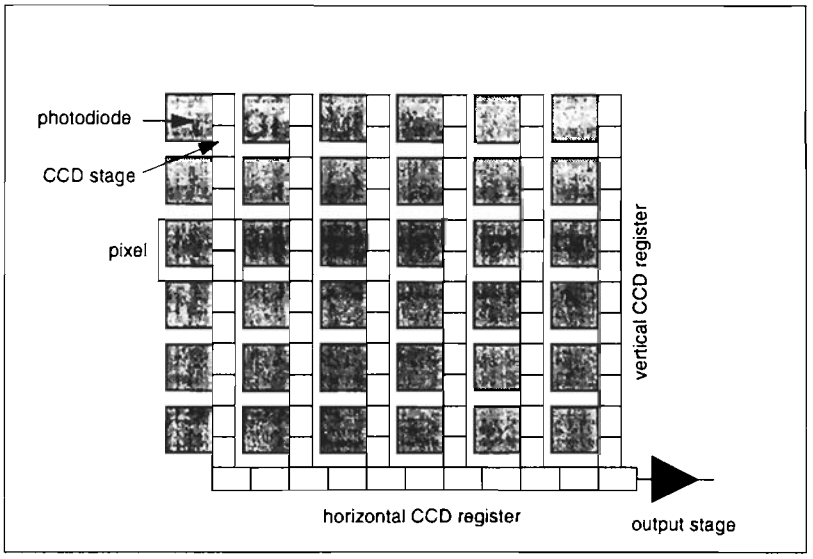


Figure 2-10. Architecture of an interline-transfer CCD image sensor.

2-3.3.3 Performance Characteristics of an Interline-Transfer CCD

Unlike the photogate structure employed by the FT-CCD, the photodiodes used with the IT-CCD provide high quantum efficiency across the visible spectrum. However, the inclusion of the vertical CCD stages in the pixel significantly reduces the pixel fill-factor which can be as low as 25%. For this reason microlenses are widely used with IT-CCDs and will be discussed further in Section 2-5.3.2 [Nishima et al. 1995].

The IT-CCD is also subject to smear, but from a different mechanism than that responsible for smear in the FT-CCD. Smear in an IT-CCD is caused by photon generated carriers being collected by the CCD stage rather than the photodiode. This may be due to the diffusion of carriers through the substrate, or stray photons introduced through light piping[1] that generate carriers in the CCD [Theuwissen 1995]. Smear can be reduced through the use of additional implants in the pixel design, optimizing the photoshield, and increasing the read-out speed. This last factor led to the development of the frame-interline transfer CCD.

2-3.4 Frame-Interline Transfer CCD

The frame-interline transfer (FIT) CCD is an interline-transfer CCD with the addition of a shielded storage array as used with a frame-transfer CCD [Morimoto et al. 1995]. After integration the charge packets from each pixel are transferred into the vertical CCD registers and

1. Light piping is a lateral scattering of photons caused by multiple internal reflections at the interfaces of layers deposited on the substrate surface such as the colour filter array or the SiO_2 layer.

rapidly transported to the storage array. As this operation occurs quickly it significantly reduces the level of smear when compared to the interline-transfer architecture. The read-out of the charge packets from the storage array to the output stage is identical to that used with the FT-CCD architecture.

2-3.5 The CCD Sensor Output Stage

All CCD sensors require an output stage to convert the signal charge packets into a current or voltage that can be measured externally. Most output stages used in CCD sensors perform charge-to-voltage conversion, the most common structure employed being the floating diffusion with reset [Theuwissen 1995].

2-3.5.1 Floating Diffusion with Reset

The structure and operation of floating diffusion with reset output stage is shown in Figure 2-11 at the end of a three-phase CCD register. It consists of a DC-biased output gate and an $n+$ floating diffusion node *FD*. The capacitance of the floating diffusion node converts the charge packets into a voltage. A reset device enables the floating diffusion node to be returned to a known potential prior to the read-out of each charge packet.

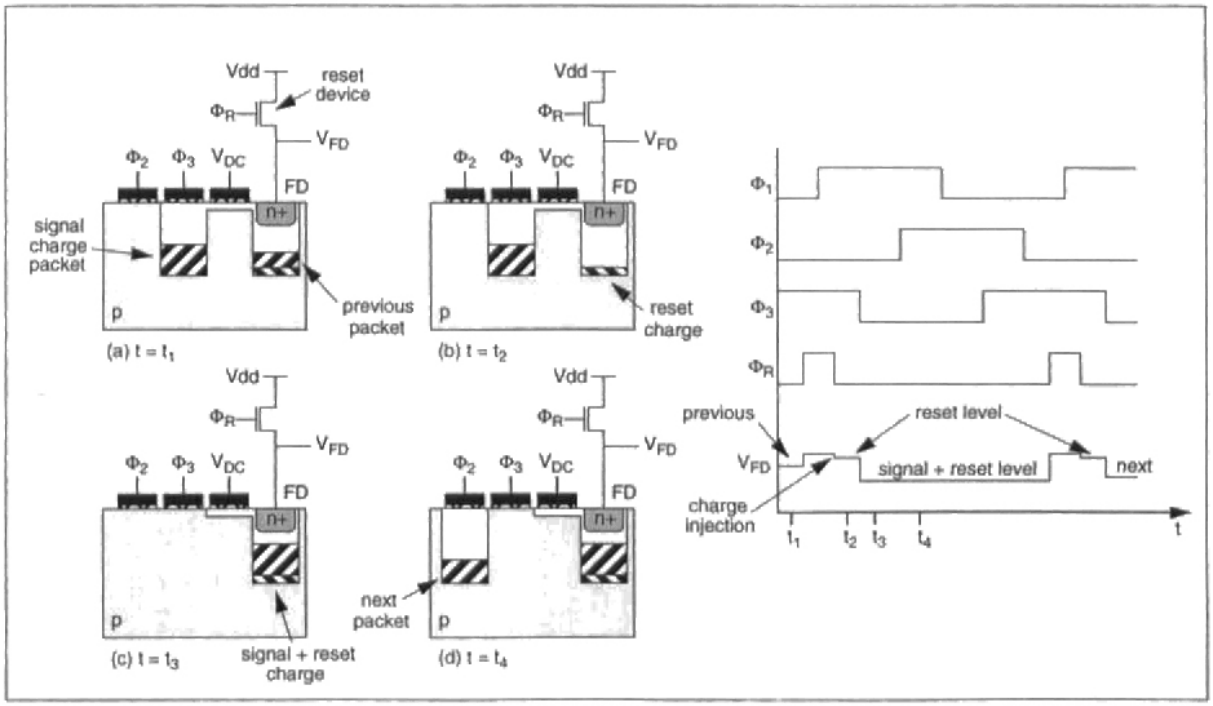


Figure 2-11. Operation of a floating diffusion (FD) with reset output stage at the end of a three-phase CCD register.

The operation of the output stage can be explained with the aid of Figure 2-11. At time t_1 the signal charge packet is stored underneath Φ_3. To reset the floating diffusion node Φ_R is then driven high and the voltage of the floating diffusion node V_{FD} takes on a value approximately

a threshold voltage drop below Vdd. When Φ_R is driven low at the end of the reset operation, V_{FD} drops slightly due to charge injection through the reset device. At time t_2 the reset operation has been completed and the voltage on the floating diffusion node V_{FD} is at the reference level. At time t_3 Φ_3 is driven low and the signal charge packet is transferred through the DC-biased gate and onto the floating diffusion node. Due to the capacitance of the floating diffusion node C_{FD} the voltage V_{FD} is displaced in proportion to the number of carriers in the charge packet. This voltage swing constitutes the signal. Time t_4 illustrates the arrival of the next signal charge packet.

2-3.5.2 Source-Followers

To buffer the voltage on the floating diffusion node and allow the sensor to drive the subsequent stages of signal conditioning circuits, a number of source-follower stages are normally used in the output stage [Schaeffer et al. 1994]. A typical arrangement of three cascaded source-followers is shown in Figure 2-12.

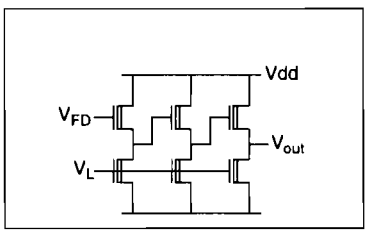


Figure 2-12. Source-follower arrangement used in a typical CCD output stage.

While the source-followers used in the output stage provide a necessary buffering function, they reduce the signal voltage swing at the sensor output. For example, the combined gain of the source-followers in a CCD output stage A_{SF} is normally in the range 0.5 to 0.9 [Levine et al. 1994, Theuwissen 1995]. In addition the source-followers introduce a number of temporal noise components including thermal noise and 1/f noise. Careful design of the transistor dimensions is required to ensure that the noise contribution of the source-followers is minimized [Centen 1991].

2-3.5.3 Conversion Gain

The conversion gain at the floating diffusion node G_{FD} is given by:

$$G_{FD} = \frac{V_{FD}}{N} = \frac{q}{C_{FD}} \quad Volts/electron \tag{2-14}$$

To refer the conversion gain to the sensor output it must be multiplied by the combined gains of the source-followers in the output stage A_{SF} to yield:

$$G = A_{SF}G_{FD} = \frac{qA_{SF}}{C_{FD}} \quad Volts/electron \tag{2-15}$$

It is difficult to achieve high conversion gain using the floating diffusion with reset output stage presented in this section. This is because the capacitance of the floating diffusion node C_{FD} is the total capacitance of this node, and includes parasitic capacitance such as the gate capacitance of the first source-follower stage. Typical values of conversion gain for output stages employing the floating diffusion with reset structure are in the range $3\mu V/electron$ to $15\mu V/electron$ [Stevens et al. 1991, Kamasz et al. 1994]. Values of conversion gain greater than $20\mu V/electron$ can be achieved by reducing the dimensions of the floating diffusion node or using feedback [Akimoto et al. 1991, Itakura et al. 1995].

2-3.5.4 Reset Noise

Whenever a capacitor is charged or discharged through a resistor, an uncertainty is introduced to the charge stored in the capacitor and the voltage drop across it. This phenomenon is known as *reset noise* and the RMS variation in the number of charge carriers stored in the capacitor n_{reset}, and voltage across the capacitor σ_{reset} are given by:

$$n_{reset} = \frac{\sqrt{kTC}}{q} \quad electrons\ RMS \tag{2-16}$$

$$\sigma_{reset} = \sqrt{\frac{kT}{C}} \quad Volts\ RMS \tag{2-17}$$

where k is Boltzmann's constant, T is the temperature in Kelvin, and C is the capacitance.

The reset operation applied to the floating diffusion capacitance C_{FD} each read-out cycle is via the resistive channel of a MOSFET. As a consequence a reset noise component is always included in the floating diffusion reset level. This uncertainty in the reset level is added to the signal charge packet when it is transferred to the floating diffusion node, and reflected in the output voltage by the sensor conversion gain and its magnitude can be significant. For example, given a sensor with a value of $C_{FD} = 16fF$ and $A_{SF} \sim 1$, at room temperature the reset noise is greater than 50 *electrons RMS* at the floating diffusion node, and $0.5mV$ *RMS* at the sensor output. However it is possible to cancel reset noise with a signal processing technique known as *correlated-double sampling*, or through the use of alternative output structures that enable complete reset of the charge-to-voltage conversion node [White et al. 1974, Mutoh et al. 1991].

2-3.5.5 Correlated-Double Sampling

Correlated-double sampling (CDS) is a post-processing technique for cancelling reset noise by measuring its value each read-out cycle and subtracting it from the signal. CDS also removes part of the $1/f$ noise contributed by the source-followers. A circuit for performing CDS is shown in Figure 2-13 and its operation can be described as follows. At time t_2 in each read-out cycle the reset level, including the reset noise contribution, is sampled on a capacitor by the switch SH1. At time t_3 the combined signal and reset level is sampled on a separate capacitor by the switch SH2. The voltage at the output of the differential amplifier gives the signal voltage with the reset level and reset noise removed.

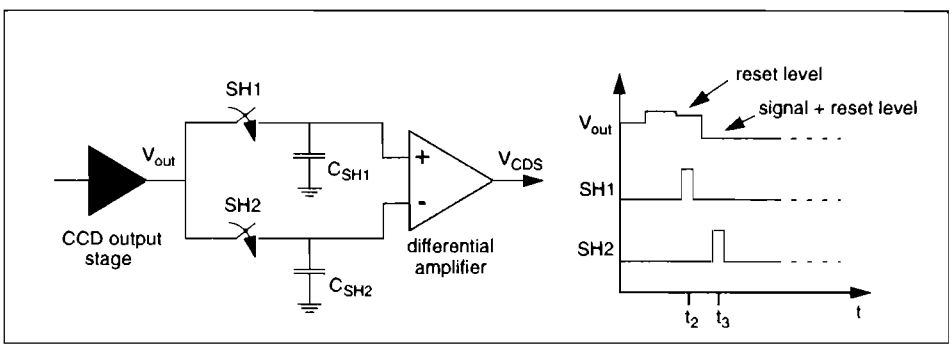


Figure 2-13. A correlated-double sampling (CDS) circuit. The timing is consistent with Figure 2-11.

2-3.5.6 Read Noise

While the use of source-followers and correlated-double sampling are necessary, they introduce additional temporal noise to the signal. For example the source-followers and the CDS differential amplifier generate thermal noise and $1/f$ noise, and the sampling operations performed as part of CDS fold any noise components with frequencies exceeding the Nyquist limit into the baseband [Theuwissen 1995]. The temporal noise contributions from all circuits involved in sensor read-out are collectively known as *read noise* $\sigma_{t_{read}}$ Read noise usually determines the temporal noise floor of a CCD sensor and is typically in the range of 10 *electrons RMS* to 30 *electrons RMS* referred to the floating diffusion node [Stevens et al. 1991, Schaeffer et al. 1994]. To minimize read noise requires careful optimization of the output stage [Centen 1991].

2-3.5.7 Parallel Output Stages

High resolution and/or high frame rate CCD arrays make the design of the sensor output stage particularly demanding. As the bandwidth requirements of the output stage increase, so does the read noise. To address these issues it is possible to use a number of parallel output stages for sensor read-out [Bosiers et al. 1991, Kamasz et al. 1994]. For this strategy to be successful it is necessary to ensure that the output stages are well matched so as not to introduce fixed-pattern noise [Morimoto et al. 1995].

2-4. CMOS Active Pixel Sensors

Unlike CCD image sensors, pixel read-out in CMOS sensors is effected at the circuit level rather than the device level. However, the performance of CMOS image sensors is limited by fixed-pattern noise (FPN) far in excess of that found in CCD sensors [Ozaki et al. 1991]. This is caused by mismatch between read-out circuits due to fabrication variations. Furthermore, the temporal noise performance of passive CMOS imagers is limited by reset noise introduced when the column capacitance is reset. The advent of CMOS active pixel sensors (APS) has enabled improved temporal and fixed-pattern noise performance to be achieved. The two CMOS APS architectures that have been most successful in this regard are the active photogate and active photodiode image sensors. The architecture of the photogate and photodiode active pixel sensors support effective FPN suppression at the circuit level based on correlated-double sampling (CDS). Typically the read-out circuits used with the photogate and photodiode APS arrays are identical, with only the control signal timing and pixel designs themselves being different. The architecture and operation of the photogate and photodiode active pixel sensors will now be discussed.

2-4.1 Photogate Active Pixel Sensor

2-4.1.1 The Photogate Active Pixel

The earliest photogate active pixel design is known as the double-poly photogate pixel and is shown in Figure 2-14(a) [Mendis et al. 1993b]. It consists of a polysilicon photogate *PG*, an overlapping transfer gate *TX* formed in a second polysilicon layer, a floating diffusion node *FD*, a reset device *M2*, an active device *M3*, and an access device *M4*. The pixel output node P_{OUT} is connected to a common column bus which is terminated by a bias device *M5* shown in Figure 2-14(c). During integration the photogate *PG* is used to create a potential well for the collection of photon generated carriers with the application of a positive voltage *Vdd*. A small positive voltage on the *TX* gate isolates the collected carriers under *PG* from the floating diffusion node *FD*. Prior to read-out the *FD* node is reset by *M2*. To effect read-out the *PG* voltage is taken low and the collected electrons are transferred to the *FD* node via the *TX* gate and converted into a voltage. When the pixel is selected by driving *SEL* high, the active device *M3* forms part of a distributed source follower with *M5* and buffers the voltage on the *FD* node onto the column bus. The architecture of the double-poly photogate pixel can be considered as a single CCD gate and output stage within a pixel. However, the double-poly photogate pixel can only be manufactured in a CMOS process that provides two polysilicon layers, such as those specialized for analog CMOS design. To achieve compatibility with a standard digital CMOS fabrication process, a single-poly photogate pixel was developed and is shown in Figure 2-14(b) [Mendis et al. 1994a, Dickinson et al. 1995a]. The operation of the single-poly

pixel is identical except electron transfer between the potential well beneath *PG* and the *FD* node now occurs via the transistor action of device *M1* biased with a small positive voltage on *TX*. However, unlike the double-poly pixel complete charge transfer between the *PG* gate and the *FD* node is not possible and the single-poly pixel suffers from image lag [Dickinson et al. 1995b]. This phenomenon and its implications will be discussed in more detail in Section 4-9.

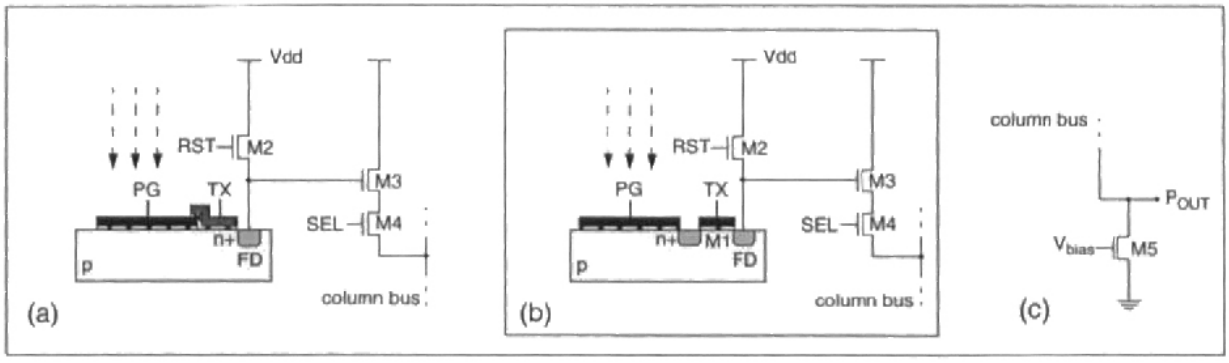


Figure 2-14. The (a) double-poly photogate pixel, (b) single-poly photogate pixel, and (c) column bias device.

2-4.1.2 Photogate APS Architecture with Correlated-Double Sampling

The architecture of an image sensor using the single-poly photogate pixel is shown in Figure 2-15. The same architecture has been used with double-poly photogate pixel [Mendis et al. 1994a].

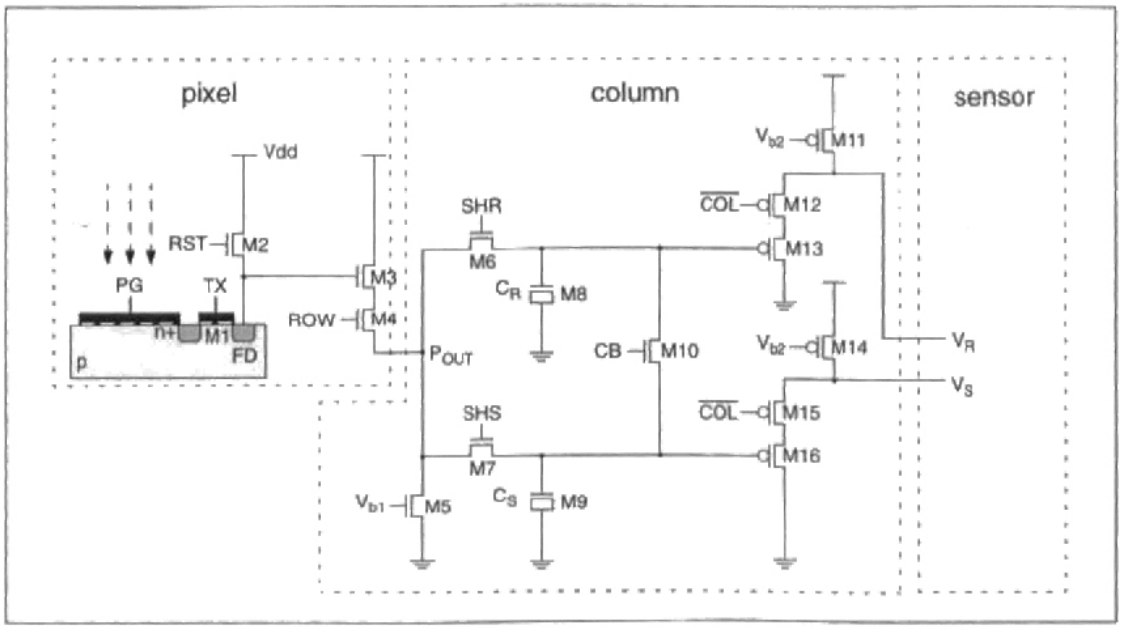


Figure 2-15. Photogate active pixel sensor architecture.

The architecture of Figure 2-15 supports two levels of correlated double-sampling (CDS) to cancel device mismatch that causes FPN at both the pixel and column level. In addition to the

circuits given in Figure 2-15, a configuration of differential amplifiers and sample-and-hold stages shown in Figure 2-16 are required. These circuits can be integrated as part of the sensor [Loinaz et al. 1998a].

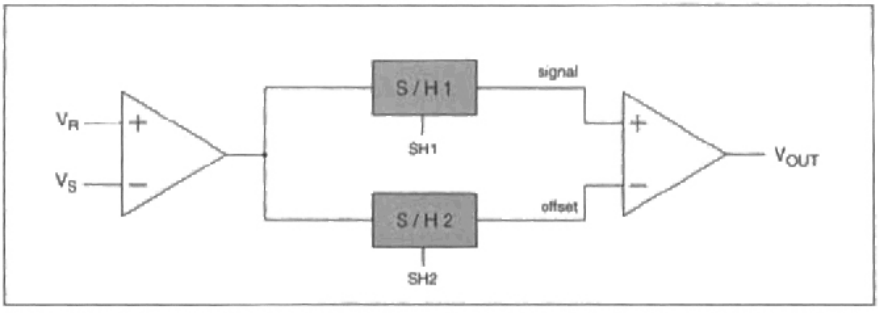


Figure 2-16. Additional circuitry required for correlated double sampling.

2-4.1.3 Photogate APS Operation

The operation of the photogate image sensor with CDS can be explained with the aid of the timing diagram shown in Figure 2-17. During integration the polysilicon photogate *PG* is held at *Vdd* and photon generated electrons are collected in the potential well beneath the gate. The transfer device *M1* is biased at a small positive voltage, isolating the collected charge under the photogate from the floating diffusion node *FD*.

For sensor read-out each row is addressed in turn with the row decoding logic (not shown in Figure 2-15) driving the appropriate row line *ROW* to *Vdd*. The *FD* node of the pixels in the row are reset to a voltage approximately one threshold voltage drop below *Vdd* by pulsing *RST*. The reset operation introduces uncertainty into the *FD* reset level due to reset noise and the threshold voltage drop across *M2*. The reset level is buffered by the source follower formed by devices *M3-M5* and is sampled on the gate capacitance C_R by pulsing *SHR*. Electrons collected under the photogate are then transferred to the *FD* node via device *M1* by pulsing *PG* to ground. The signal electrons displace the *FD* voltage and this level is sampled on the gate capacitance C_S by pulsing *SHS*. The sampling of the pixel reset and signal levels by the column circuits is carried out in parallel for the pixels in the selected row. This typically occurs in the line blanking or horizontal synchronization period. To generate the image signal each column of the sensor is then addressed in turn by the column decoding logic (not shown in Figure 2-15) by driving the $\overline{COL}$ signal to ground. The column source followers formed by devices *M11-M16* buffer the sampled reset and signal levels onto common buses denoted V_R and V_S respectively. To perform the first stage of CDS the first differential amplifier in Figure 2-16 subtracts the signal and reset levels. This removes the reset noise component and pixel offset mismatch due to threshold voltage variations in devices *M2*, *M3*, and *M4*. The signal level is stored in a sample-and-hold stage S/H1 by pulsing *SH1*. To perform the second level of CDS, sometimes referred to as *crowbar* [Mendis et al. 1994a], the *CB* signal is driven high and the

first differential amplifier forms the offset difference of the column source follower devices *M13* and *M16*. This offset is stored in a second sample-and-hold stage S/H2 by pulsing *SH2*. A final differential amplifier delivers the image signal V_{OUT} with column offsets removed that can be sampled or digitized on the rising edge of the pixel clock *PCLK*.

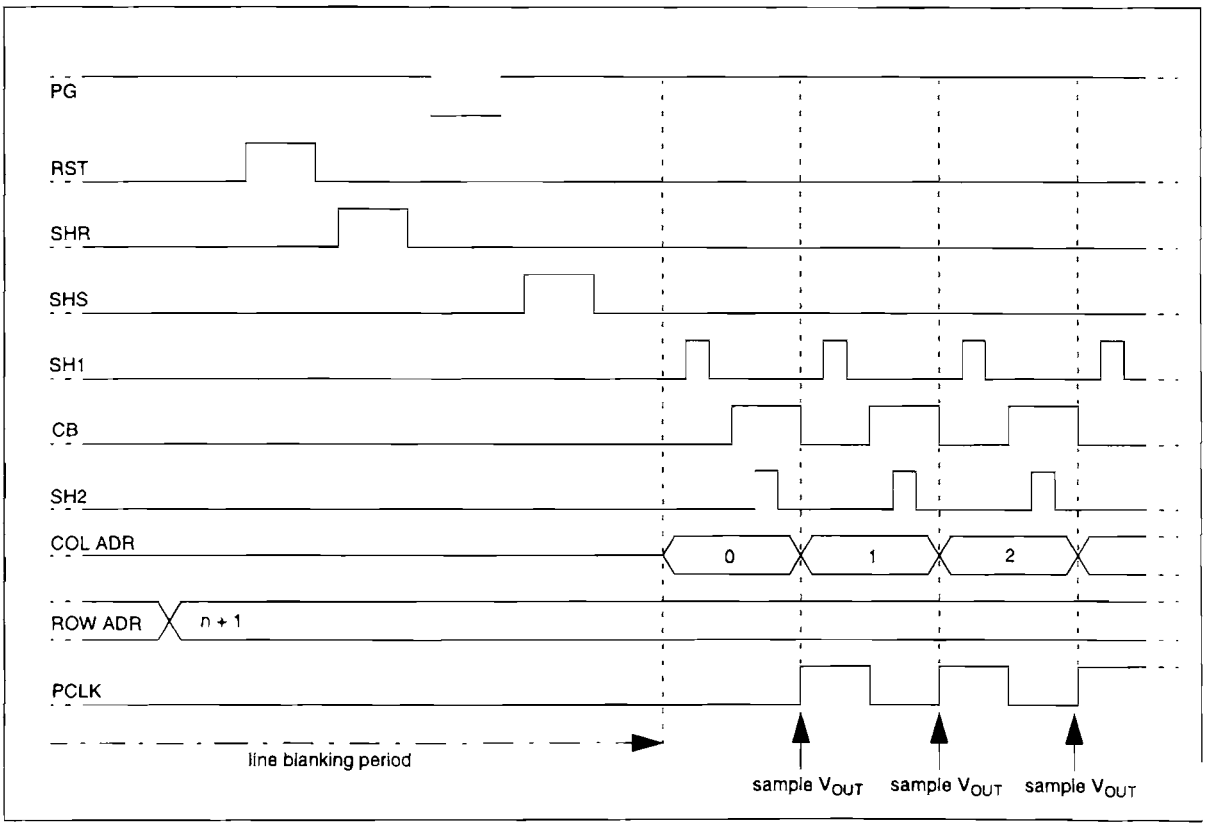


Figure 2-17. Timing diagram for the photogate active pixel sensor.

2-4.1.4 Photogate Conversion Gain

The conversion gain G of the photogate APS sensor is determined by the parasitic capacitance of the *FD* node in the pixel C_{FD}, and the combined gain of the source followers used in the read-out circuits A_{SF} according to:

$$G = A_{SF}G_{FD} = \frac{qA_{SF}}{C_{FD}} \quad Volts/electron \tag{2-18}$$

where G_{FD} is the conversion gain of the pixel floating diffusion node itself.

If minimum sized transistors are used in the pixel design, the conversion gain in the photogate pixel G_{FD} is very high as the *FD* capacitance is very small. However, the combined gain of the pixel and column source followers may range from 0.4 to 0.7 and therefore values for the conversion gain referred to the sensor output G are typically in the range 15 to 30 $\mu V/electron$ [Nixon et al. 1996b, Blanksby et al. 1997]. However, values as high as

43 $\mu V/electron$ have recently been reported for sensors fabricated in a 0.35μm CMOS process [Mendis et al. 1997b]. The conversion gain of the photogate APS sensor is higher than that achieved by the output stage of CCD sensors and so provides greater immunity from image SNR degradation by subsequent stages of processing. Furthermore, as the highest gain is provided in the pixel itself, the read noise contribution from the sensor read-out circuits to the SNR is also minimized.

2-4.2 Photodiode Active Pixel Sensor

2-4.2.1 The Photodiode Active Pixel

The basic photodiode active pixel is shown in Figure 2-18(a) [Nixon et al. 1995]. It consists of a photodiode that also acts as the floating diffusion node *FD*, a reset device *M2*, an active device *M3*, and an access device *M4*. Prior to integration the photodiode is precharged by the reset device *M2*. During integration carriers are collected in the depletion region of the photodiode and discharge *FD* proportionally. In the same manner as for the photogate active pixel shown in Figure 2-14, when the pixel is selected by driving *SEL* high, the active device *M3* forms part of a distributed source follower with *M5* (Figure 2-14(c)) and buffers the voltage on the *FD* node onto the column bus.

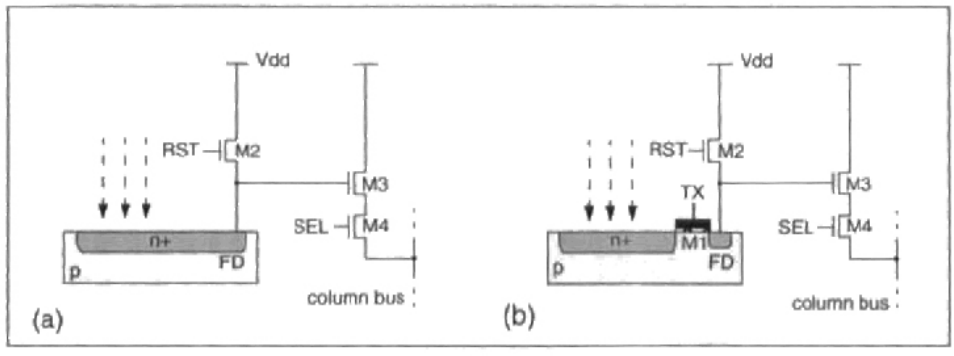


Figure 2-18. The (a) photodiode active pixel, and (b) photodiode active pixel with transfer gate.

The dimensions of the *FD* node of the photodiode active pixel are much larger than that of the photogate active pixel resulting in a larger capacitance and lower conversion gain. Typical values of conversion gain referred to the sensor output are less than 10 $\mu V/electron$ [Nixon et al. 1995]. To achieve conversion gain comparable to that of the photogate active pixel a transfer device *M1* can be introduced to the photodiode pixel as shown in Figure 2-18(b) to create a separate low capacitance *FD* node [Kyomasu 1991, Mendis et al. 1997b]. However, as with the single-poly photogate pixel it is not possible to ensure complete charge transfer from the photodiode to the *FD* node and consequently the photodiode active pixel with transfer gate suffers from image lag.

2-4.2.2 Photodiode APS Architecture with Correlated-Double Sampling

The read-out architecture used by the photogate APS imager can also be employed with the photodiode active pixel as shown in Figure 2-19. To realize two levels of CDS the additional circuits given in Figure 2-16 must also be implemented.

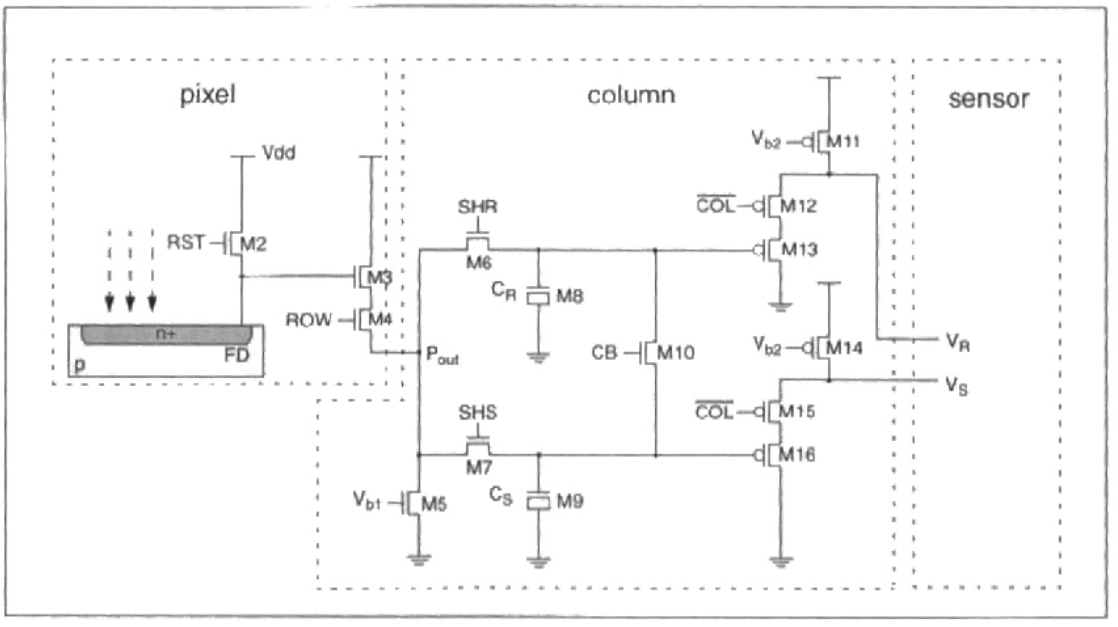


Figure 2-19. Photodiode active pixel sensor architecture.

2-4.2.3 Photodiode APS Operation

The operation of the photodiode image sensor with CDS can be explained with the aid of the timing diagram shown in Figure 2-20. For sensor read-out, each row is addressed in turn with the row decoding logic (not shown in Figure 2-19) driving the appropriate row line *ROW* to *Vdd*. The signal level on the *FD* node is buffered by the source follower formed by devices *M3-M5* and is sampled on the gate capacitance C_S by pulsing *SHS*. The *FD* node of the pixels in the row are then reset to a voltage approximately one threshold voltage drop below *Vdd* by pulsing *RST*. The reset level for each pixel is sampled on the gate capacitance C_R by pulsing *SHR*. The sampling of the pixel signal and reset levels by the column circuits is carried out in parallel for the pixels in the selected row. This typically occurs in the line blanking or horizontal synchronization period. To generate the image signal each column of the sensor is then addressed in turn by the column decoding logic (not shown in Figure 2-19) by driving the $\overline{COL}$ signal to ground. The column source followers formed by devices *M11-M16* buffer the sampled reset and signal levels onto common buses denoted V_R and V_S respectively. To perform the first stage of CDS the first differential amplifier in Figure 2-16 subtracts the signal and reset levels. This removes the pixel offset mismatch due to threshold voltage variations in devices *M2*, *M3*, and *M4* but not the pixel reset noise. The signal level is stored in a sample-and-hold stage S/H1 by pulsing *SH1*. To perform the second level of CDS the *CB* signal is driven high

and the first differential amplifier forms the offset difference of the column source followers. This offset is stored in a second sample-and-hold stage S/H2 by pulsing *SH2*. A final differential amplifier delivers the image signal V_{OUT} with column offsets removed that can be sampled or digitized on the rising edge of the pixel clock *PCLK*.

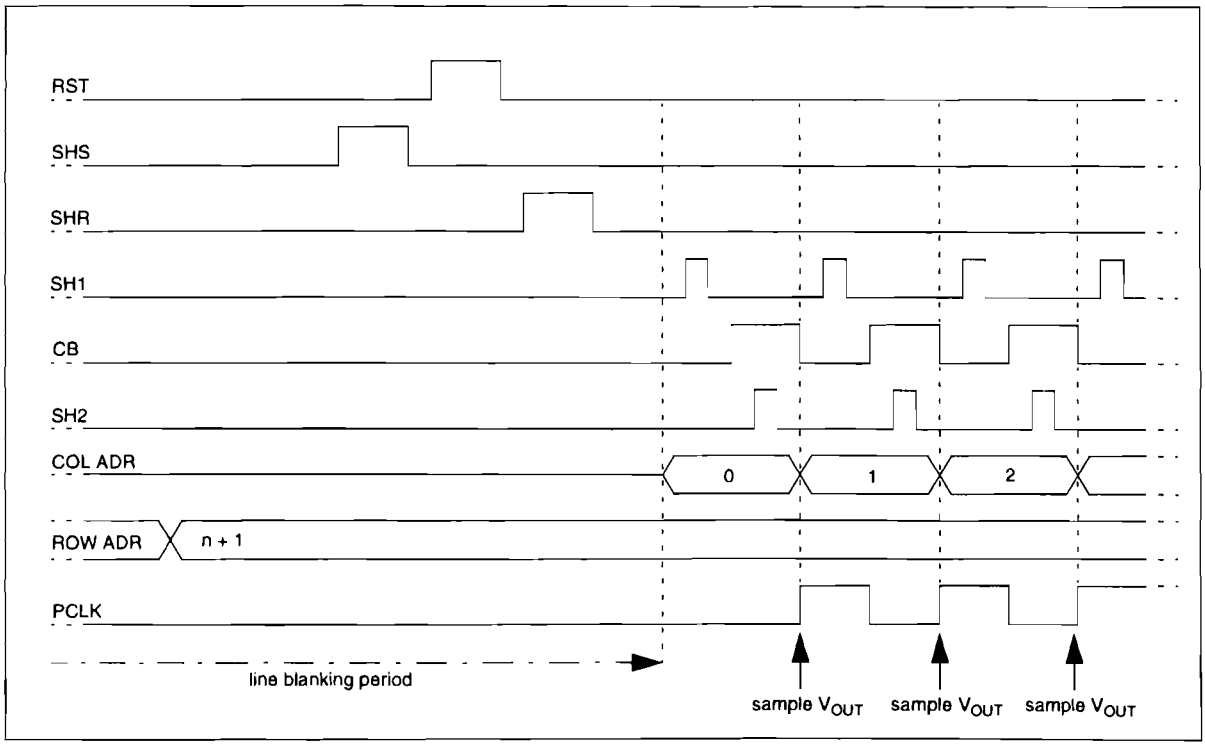


Figure 2-20. Timing diagram for the photodiode active pixel sensor.

2-4.2.4 Photodiode Reset Noise

Unlike the photogate APS sensor, the first stage of CDS does not cancel the reset noise introduced during pixel reset. This is because the reset noise contribution contained in the pixel signal level sampled on C_S is due to the reset operation of the previous read-out cycle, while the reset noise present in the reset level sampled on C_R is from the current cycle. As the two reset noise contributions are from different reset operations, they are not correlated and are not cancelled during CDS as described in Section 2-4.2.3 The magnitude of the reset noise for the photodiode APS can be computed with (2-16) using the capacitance of the photodiode. Typical values range from 75 to 100 electrons RMS [Fossum 1997]. To perform "true" CDS with the photodiode APS sensor to remove reset noise requires an external frame memory to store the reset level for each pixel at the start of the integration period, and then a means to subtract it off during sensor read-out. However, for many applications this is not practical or cost-effective. Despite "true" CDS not usually being performed with the active photodiode, the reset noise component of the active photodiode sensor is still smaller than that of a passive CMOS photodiode sensor. This is because in the active photodiode sensor only the relatively small capacitance of the photodiode is reset and not the capacitance of the entire column bus.

2-5. Non-Idealities of Solid-State Image Sensors

In addition to smear, lag, and read noise introduced earlier in the chapter, a number of other non-idealities limit the performance of both CCD and CMOS image sensors. They include dark current, photon shot noise, excess signal carriers, fixed-pattern noise, pixel cross talk, and aliasing. Each of these phenomena and the techniques used to manage them will now be discussed.

2-5.1 Dark Current

During sensor integration, independent of whether the sensor is illuminated or not, a small current known as the *dark current* produces carriers that are collected by the pixels. Dark current is caused by thermal generation of electron-hole pairs at defects in the silicon crystal structure [Theuwissen 1995]. Generation sites that contribute to the dark current are located at the Si-SiO_2 interface, in the depletion region defined by the pixel structure, or in the silicon bulk itself. However, the contribution from the interface states that occur at the Si-SiO_2 interface is in excess of 90% of the total dark current [Toren and Bisschop 1994]. The remaining fraction is due to minority carriers that are generated within the pixel depletion region, or diffuse to it from the substrate bulk.

2-5.1.1 Characterizing Dark Current

The dark current of a sensor is usually described using a characteristic current density J_{dark}. For an integration time T_{int} and pixel area A_{pixel} the number of dark electrons N_{dark} collected by each pixel corresponding to a dark current density J_{dark} is given by [Holst 1996]:

$$N_{dark} = \frac{J_{dark} A_{pixel} T_{int}}{q} \quad electrons \tag{2-19}$$

where q is the electronic charge. Through the sensor conversion gain G this produces a mean dark signal μ_{dark}:

$$\mu_{dark} = G N_{dark} \quad Volts \tag{2-20}$$

2-5.1.2 Dark Current Shot Noise

Associated with dark current is a temporal noise component known as *dark current shot noise* [Theuwissen 1995]. Dark current generation is a stochastic process described by a Poisson probability distribution. Consequently the number of RMS electrons representing the shot noise on the dark current $n_{dark\ shot}$ is given by the square root of the number of electrons representing the dark current:

$$n_{dark\ shot} = \sqrt{N_{dark}} \quad electrons\ RMS \tag{2-21}$$

Through the sensor conversion gain G this corresponds to an RMS voltage variation $\sigma_{t_{dark\ shot}}$ on the mean signal given by:

$$\sigma_{t_{dark\ shot}} = G\, n_{dark\ shot} \quad Volts\ RMS \tag{2-22}$$

Dark current shot noise can only be reduced by decreasing the sensor dark current level.

2-5.1.3 Dark Current Non-Uniformity

The generation sites for the dark current are statistically distributed throughout the sensor and the generation rate of each site can vary. As a result the sensor dark current is not uniform from pixel to pixel [Theuwissen 1995]. This is known as *dark current non-uniformity* and contributes a random offset to the signal charge collected by each pixel. As the mean value of this offset is unchanged from frame to frame it produces stationary artifacts in the image output from the sensor. This constitutes a component of the sensor *fixed-pattern noise* (FPN). Dark current non-uniformity can be reduced by decreasing the dark current level, or by measuring and storing its value for each pixel external to the sensor and subtracting it during sensor read-out [Hurwitz et al. 1997].

2-5.1.4 Managing Dark Current

Dark current can be managed at the fabrication process level, at the sensor architectural level, or by lowering the sensor operating temperature. As the greatest number of traps responsible for dark current generation occur at the Si-SiO_2 interface, a number of important techniques specifically target this region. The rate of carrier generation U_s by interface states is a function of both the density of states, and the density of free carriers at the interface [Saks 1980]. Under normal operation the interface of most pixel structures is depleted and devoid of carriers and consequently U_s has its maximum value. However, U_s decreases by orders of magnitude if a high density of free carriers exists at the interface, as occurs when the interface is inverted or in accumulation.

2-5.1.5 Surface Pinning

Surface pinning is a technique that minimizes dark current by ensuring that the Si-SiO_2 interface remains in accumulation [Teranishi et al. 1982, Stevens et al. 1991]. Surface pinning for a photodiode pixel can be achieved by implanting a thin $p+$ layer at the surface of the photodiode structure as shown in Figure 2-9(b). This pins the potential at the Si-SiO_2 interface to that of the substrate and ensures free holes are available to fill the interface states. For this reason the pinned photodiode is sometimes called a hole-accumulation device (HAD) [Hojo et al. 1991, Furukawa et al. 1992]. Surface pinning also ensures complete charge transfer from the

photodiode to eliminate image lag. However, pinned photodiodes are not available in a standard CMOS fabrication process and an additional process module must be introduced if they are to be used [Guidash et al. 1997]. Surface pinning has also been applied to a frame-transfer CCD but the details of the implementation are quite different [Bosiers et al. 1995].

2-5.1.6 Charge Pumping

The dynamic properties of interface states are such that if the surface beneath a CCD gate is switched from inversion to depletion and then back to inversion within a certain time interval, the generation of dark current can be effectively suppressed. This technique is known as *charge pumping* and can be used with multi-phase frame-transfer CCDs [Burke and Gajar 1991, Schaeffer et al. 1994]. During integration a number of the stages within each pixel of the multi-phase FT-CCD are inverted, while the others are depleted to collect photon generated charge. During the course of the integration period the phase voltages are changed such that the role of each stage is cycled between inversion to suppress dark current generation, and depletion to collect the signal charge packet.

2-5.1.7 Process Cleanliness

A critical aspect of dark current management is the purity of the starting materials and the cleanliness of the fabrication process used to manufacture the sensor [Theuwissen 1995]. Both of these issues are rigorously addressed in the production of CCD image sensors. However, as the performance of digital logic circuits used in the vast majority of CMOS applications is not degraded by the presence of modest levels of leakage[1], dark current in a standard CMOS fabrication process is greater than that found in CCD sensors.

2-5.1.8 Cooling

Dark current has a substantial dependence on temperature, doubling approximately every 8°C [Theuwissen 1995]. While cooling solid-state image sensors greatly reduces dark current, it is only practical to do so for certain scientific applications.

2-5.2 Photon Shot Noise

The absorption of photons in a semiconductor substrate to produce electron-hole pairs is a stochastic process described by a Poisson probability distribution [Holst 1996]. Consequently, the number of RMS electrons representing the shot noise on the signal $n_{photon\ shot}$ is given by the square root of the number of signal electrons N_{signal} according to:

$$n_{photon\ shot} = \sqrt{N_{signal}} \quad electrons\ RMS \tag{2-23}$$

1. Dark current in non-imaging applications of CMOS technology is known as *leakage current*.

Through the sensor conversion gain G this corresponds to an RMS voltage variation $\sigma_{t_{photon\ shot}}$ on the mean signal given by:

$$\sigma_{t_{photon\ shot}} = G\, n_{photon\ shot} \quad Volts\ RMS \tag{2-24}$$

2-5.3 Sensor Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) of a solid-state image sensor is defined as the ratio of the signal level μ_{signal} to the total temporal noise $\sigma_{t_{total}}$:

$$SNR = \frac{\mu_{signal}}{\sigma_{t_{total}}} \text{ or } SNR_{dB} = 20log_{10}\left(\frac{\mu_{signal}}{\sigma_{t_{total}}}\right) \tag{2-25}$$

The total temporal noise of a sensor consists of a number of components including the photon shot noise $\sigma_{t_{photon\ shot}}$, dark current shot noise $\sigma_{t_{dark\ shot}}$, and read noise $\sigma_{t_{read}}$. It also contains temporal noise contributed by subsequent stages of processing in the signal path such as amplifiers and A/D converters which can be collectively denoted $\sigma_{t_{post\text{-}prrocessing}}$. As these noise components are independent their contributions add in quadrature to give

$$\sigma_{t_{total}} = \sqrt{\sigma^2_{t_{photon\ shot}} + \sigma^2_{t_{dark\ shot}} + \sigma^2_{t_{read}} + \sigma^2_{t_{post\text{-}prrocessing}}} \quad Volts\ RMS \tag{2-26}$$

Using (2-10) and (2-21) - (2-25) it is possible to express the SNR as:

$$SNR = \frac{N_{signal}}{\sqrt{N_{signal} + N_{dark} + \left(\frac{\sigma_{t_{read}}}{G}\right)^2 + \left(\frac{\sigma_{t_{post\text{-}prrocessing}}}{G}\right)^2}} \tag{2-27}$$

From (2-27) it is clear that high conversion gain G minimizes the contribution of the sensor read noise and that of post-processing stages to the sensor SNR.

2-5.3.1 Photon Shot Noise Limit

At moderate to high levels of illumination N_{signal} becomes much larger than the other terms in the denominator of (2-27) and consequently the temporal noise performance of a sensors is dominated by photon shot noise [Theuwissen 1995]. Under these conditions the signal-to-noise ratio of a sensor is given simply by

$$SNR = \sqrt{N_{signal}} \tag{2-28}$$

When the sensor is photon shot noise limited in this manner, the SNR performance of the sensor can only be improved by increasing the number of signal electrons collected N_{signal}.

For most applications the integration time is determined by the frame rate of the video format, and the pixel dimensions are determined by resolution and optical considerations. However, it is often possible to increase N_{signal} by improving the pixel fill-factor and/or the quantum efficiency of the photodetector structure.

2-5.3.2 Microlenses

The pixel fill-factor can be increased by placing a *microlens* over each pixel as illustrated in Figure 2-21. Microlenses are designed to re-direct incident light that would otherwise fall on pixel read-out devices, onto the portion of the pixel area that is available for the collection of photon generated charge. The use of microlenses is widespread and typical improvement in pixel sensitivity is about 35% [Daemen and Peek 1994].

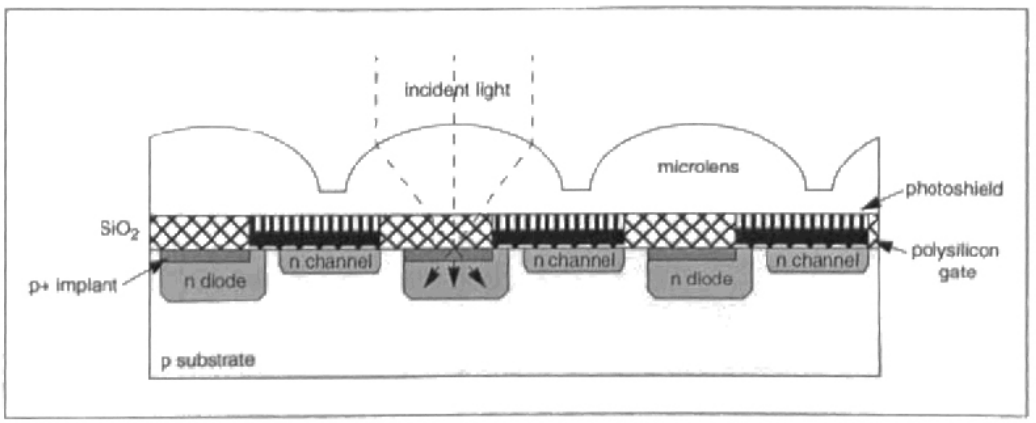


Figure 2-21. Cross section of an IL-CCD sensor with microlenses.

2-5.4 Excess Signal Carriers

In addition to performance limitations due to the collection of insufficient signal carriers, the generation of too many carriers can also cause problems for solid-state image sensors. Once the collection site in a pixel is full, excess carriers can spill into neighbouring pixels [Theuwissen 1995]. This phenomenon is known as *blooming*.

2-5.4.1 Anti-Blooming Structures

To prevent blooming it is common for CCD sensors to include additional implants or devices within each pixel to allow excess carriers to be removed. Once the collected charge has reached a predetermined level, any additional charge is preferentially drained to an *n*-type epitaxial layer beneath the *p*-type substrate, rather than adjacent pixels. Both vertical and lateral anti-blooming structures have been demonstrated [Ishihara et al. 1982, Ando et al. 1991].

2-5.4.2 Electronic Shutter

The frame rate of a solid-state image sensor is usually determined by the application. However, it is possible to reduce the amount of charge collected in each pixel by shortening the

effective integration period T_{int} to some fraction of the frame period T_{frame}. This technique is known as *electronic shutter* or *charge reset* and requires the ability to remove the charge collected by each pixel at the instant T_{int} prior to normal signal charge read-out as shown in Figure 2-22. The mechanism by which charge reset is realized is different for the various solid-state sensor architectures but includes options such as a "dummy" read-out, or the global operation of anti-blooming devices [Theuwissen 1995]. In general electronic shutter is used to provide a method for controlling the exposure level of the entire sensor, while anti-blooming structures are used to deal with excess carriers at the individual pixel level generated by image highlights.

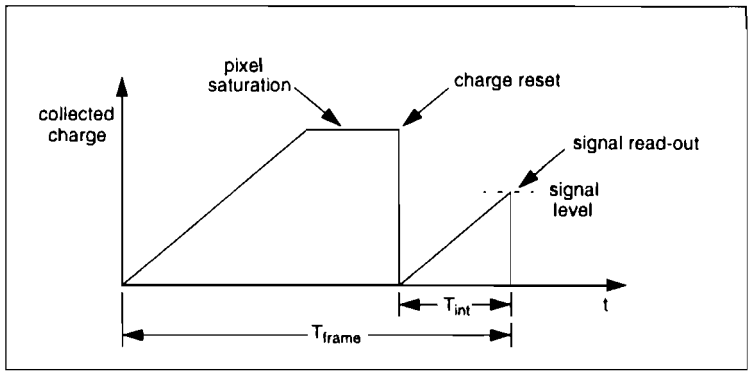


Figure 2-22. Electronic shutter or charge reset to control sensor exposure.

2-5.5 Fixed-Pattern Noise

Stationary artifacts present in the image produced by a solid-state sensor are known as *fixed-pattern noise* (FPN). Fixed-pattern noise is caused by device and circuit non-uniformity across the array and in the read-out path(s).

2-5.5.1 Dark Current Non-Uniformity

As discussed in Section 2-5.1.3, dark current non-uniformity across the sensor contributes a fixed-pattern noise component that can be characterized as a random pixel offset.

2-5.5.2 Photo-Response Non-Uniformity

Due to manufacturing tolerances the quantum efficiency of each pixel in a sensor array may differ slightly. This is known as *photo-response non-uniformity* (PRNU) and can be characterized as a random pixel gain variation [Holst 1996]. Therefore PRNU is signal dependent and it is a multiplicative factor of the photon shot noise.

2-5.5.3 Signal Read-Out Non-Uniformity

As signal read-out from each pixel follows a different path to the sensor output stage, any device or circuit variations in the read-out path can introduce fixed-pattern noise. FPN in CCD sensors can be caused by defects producing variations in the charge transfer efficiency of CCD

stages in the array. FPN may also be introduced by variations in read-out timing [Holst 1996]. If multiple output stages are used in the sensor, any conversion gain non-uniformity between the output stages introduces gain mismatch between the segments of the image that correspond to the respective output stages. Fixed-pattern noise in CMOS image sensors is dominated by pixel and column circuit mismatch. Threshold voltage variations across the array introduce FPN at both the pixel and column level characterized as random pixel and column offsets respectively. Conversion gain non-uniformity in CMOS APS image sensors produces random pixel gain variations [Nixon et al. 1996b].

2-5.5.4 Managing Fixed-Pattern Noise

Fixed-pattern noise in CCD image sensors is managed at the device level. Dark current non-uniformity, photo-response non-uniformity, and signal read-out non-uniformity are all minimized by optimization of the fabrication process. Dark current non-uniformity can also be significantly reduced by cooling. Manufacturing CMOS image sensors in a standard CMOS fabrication process precludes managing fixed-pattern noise at the device level. Instead FPN must be minimized through careful circuit design. Pixel and column FPN due to device mismatch in CMOS APS imager sensors can be reduced through the use of two levels of correlated-double sampling [Mendis et al. 1994a]. However CDS does not cancel dark current non-uniformity, photo-response non-uniformity, or conversion gain non-uniformity.

2-5.6 Pixel Cross Talk

2-5.6.1 Lateral Diffusion of Photon Generated Carriers

A portion of the minority carriers generated by photons in the substrate of a solid-state image sensor have to diffuse to the depletion region to be collected. As there is no predefined direction for this diffusion path, it is possible for carriers to be collected by pixels other than those under which they were generated [Stevens and Lavine 1994, Theuwissen 1995]. This "misdiffusion" is illustrated in Figure 2-23 and causes image blurring.

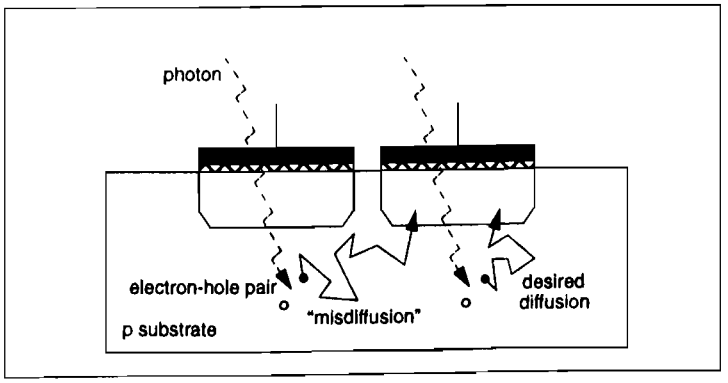


Figure 2-23. "Misdiffusion" of photon generated minority carriers.

As the penetration depth of longer wavelength photons is greater than that of photons with short wavelength, misdiffusion is chiefly caused by photons with long wavelengths being absorbed below the pixel structures.

2-5.6.2 Light Piping

Another phenomenon that degrades image sharpness is light piping [Theuwissen 1995]. In this instance stray photons incident on one pixel are introduced into neighbouring pixels by multiple internal reflections at the interface of layers deposited on the sensor substrate. Interfaces responsible for light piping can include the Si-SiO_2 interface, and the interface between SiO_2 and other layers such as light shields or colour filters.

2-5.6.3 Managing Cross Talk

Cross talk in CCD sensors is managed at the fabrication process level by optimization of the thickness of layers deposited on the sensor surface. It is also managed by controlling the doping concentration of the sensor substrate to limit the diffusion length of minority carriers. However, as the sensor quantum efficiency at long wavelengths is also a function of the diffusion length, reducing pixel cross talk in this manner involves a trade-off. Cross talk can also be reduced by providing $p+$ channel stops between pixels that absorb free electrons. The manufacture of image sensors in standard CMOS precludes optimizing the fabrication process to control pixel cross talk.

2-5.7 Aliasing

Image acquisition by solid-state image sensors involves sampling in two spatial dimensions and in time [Dubois 1985]. As with any sampled data system, *aliasing* occurs for frequencies greater than the Nyquist frequency unless appropriate low-pass filtering is used.

2-5.7.1 Temporal Aliasing

The three-dimensional signal produced by the camera optical system is not temporally bandlimited. Furthermore, the linear integration of photon generated charge in the camera solid-state imager does not realize the optimal temporal low-pass filtering operation for a given frame or field rate. This admits the possibility of *temporal aliasing* in which high temporal frequencies are mapped to lower frequencies in the video stream. This can lead to unwanted visual effects. For example, continuously rotating objects in a scene may appear to rotate forward or backwards at strange speeds. In general it is not practical to temporally bandlimit the optical signal, so to minimize temporal aliasing it is necessary to employ a sufficiently high frame rate for a given application.

2-5.7.2 Spatial Aliasing

The pixel array of a solid-state imager performs two-dimensional spatial sampling of the image produced by the camera optical system. The sampling function is not only dependent on the pixel *pitch*, the distance between adjacent pixel centres, but also on the pixel fill-factor [Holst 1996]. As the camera optics do not sufficiently spatially bandlimit the optical signal, spatial aliasing is introduced into the image produced by the sensor. Spatial aliasing artifacts generated by periodic image structure are known as *Moiré patterns*. For some applications spatial aliasing is reduced with the use of optical birefringent filters to blur the image prior to sampling by the pixel array.

2-6. Conclusion

Fundamental principles of solid-state imaging such as photon absorption and charge collection and integration are the same for both CCD sensors and CMOS active pixel sensors. The primary differences between CCD and CMOS imaging technology is in the way signal read-out is effected, and in the management of non-idealities such as dark current, fixed-pattern noise, and pixel cross talk.

High performance signal read-out in a CCD sensor is achieved through transporting signal charge to the output stage with a high degree of efficiency. However, the manufacturing requirements and power dissipation needed to accomplish this goal are restrictive for many applications. High performance signal read-out in a CMOS APS sensors is achieved through in-pixel charge-to-voltage conversion, and the application of correlated-double sampling methods to reduce fixed-pattern noise due to circuit mismatch. Extremely low power dissipation is possible as each pixel is only addressed once, and the capacitances and voltages involved are markedly lower that those of CCDs.

The key difference between CCD and CMOS imaging technology in terms of the level of image quality that can be attained is in the management of non-idealities such as dark current, fixed-pattern noise, and pixel cross talk. CCD technology addresses each of these issues at the device level through specialization of the fabrication process. The last 20 years has seen the maturation of CCD imaging technology with the origins of non-idealities being identified, and advancements to the fabrication process to eliminate or reduce their impact on sensor performance being developed. In contrast, APS is being promoted as a new technology that enables image sensors to be produced in a standard CMOS fabrication process that is not specialized for this purpose. Within this paradigm the only avenue available to address sensor non-idealities are innovations at the circuit level. While subjectively impressive CMOS APS image sensors have been demonstrated, rigorous performance comparisons with CCD sensors have not been undertaken prior to this thesis work. As such the non-idealities that limit the performance

of APS sensor manufactured in standard CMOS have remained largely unidentified and unquantified, and questions as to whether they could be addressed at the circuit level were not resolved. A major contribution of this thesis is to identify the performance limitations of CMOS APS technology, and show that they can only be effectively managed at the fabrication process level.

CHAPTER 3 Digital Colour Camera Technology

3-1. Introduction

This chapter introduces digital camera technology. Electronic display technology and colour science have a substantial influence on solid-state camera architecture and hence are reviewed in detail. The system level requirements for realising a digital colour camera are then described. The chapter concludes by discussing the implementation of digital cameras in terms of CCD and CMOS APS technology. The material presented in this chapter can be considered prerequisite for Chapters 4 and 5.

3-2. Digital Cameras

3-2.1 General Electronic Image Acquisition

Electronic image acquisition is the process by which an image formed by an optical system is converted into an electrical signal suitable for storage, transmission, or display. It requires a mechanism by which an optical image can generate or modulate an electrical quantity such as charge, current, or voltage. Electronic imaging also entails a sampling and reformatting operation to convert the temporal and two spatial dimensions of the image produced by an optical system into the one temporal dimension of an electrical signal [Schrieber 1993]. With the exception of machine vision applications, the purpose of an electronic imaging system is the reproduction of an electronically acquired image for viewing, either in printed form, or on a television or computer display.

A generalized electronic imaging system is shown in Figure 3-1. As the ultimate purpose of an electronic imaging system is image reproduction for a human observer, the characteristics

of the human visual system play an important role in electronic imaging, transmission, and display technology.

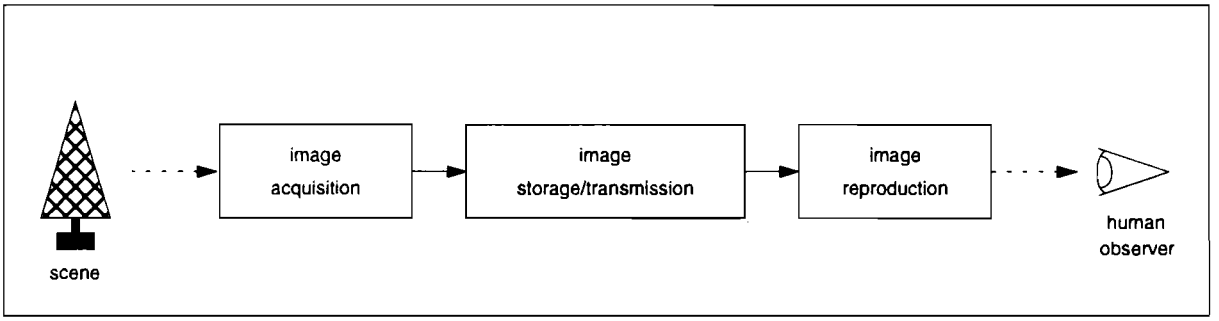


Figure 3-1. A generalized electronic imaging system.

3-2.2 Analog and Digital Imaging Technology

All image acquisition and image reproduction technologies are analog in nature. The difference between analog and digital imaging technology is the manner in which images are stored or transferred. In conventional photography images are generated and stored chemically on a film. Images for television and video are stored or transmitted using analog modulation techniques. While digital signal processing techniques and hardware are widely used to implement various stages of processing subsequent to image acquisition, the final image representation employed for storage or transmission is analog [Morimura et al. 1990]. In contrast a digital camera represents an image or video stream as a sequence of binary numbers. The advantages of digital images and digital video is that they are easily manipulated or edited using a computer and transferred over a digital network [Netravali and Haskell 1988]. Digital storage and transmission are not subject to degradation in the same manner that analog recording and transmission techniques are. In addition it is straightforward to implement redundancy and error correction digitally.

3-2.3 Categories of Digital Cameras

Consumer digital cameras that are currently available fall into three main categories; portable digital cameras for still-image acquisition, portable digital cameras for video acquisition, and digital cameras which are tethered to a computer that can be used for both still-image and video acquisition.

3-2.3.1 Portable Digital Cameras for Still-Image Acquisition

Portable digital cameras for still-image acquisition provide immediate access to captured images in a digital format as opposed to the time and cost involved in processing the film from a photographic camera, and then scanning and digitizing the print. Digital images are taken and stored on the camera and can later be down-loaded to a computer through a standard I/O

port. However, at present the quality of images generated from consumer level digital cameras cannot match those produced by a 35-mm photographic camera. For many applications this shortcoming is outweighed by the convenience of immediate digital images. An example of such a product is the Apple Quicktake 150 which has a resolution of 640 x 480 pixels [Quicktake]. A high-end professional level digital camera which provides image quality approaching that of 35-mm photographic film is the Kodak DCS460 which has a resolution of 3060 x 2036 pixels [Kodak]. Portable digital cameras for still-image acquisition are finding increasing application in commercial areas such as publishing, law enforcement, security, real-estate, and insurance.

3-2.3.2 Portable Digital Cameras for Video Acquisition

Portable digital cameras for video acquisition, in conjunction with new standards for recording digital video on magnetic tape, provide precise and essentially lossless video editing and copying. Such capabilities make use of sophisticated digital error correction coding and an intra-frame compression technique known as I-MPEG [Doyle]. Most portable digital cameras also support the capture of still-images. An example of such a camera is the Sony DCR-DX700 Digital Handycam that provides video quality superior to analog video standards such as Betacam or S-VHS [Sony]. Portable digital cameras for video acquisition are finding application with corporate and media video producers and as the price of digital video cameras falls they will replace the consumer analog video camera.

3-2.3.3 Tethered Digital Cameras

The final category is that of the tethered digital camera which is attached to a computer and provides both still-image and video acquisition capability. Tethered digital cameras have no on-camera image storage and instead directly transfer still-images or video to a host computer via a digital interface. To remove the need for the host computer to have specialized hardware it is common to make use of standard interfaces such as the serial or parallel port. Unfortunately these interfaces were not intended for transferring video and have a relatively low bandwidth. This limits the video image quality obtained from tethered digital cameras in terms of resolution, available colours, and frame rate. An example of such a camera is the Connectix Color QuickCam [Connectix]. Tethered digital cameras are being used in a growing number of multi-media applications and it has been suggested that if their price can be reduced to below US $50 they will become a standard peripheral in the consumer personal computing market [Ackland and Dickinson 1996]. It can also be expected that as new higher bandwidth digital interface standards are adopted, for example Firewire or the Universal Serial Bus, the image quality and frame rate available from tethered digital cameras will significantly improve [Firewire, USB].

3-3. Electronic Display Technology

The architecture of a digital colour camera is determined by many factors in addition to those associated with solid-state image sensors. In particular the requirements of producing images suitable for electronic display with accurate colour rendition play a critical role in camera system architectures.

3-3.1 CRT Display Technology

The electronic display technology of television receivers and computer monitors is based on the cathode ray tube (CRT) [Schrieber 1993, Holst 1996]. While a number of alternative display technologies have been developed, they have only replaced the CRT in niche applications. The most important of these technologies at present is the liquid crystal display (LCD) which is widely used in portable applications such as laptop computers. The LCD is superior to the CRT in terms of power dissipation, weight, and physical dimensions but cannot compete with the colour rendition and contrast ratio achievable by the CRT. The dominance of the CRT and its influence on video and transmission standards has important implications for the architecture of solid-state image sensors and cameras.

3-3.2 Frame Rate

The temporal sampling frequency or *frame rate* of analog video standards is determined by the need to minimize the perceptibility of *flicker* on CRT displays [Schrieber 1993]. The phosphors used in CRTs are brightened only momentarily by the scanning electron beam and their decay is quasi-exponential. This means that they do not provide the optimal temporal low-pass filtering operation required for reconstruction of the video signal. While a frame-store can be included as part of the display hardware to support temporal interpolation to reduce flicker, this technique is not yet widely used due to the additional complexity and cost involved. Instead video standards exploit the characteristic of the human visual system to behave like a temporal integrator for a select range of input frequencies. The human perception of flicker depends on the size and brightness of the object being viewed, the larger and brighter the object, the more noticeable is the flicker. The ambient light level for viewing also plays a significant role.

3-3.3 Scanning Formats

3-3.3.1 Interlace Scanning

Analog video standards such as NTSC and PAL acquire, record, transmit, and display images using an *interlaced* format [Poynton 1996]. Each frame is scanned in two successive vertical passes, first the odd field and then the even field as shown in Figure 3-2(a). As the flicker susceptibility of vision is due to a wide-area effect, as long as the complete height of the

picture is scanned rapidly enough to overcome wide-area flicker, small-scale picture information, such as that in the alternate lines, can be displayed at a lower rate. This means that a lower frame rate can be used with a given display brightness resulting in a higher vertical resolution for the same signal bandwidth or data rate. For example NTSC uses two fields of 262.5 lines at a field rate of 60 Hz to give a frame of 525 lines at a frame rate of 30 Hz. Under appropriate viewing conditions the visual system temporally integrates the two fields.

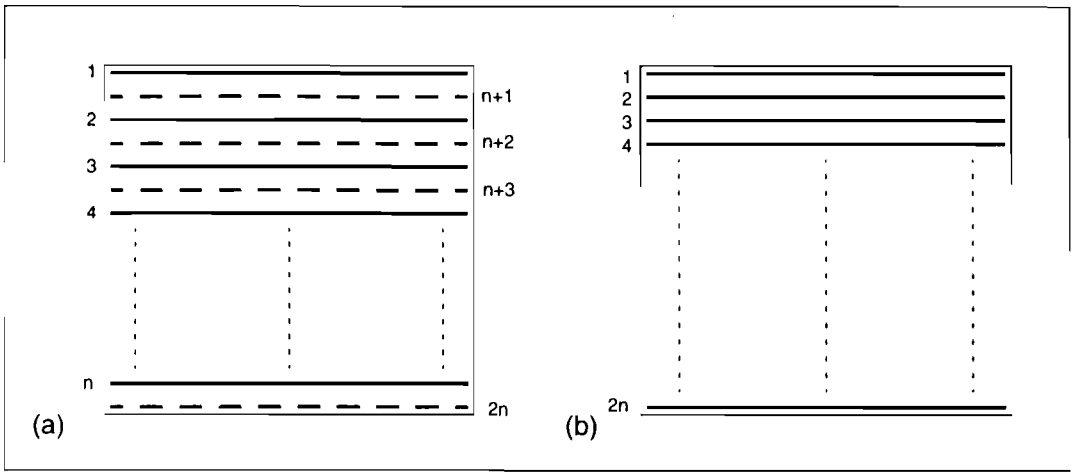


Figure 3-2. Interlaced and progressive scanning with *2n* rows or lines where the numbers indicate the order in which the rows are scanned. (a) Interlaced scanned frame formed from two fields each of *n* rows represented by solid and dashed lines respectively. (b) Progressive scanned frame consisting of one field of *2n* rows.

3-3.3.2 Progressive Scanning

If interlace worked perfectly the frame vertical resolution would be double the field vertical resolution. In fact however the vertical resolution is increased only marginally except at low brightness [Schrieber 1993]. Also fine detail in images is subject to *twitter*, a small-scale phenomenon that is perceived as rapid back-and-forth motion [Poynton 1996]. An important application in which interlace is not satisfactory is that of computer displays. For typical computer operation the user is much closer to the display than in a television viewing environment and the ambient light level is considerably brighter. Computing applications also require the display of small alpha-numerical characters and highly detailed images. For these reasons a *progressive* video format is used to drive the CRT display in which each row or line is scanned in turn as shown in Figure 3-2(b). A higher frame rate of at least 70 Hz is also required.

Another important application which uses a progressive format is that of digital video compression standards such as MPEG. If the video source for compression is only available in interlaced format then either only one field is used, or else a field memory is required to de-interlace the video stream for each complete frame to be compressed [AVP 1995].

3-3.4 Synchronization and Blanking Intervals

Analog video standards and their digital equivalents include both horizontal and vertical blanking intervals within the video stream [Poynton 1996]. The CRT requires these intervals to extinguish the electron gun and retrace its position to the start of the next line or to the top of the display ready to start the next field or frame. The blanking intervals of NTSC and PAL form a significant percentage of the time allotted for each frame as shown in Figure 3-3. To save bandwidth recent digital video standards for recording or transmission across a digital network do not include this synchronization information. Instead it is generated in the receiver or decoder before display [Doyle].

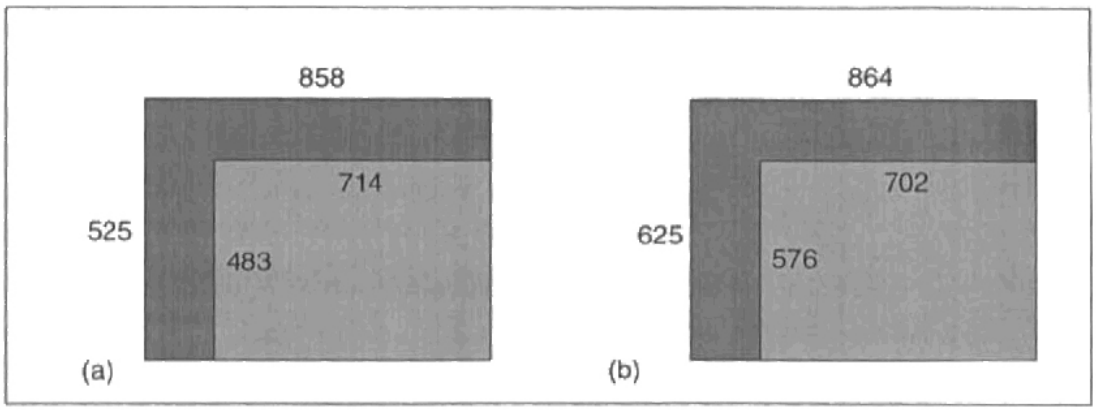


Figure 3-3. Digital component video (4:2:2) for (a) NTSC and (b) PAL. The dark areas represents the vertical and horizontal blanking intervals and the light areas the active image area. The numbers indicate the number of lines and pixels. The sampling frequency is 13.5 MHz [Poynton 1996].

3-3.5 Gamma Correction

Another important property of CRTs that has influenced video standards is that of the very non-linear response of the electron guns used to excite the screen phosphors. As a consequence the luminance of a CRT display is not proportional to the voltage applied to the electron gun by the video signal, but rather that voltage raised to a power between 2 and 3. It is conventional to compensate for this non-linearity by applying what is known as *gamma correction* to the pixel values in the camera [Poynton 1996]. The transfer function of a typical CRT and the transfer function of a nominal gamma correction to be applied to the video signal by the camera are shown in Figure 3-4. For colour video it is necessary to apply gamma correction to each of the red, green, and blue components respectively prior to colour difference encoding. Performing gamma correction in the camera has the added advantage of transforming the video signal into a more perceptually uniform signal space that maximizes the use of the available digital video codes and minimizes the visibility of noise introduced during digital video compression and

transmission. Gamma correction is assumed for digital coding standards such as JPEG and MPEG.

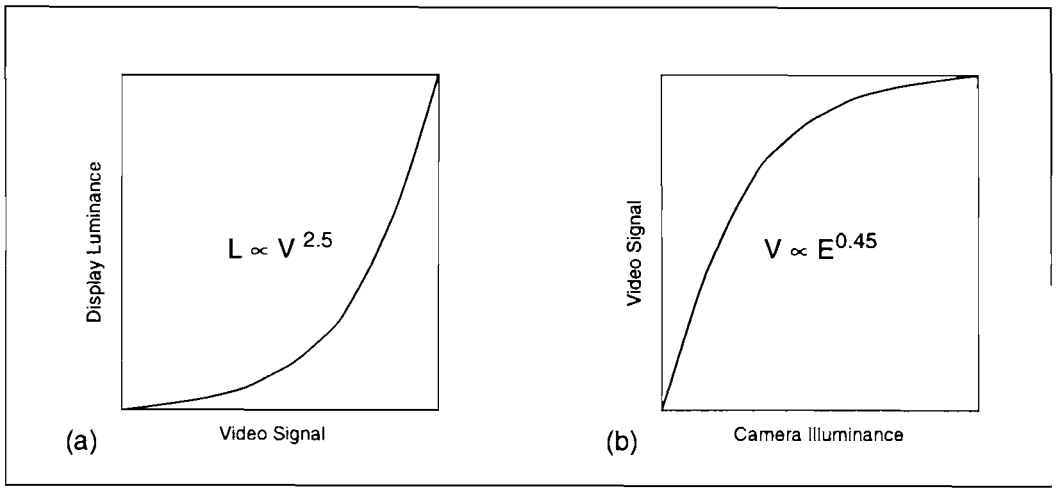


Figure 3-4. (a) The transfer function of a typical CRT. (b) The gamma correction transfer function required by a camera for a gamma of 0.45.

3-3.6 Influence on Solid-State Imaging Technology

The characteristics of CRTs discussed in the previous paragraphs have important implications for the architecture of CCD image sensors and the signal processing requirements of solid-state cameras [Theuwissen 1995]. Most CCD sensors are dedicated to a specific scanning mode, either interlaced or progressive. Furthermore the method by which each scanning mode is implemented for the interline, frame-interline transfer, and frame-transfer architectures is different. The architecture of CMOS image sensors are more flexible and support both interlaced and progressive scan using appropriate address generation. The scanning format also influences electronic shutter operation used to regulate the camera exposure, particularly for CCD sensors. For example, it is common for interlace cameras to use integration periods based on the field rate rather than the frame rate to avoid image disturbances caused by moving objects in a scene.

Analog video cameras require an interlaced format while digital video and digital still cameras employ progressive scan [Naito et al. 1995]. Analog video cameras directly provide the timing signals required to drive a CRT display. Therefore the frame rate, scanning format, and clock signals needed by the image sensor are predetermined. The read-out of image sensors used in digital video and digital still cameras is more flexible because the sensor is not synchronized to the display.

All video cameras perform gamma correction. Historically this has been done for reasons of economies of scale to make the electronics of the television receiver and display as simple and

low cost as possible. As long as CRT is the dominant display technology it is likely that video standards will continue to compensate for CRT non-idealities.

3-4. Colour Science for Solid-State Imaging

This section introduces the basic principles of colour science and their application to solid-state imaging. It will be shown that imaging in colour places additional requirements on the performance of solid-state image sensors and substantially determines the architecture of solid-state colour cameras.

3-4.1 Human Colour Vision

The concept of colour is more subtle than is widely understood. Colour is not an external physical phenomenon but the perceptual result of a given power spectral power distribution of light, with wavelengths in the visible region of 380nm to 780nm, stimulating the human visual system. Incident light is focused by the optical system of the eye onto the retina. The retina of the human eye is covered with two different types of photoreceptors known as rods and cones [Hunt 1995]. The function of the rods is to provide monochromatic[1] or *scotopic* vision under low levels of illumination while the cones provide colour or *photopic* vision at normal levels of illumination. The cones themselves can be divided into three types, ρ, γ, and β, each responding to incident radiation with a different spectral response. Perceptual sensations such as brightness and colour are generated in the visual cortex of the brain by combining and comparing the outputs of the three types of cones and the rods in a manner that is not well understood [Zeki 1993]. In this sense colour only exists in the brain of the observer.

3-4.2 Colorimetry

While the physiology of colour vision and its philosophical implications are of considerable interest, they have not been explicitly used to provide a framework for colour image acquisition and reproduction systems. Instead all practical electronic colour imaging and reproduction systems have been developed by applying principles of an empirical science known as *colorimetry* [Wyszecki and Stiles 1982, Hunt 1995]. Colorimetry provides a numerical specification of colour. It incorporates photometry, the empirical science that quantifies perceived brightness, which was introduced in Section 2-2.2.2. Using the results of a series of brightness and colour matching experiments the Commission Internationale de l'Eclairage (CIE) has estab-

1. The word "monochromatic" is used in this context to describe vision without the sensation of colour and does not imply that vision under these conditions is dependent on a single wavelength. However in the remainder of this chapter the word monochromatic will be used in the latter, stricter sense.

lished photometric and colorimetric standards based on the concept of the *Standard Photometric Observer* and the *Standard Colorimetric Observer* respectively. These standards allow the brightness and colour of a given spectral power distribution to be predicted and quantified under specific viewing conditions.

3-4.3 Additive Colour Mixtures

As colour is determined by the spectral power distribution of visible light reaching the eye, a given colour can be generated by synthesizing an appropriate spectral power distribution. Colorimetry is based on additive colour mixtures formed using multiple radiant energy sources as shown conceptually in Figure 3-5. The total radiant flux received by the eye is the sum of the flux from each of the sources and the spectral power distribution at the eye is the wavelength-by-wavelength sum of the respective spectral power distributions of each of the sources. In practice additive colour mixtures are formed by superimposing beams of light on a diffuser, by viewing the different beams in succession at a frequency high enough to remove all sense of flicker, or by viewing them in adjacent areas that are too small to resolve with the acuity of the human visual system [Hunt 1995].

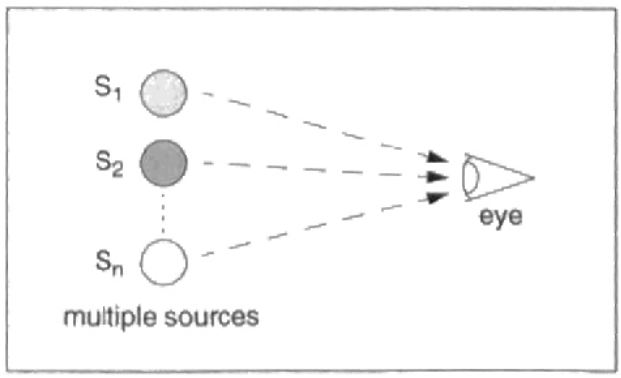


Figure 3-5. Conceptual definition of an additive colour mixture. The S_i denote different sources of radiant energy in the visible spectrum.

The range or *gamut* of colours that can be realized using additive colour mixtures is dependent on the number of sources and the relationship of their respective spectral power distributions. As a consequence of the fact that there are three types of cones responsible for colour vision, most colours can be mixed using three suitably chosen light sources which respectively appear red, green, and blue coloured.

One of the most important applications of additive colour mixtures is that of the colour cathode ray tube (CRT) [Sproson 1983]. The screen of a colour CRT display is covered with three different phosphors that emit red, green, and blue light respectively when excited by a beam of electrons from an electron gun. The spatial size and arrangement of the phosphors is

such that when the screen is viewed from a sufficient distance, the spectra of these phosphors add at the retina of the observer.

3-4.4 Trichromatic Matching and Primaries

The system of colour specification developed by the CIE is based on *trichromatic matching* [Hunt 1995]. The experimental arrangement for trichromatic matching is shown in Figure 3-6. The test colour is viewed alongside an additive mixture of red, green, and blue light. The intensity of these beams is adjusted until the mixture matches the test colour. Trichromatic matching requires the specification of the red, green, and blue light sources used. The 1931 CIE standard employed monochromatic stimuli of 700nm for red, 546.1nm for green, and 435.8nm for blue. These stimuli are known as *primaries* and denoted ***R***, ***G***, and ***B*** respectively. The constraint on the choice of primaries for trichromatic matching is that none of the primaries can be matched by an additive mixture of the other two.

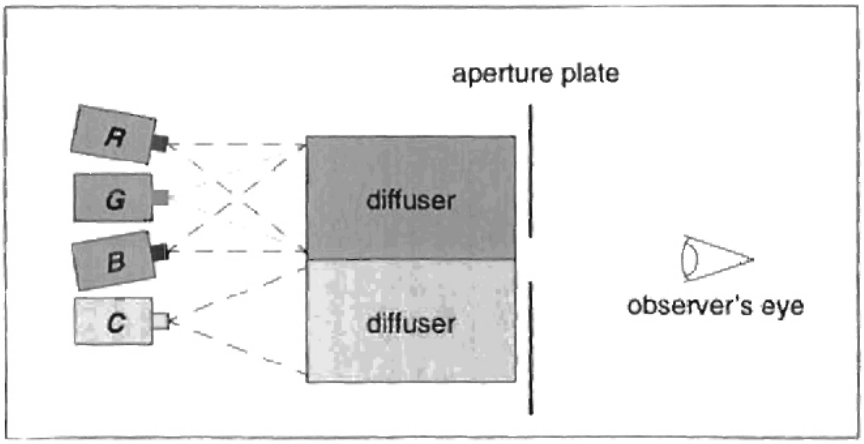


Figure 3-6. Trichromatic matching by additive mixing of three light sources, red ***R***, green ***G***, and blue ***B***, whose intensities can be adjusted. The light source whose colour is to be matched is denoted ***C***. The diffusers result in uniform fields for viewing by the observer [Hunt 1995].

3-4.5 Tristimulus Values

A given colour C can be defined or matched by saying that it is produced by adding R units of the red primary $\boldsymbol{R}$, G units of the green primary $\boldsymbol{G}$, and B units of the blue primary $\boldsymbol{B}$ as described by:

$$C = R\boldsymbol{R} + G\boldsymbol{G} + B\boldsymbol{B} \tag{3-1}$$

where the '+' sign indicates an additive mixture and the '=' sign implies matching.

The results obtained from trichromatic matching are not usually given in the established photometric units for luminance, candelas per square metre (cd/m^2). The reason for this is that

the magnitudes of R, G, and B are typically very unequal. The contribution from the blue primary is especially small compared to that of the red and green primaries. This is a consequence of there being fewer β cones than γ and ρ cones in the retina, the β cones being the more sensitive to short wavelengths. Since white may be regarded as not having an excess of any colour, a new set of units was established where the red, green, and blue contributions are equal for a white light consisting of equal amounts of power per constant-width wavelength interval throughout the spectrum. This stimulus is known as the *equi-energy stimulus* S_E. R, G, and B in the new set of units adopted are known as *tristimulus values*. An example of the conversion to tristimulus units from photometric units for 5.6508 cd/m^2 of the equi-energy stimulus is given in Table 3-1.

	Photometric Units	Tristimulus Units
R	1.0000 cd/m^2	1.0
G	4.5907 cd/m^2	1.0
B	0.0601 cd/m^2	1.0

Table 3-1. The conversion between photometric units and tristimulus units for 5.6508 cd/m^2 of white equi-energy illuminant S_E [Hunt 1995].

3-4.6 Grassman's Laws of Additive Colour Mixture

Additive colour mixtures expressed as tristimulus values obey a powerful series of empirical colour matching laws known as *Grassman's Laws* of which one formulation is as follows [Wyszecki and Stiles 1982]:

1. *Symmetry Law*: If $\boldsymbol{A} = \boldsymbol{B}$ then $\boldsymbol{B} = \boldsymbol{A}$.
2. *Transitivity Law*: If $\boldsymbol{A} = \boldsymbol{B}$ and $\boldsymbol{B} = \boldsymbol{C}$ then $\boldsymbol{A} = \boldsymbol{C}$.
3. *Proportionality Law*: If $\boldsymbol{A} = \boldsymbol{B}$, then $\alpha\boldsymbol{A} = \alpha\boldsymbol{B}$ where α is any positive factor by which the radiant power of the colour stimulus is increased or reduced, while its relative spectral power distribution is kept constant.
4. *Additivity Law*: If $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, and $\boldsymbol{D}$ are any four colour stimuli, then if any two of the following three conceivable colour matches, $\boldsymbol{A} = \boldsymbol{B}$, $\boldsymbol{C} = \boldsymbol{D}$, and $\boldsymbol{A} + \boldsymbol{C} = \boldsymbol{B} + \boldsymbol{D}$, holds good, then so does the remaining match $\boldsymbol{A} + \boldsymbol{D} = \boldsymbol{B} + \boldsymbol{C}$.

3-4.7 Transformations Between Sets of Primaries

The limitation on the choice of primary stimuli, that none of the primary stimuli can be matched by an additive mixture of the other two, means that in the tristimulus representation

the vectors representing the primaries must be linearly independent [Wyszecki and Stiles 1982]. As a consequence there are no set of values R, G, and B which solve (3-2) except the trivial case $R = G = B = 0$

$$RR + GG + BB = 0 \tag{3-2}$$

It is sometimes necessary to transform from one set of primaries $\boldsymbol{R}$, $\boldsymbol{G}$, $\boldsymbol{B}$ to another set of primaries $\boldsymbol{R'}$, $\boldsymbol{G'}$, $\boldsymbol{B'}$. As each primary stimulus of one set can be matched by a mixture of the primaries of the other set, the linear system of (3-3) will hold. Both sets of primary stimuli are linearly independent and the matrix $\boldsymbol{A}$ formed by the coefficients a_{ij} must be non-singular.

$$\begin{bmatrix} \boldsymbol{R'} \\ \boldsymbol{G'} \\ \boldsymbol{B'} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{21} & a_{31} \\ a_{12} & a_{22} & a_{32} \\ a_{13} & a_{23} & a_{33} \end{bmatrix} \begin{bmatrix} \boldsymbol{R} \\ \boldsymbol{G} \\ \boldsymbol{B} \end{bmatrix} \tag{3-3}$$

3-4.8 Negative Tristimulus Values

Although a large range of colours can be matched by an additive mixture of red, green, and blue primaries, there are some colours that cannot be matched in this way [Wyszecki and Stiles 1982]. For example some monochromatic stimuli in the blue-green region are more saturated than any mixture of green and blue primaries. If however the red primary is added to such colours in suitable quantity, it is then possible to match this new colour with a mixture of the blue and green primaries. In such circumstances (3-1) becomes:

$$C + RR = GG + BB \tag{3-4}$$

However, it is more usual to rewrite such expressions in the form:

$$C = -RR + GG + BB \tag{3-5}$$

While (3-5) illustrates how negative tristimulus values occur, negative light flux is a physical impossibility and equations of this type must always be interpreted as (3-4). Sometimes it may be necessary to add two of the primary stimuli to the test colour to achieve a match with the remaining primary. In such cases two of the quantities on the right hand side of (3-5) will have negative signs.

3-4.9 Colour-Matching Functions

The 1931 CIE standard is based on trichromatic matching experiments carried out by two different investigators using a total of 17 British observers with normal colour vision [Hunt 1995]. The results from both experiments were similar and these results were averaged to yield

the 1931 CIE Standard Colorimetric Observer. In particular the amounts of the ***R***, ***G***, and ***B*** primaries needed to match a constant amount of power per small constant-width wavelength interval at each wavelength of the visible spectrum were determined. This data is plotted in Figure 3-7 and such curves are known as *colour-matching functions* and designated $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, and $\bar{b}(\lambda)$, respectively.

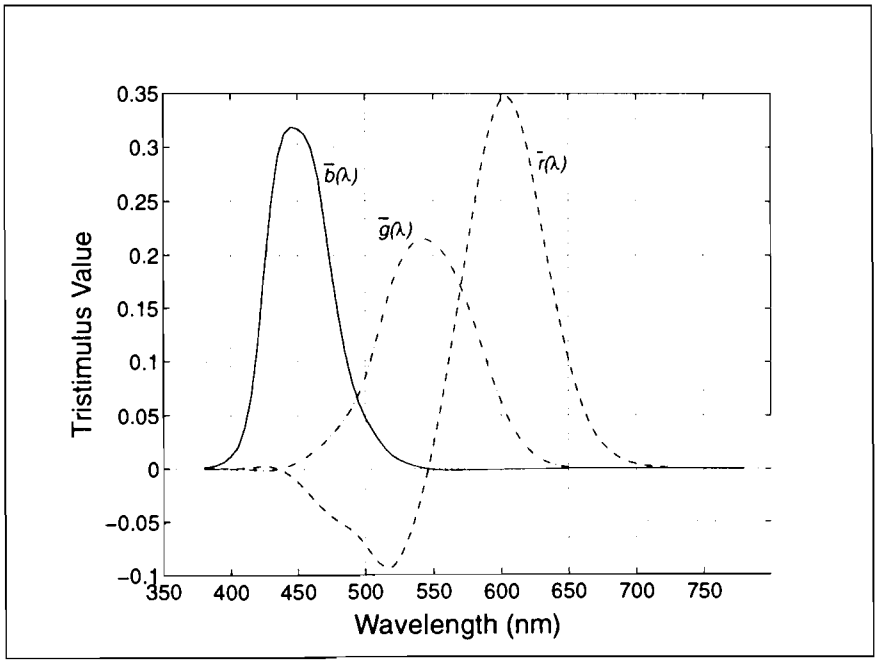


Figure 3-7. The colour-matching functions $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, and $\bar{b}(\lambda)$ for the CIE 1931 Standard Colorimetric Observer, expressed in terms of primaries ***R***, ***G***, and ***B*** consisting of monochromatic stimuli of wavelengths 700 nm, 546.1 nm, and 435.8 nm respectively.

Subsequent investigations have shown that the 1931 CIE Standard Colorimetric Observer represents normal human colour vision in 2^{o} viewing fields adequately. As is to be expected, light of 700 nm is matched by ***R*** only, light of 546.1 nm is matched by ***G*** only, and light of 435.8 nm is matched by ***B*** only, the other two curves being zero at each of these wavelengths. The colour-matching functions also have negative portions which correspond to the need to add this amount of the respective primary to the test colour to enable it to be matched by the other two primaries as was discussed in Section 3-4.8. If different primaries were used for trichromatic matching then the positions of the zeros and the positive and negative portions of the colour-matching functions would change. However, all sets of physical primaries, no matter what their colours, give rise to colour-matching functions having some negative portions to their curves.

3-4.10 The 1931 CIE Standard Colorimetric Observer

In 1931 when the CIE established the system of colour specification it was decided that using a scheme with negative tristimulus values for some colours and negative excursions in the colour matching functions was undesirable. Three new imaginary or non-physical primaries denoted ***X***, ***Y***, and ***Z*** were defined in addition to the primaries ***R***, ***G***, and ***B*** introduced in Section 3-4.4 to allow all real colours ***C*** to be expressed as positive tristimulus values *(X, Y, Z)* according to:

$$C = XX + YY + ZZ \tag{3-6}$$

The transformation between the two sets of primaries was determined such that the corresponding colour matching functions $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$ are entirely positive as shown in Figure 3-8.

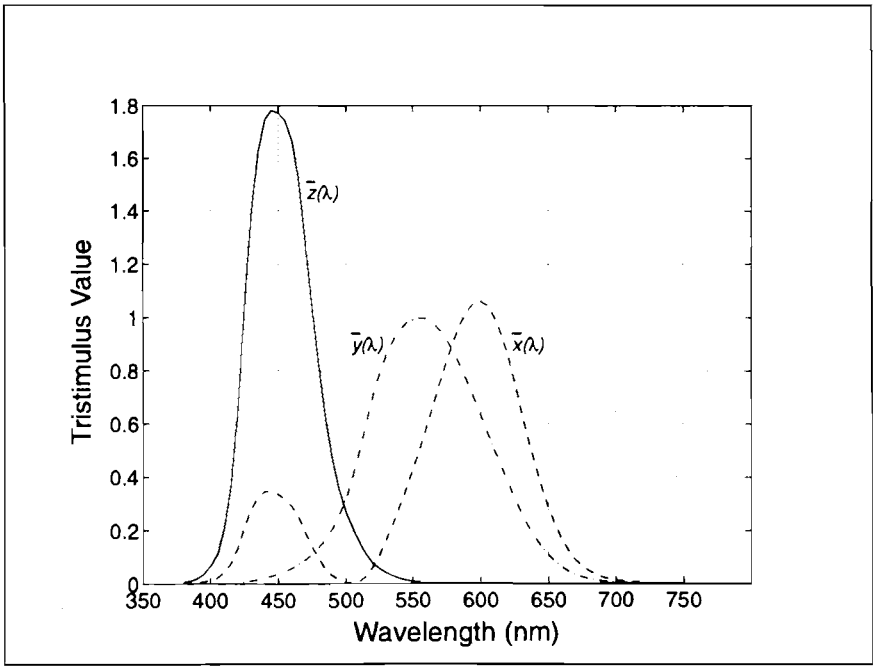


Figure 3-8. The colour-matching functions $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$ for the CIE 1931 Standard Colorimetric Observer, expressed in terms of primaries ***X***, ***Y***, and ***Z*** respectively.

3-4.11 Computing Tristimulus Values for Illuminants

The additivity of trichromatic mixtures means that the colour-matching functions of Figure 3-8 can be used as spectral weighting functions to determine the amounts of ***X***, ***Y***, and ***Z***, needed to match the colour of any illuminant. This requires that the amount of power per small constant-width wavelength interval is known for the illuminant throughout the visible spectrum. The tristimulus values *(X, Y, Z)* for a given illuminant ***C*** with spectral power distribution $P_e(\lambda)$ can be computed using (3-7) where K is a constant. For most applications it is suffi-

cient to replace the integral with a summation of the product of the spectral power distribution and the colour matching function evaluated at every 5 or 10 nm.

$$X = K \int_{380nm}^{780nm} P_e(\lambda)\,\bar{x}(\lambda)\,d\lambda$$

$$Y = K \int_{380nm}^{780nm} P_e(\lambda)\,\bar{y}(\lambda)\,d\lambda$$

$$Z = K \int_{380nm}^{780nm} P_e(\lambda)\,\bar{z}(\lambda)\,d\lambda \qquad (3\text{-}7)$$

The colour matching function $\bar{y}(\lambda)$ was chosen to be the spectral luminous efficiency function $V(\lambda)$ discussed in Section 2-2.2. Therefore the value of Y for a given colour is directly proportional to the luminance L_v of that colour. The constant K can be chosen to yield Y in photometric units.

The relationship between tristimulus values determined in the two sets of primaries used in the 1931 CIE standard, namely ***R***, ***G***, and ***B*** and ***X***, ***Y***, and ***Z***, is described by the linear transformation [Hunt 1995]:

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} 0.49 & 0.31 & 0.20 \\ 0.17697 & 0.81240 & 0.01063 \\ 0.00 & 0.01 & 0.99 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} \qquad (3\text{-}8)$$

3-4.12 Computing Tristimulus Values for Surfaces

For a surface with spectral reflectance function $\rho(\lambda)$ illuminated by a source with spectral power distribution $P_e(\lambda)$ the tristimulus values (X, Y, Z) can be determined using:

$$X = K \int_{380nm}^{780nm} P_e(\lambda)\,\bar{x}(\lambda)\,\rho(\lambda)\,d\lambda$$

$$Y = K \int_{380nm}^{780nm} P_e(\lambda)\,\bar{y}(\lambda)\,\rho(\lambda)\,d\lambda$$

$$Z = K \int_{380nm}^{780nm} P_e(\lambda)\,\bar{z}(\lambda)\,\rho(\lambda)\,d\lambda \qquad (3\text{-}9)$$

When computing the tristimulus values for a surface it is usual to work with relative rather than absolute quantities. The value of K in (3-9) is typically chosen such that the maximum value of Y is normalized to 1.0 or 100 for a perfect diffuser under the same illuminant, according to [Hunt 1995]:

$$K = \frac{1}{\int_{380nm}^{780nm} P_e(\lambda)\,\bar{y}(\lambda)\,d\lambda} \tag{3-10}$$

3-4.13 Metamerism

If two colour stimuli have the same tristimulus values computed using (3-7) or (3-9) they will be matched when viewed under the same conditions by an observer whose colour vision is not significantly different from that characterized by the 1931 CIE Standard Colorimetric Observer. If the two matching colours have the same tristimulus values but different power spectral distributions for an illuminant, or different spectral reflectance functions for a surface, they are said to be *metamers* [Cohen and Kappauf 1982, Hunt 1995].

The phenomenon of metamerism is exploited in colour reproduction systems as it means that the spectral composition that defines each colour in an image need not to be precisely replicated. Instead using an additive colour reproduction system it is possible to use primaries of convenient spectral composition to reproduce a wide range of the original colours. However, in a stricter sense a characteristic of metamerism is that in general absolute colour matching is upset if a different observer is used, or in the case of reflecting surfaces, a different illuminant is used.

3-4.14 Standard Illuminants

The form of (3-9) and (3-10) make it clear that the tristimulus values of a surface determined using one illuminant will not usually be the same found using a different illuminant. The large number of possible illuminants available in practical situations therefore make a rigorous comparison of colorimetric results impossible. This difficulty led the CIE to establish a series of standard illuminants for colorimetric applications, the most important being Standard Illuminant A (or $\boldsymbol{S_A}$), and Standard Illuminant $\boldsymbol{D_{65}}$ [Hunt 1995]. $\boldsymbol{S_A}$ is a convenient representation of tungsten lamps and is available as a calibrated source. $\boldsymbol{D_{65}}$ is a representation of average indoor daylight but is not as straightforward to synthesize as a calibrated source. The relative spectral power distributions defined by the CIE for $\boldsymbol{S_A}$ and $\boldsymbol{D_{65}}$ are shown in Figure 3-9.

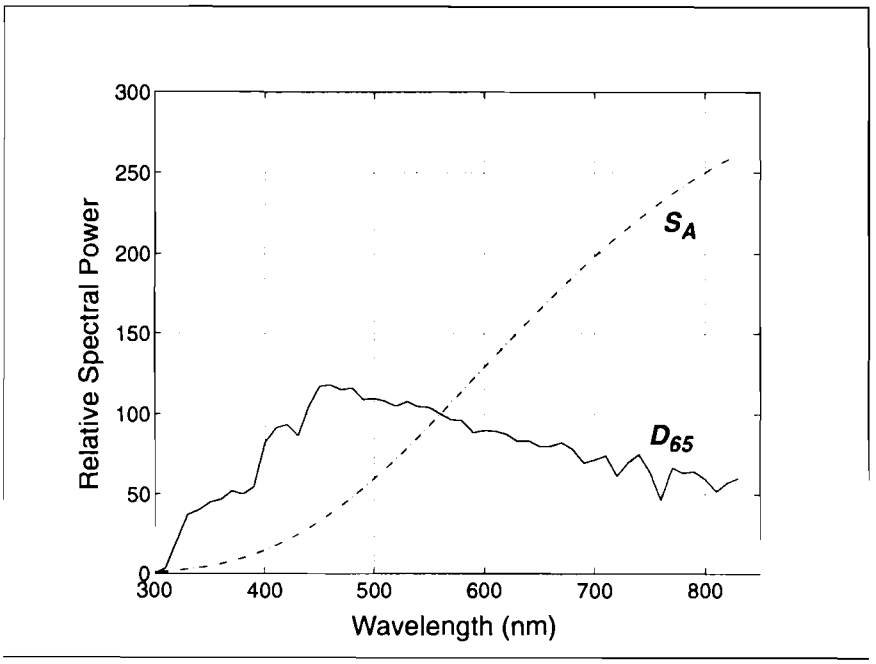


Figure 3-9. Relative spectral power distributions of the CIE Standard Illuminants S_A and D_{65}. Both distributions have been normalized to 100 at 560nm [Hunt 1995].

3-4.15 The Specification of White

The CIE recommends the perfect isotropic diffuser with a reflectance equal to unity as the reference white. Therefore the *white point* for an illuminant can be computed using (3-9) where the spectral reflectance function $\rho(\lambda)$ is set to unity. For example the white point for D_{65} is *(0.9514, 1.0000, 1.0881)* in *(X, Y, Z)* tristimulus values. By convention the white point in *(R, G, B)* tristimulus values is defined as *(1, 1, 1)*.

3-4.16 Chromaticity Diagrams

The *X*, *Y*, and *Z* primaries can be considered to form a colour space *XYZ* in which each colour is defined by a vector given by its tristimulus values *(X, Y, Z)*. The problems with graphically displaying three-dimensional colour spaces has led to various two-dimensional projections or mappings. The most important of these is based on the *chromaticity coordinates* defined as [Wyszecki and Stiles 1982]:

$$x = \frac{X}{X+Y+Z}$$

$$y = \frac{Y}{X+Y+Z}$$

$$z = \frac{Z}{X+Y+Z} \qquad (3\text{-}11)$$

As $x+y+z = 1$ only two variables x and y are needed to describe the chromaticity of a colour and it is possible to construct two-dimensional chromaticity diagrams to graphically represent colorimetric relationships. For example, it can be demonstrated that the chromaticity of a colour formed by mixing any two stimuli lies on a straight line joining the chromaticity coordinates of the two stimuli.

The 1931 CIE chromaticity diagram is shown in Figure 3-10. The spectral locus is the curve obtained for monochromatic stimuli. The straight line joining the long and short wavelengths is known as the *line of purple* and together with the spectral locus encloses the gamut of real colours. The chromaticity coordinates of the ***X***, ***Y***, and ***Z*** primaries lie outside the gamut of real colours hence their description as imaginary or non-physical primaries. The gamut of colours that can be matched by positive amounts of a given set of primaries is bounded by a triangle with the primaries as the vertices. The ***X***, ***Y***, and ***Z*** primaries span the gamut of real colours and all real colours can be matched by positive amounts of these primaries. In contrast the gamut of the ***R***, ***G***, and ***B*** primaries is a subset of the gamut of real colours and colours outside of this range cannot be matched by positive amounts of the ***R***, ***G***, and ***B*** primaries.

Chromaticity diagrams only represent proportions of tristimulus values. As a consequence bright and dim light sources or surfaces having tristimulus values in the same ratios to each other all plot to the same chromaticity coordinates. It is therefore convenient in many colorimetric applications to specify a colour using the triple *(Y, x, y)*. The remaining tristimulus values X and Z can be recovered using (3-12) if required.

$$X = \frac{x}{y} Y$$

$$Z = \frac{1-x-y}{y} Y \qquad (3\text{-}12)$$

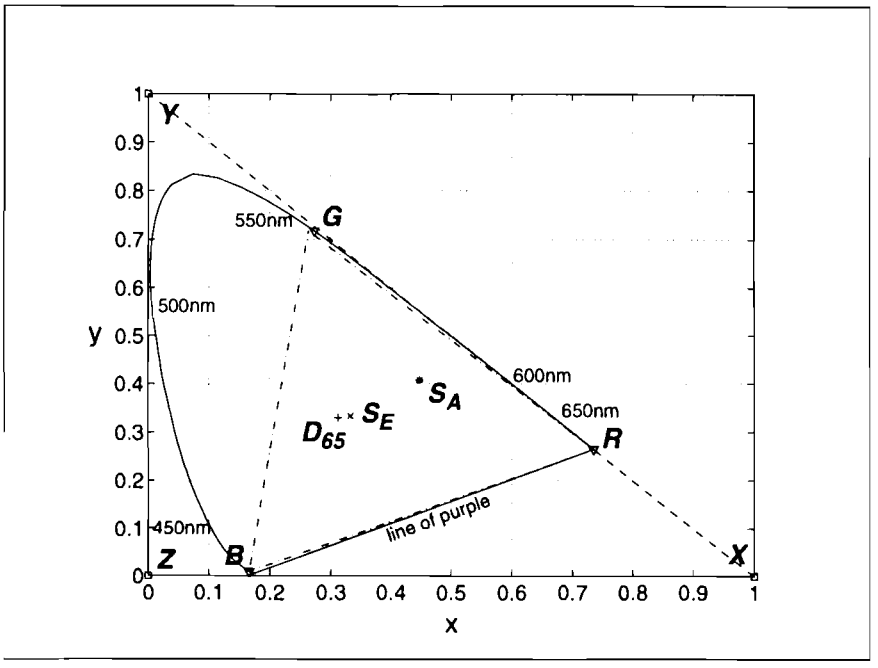


Figure 3-10. The 1931 CIE chromaticity diagram. The spectral locus is graphed with a solid trace and together with the line of purple enclose the gamut of real colours. All real colours can be matched by positive amounts of the imaginary primaries ***X***, ***Y***, and ***Z*** (squares). The gamut of colours that can be matched by positive amounts of the physical primaries ***R***, ***G***, and ***B*** is defined by the triangle with these primaries at its vertices (triangles). The white point of the equi-energy stimulus S_E (×) and the white point of the CIE Standard Illuminants S_A (*) and D_{65} (+) are also plotted.

3-4.17 Perceptually Uniform Colour Spaces

While the *XYZ* colour space and corresponding *xy* chromaticity diagrams are extremely important to colorimetry they are not *perceptually uniform* which is a disadvantage for some applications. A colour space can be said to be perceptually uniform if a small perturbation to a component value is approximately equally perceptible across the range of that value.

Finding a transformation from *(X, Y, Z)* tristimulus values into a reasonably perceptually uniform colour space is not trivial and the CIE decided to standardize to two different systems, the *L*u*v** and *L*a*b** colour spaces, sometimes known as CIELUV and CIELAB respectively [Wyszecki and Stiles 1982].

3-4.18 The 1976 CIE *L*u*v** Colour Space

The transformation from a *(X, Y, Z)* tristimulus value to a *(L*, u*, v*)* triple occurs in two steps [Wyszecki and Stiles 1982]. The intermediate results u', v' and u_n', v_n' are first computed according to (3-13) and (3-14) respectively, where (X_n, Y_n, Z_n) is the tristimulus value of the white point, usually one of the CIE standard illuminants such as D_{65} or S_A.

$$u' = \frac{4X}{X + 15Y + 3Z}$$
$$v' = \frac{9Y}{X + 15Y + 3Z} \tag{3-13}$$

$$u_n' = \frac{4X_n}{X_n + 15Y_n + 3Z_n}$$
$$v_n' = \frac{9Y_n}{X_n + 15Y_n + 3Z_n} \tag{3-14}$$

Using these intermediate results the (L^*, u^*, v^*) coordinates are calculated using (3-15) with the constraint that $Y/Y_n > 0.008856$.

$$L^* = 116\left(\frac{Y}{Y_n}\right)^{\frac{1}{3}} - 16$$
$$u^* = 13L^*(u' - u_n')$$
$$v^* = 13L^*(v' - v_n') \tag{3-15}$$

If $Y/Y_n \leq 0.008856$ then L^* is determined using (3-16).

$$L^* = 903.3\frac{Y}{Y_n} \tag{3-16}$$

3-4.19 The 1976 CIE $L^*u^*v^*$ Colour Difference Formula

While the $L^*u^*v^*$ colour space achieves greater perceptual uniformity than the XYZ colour space this comes at the expense of computational complexity. As a consequence the $L^*u^*v^*$ colour space is not suitable for real-time applications. However, the $L^*u^*v^*$ colour space is often used off-line for measuring and optimizing the colour rendition of television and video systems [Sproson 1983]. For example, (3-17) can be used to compute the colour difference ΔE^*_{uv} between an actual and rendered colour stimulus each in (L^*, u^*, v^*) coordinates.

$$\Delta E^*_{uv} = \sqrt{(\Delta L^*)^2 + (\Delta u^*)^2 + (\Delta v^*)^2} \tag{3-17}$$

It is generally held that a colour difference of 1 corresponds to a "just noticeable difference" between two colour samples. By finding the RMS or mean value of ΔE^*_{uv} over a number of

representative colour samples the colorimetric accuracy of a camera or CRT display can be quantified.

3-4.20 General Colour Acquisition and Reproduction

A number of key issues concerning the practical application of colour science to colour image acquisition and reproduction systems can be illustrated using Figure 3-11.

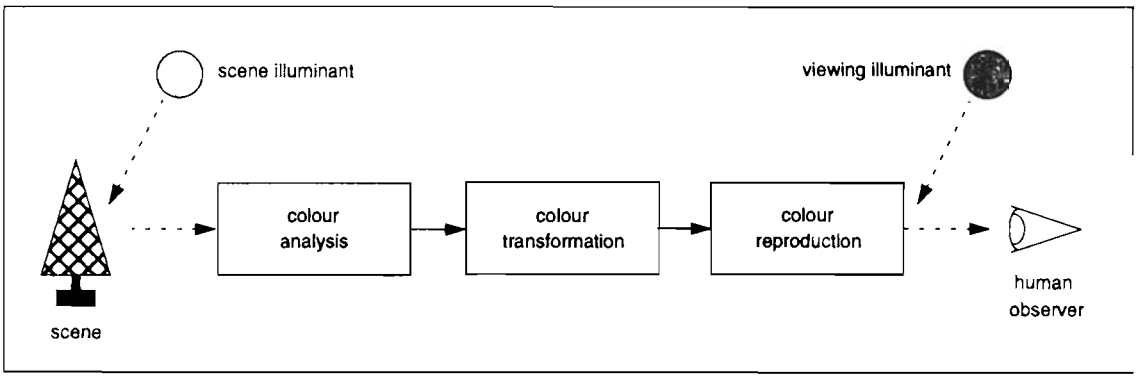


Figure 3-11. A generalized colour image acquisition and reproduction system.

In this example a scene is illuminated by a source with a given spectral power distribution. Some of the radiant flux from the source is reflected from objects in the scene, its spectral composition being modified by the spectral reflectance of the objects. A fraction of this reflected flux is collected by the optical system of the camera. Here the incident spectral power distribution is subjected to a colour analysis to determine the tristimulus values for each resolvable portion of the scene. As discussed in Section 3-4.9 at least three different spectral weighting functions are necessary to analyse a given spectral power distribution and uniquely specify its colour. In the context of solid-state imaging they are known as *colour analysis functions* and to be physically realizable they must be non-negative for all wavelengths.

However, it can be demonstrated that any realizable set of colour analysis functions that overlap in wavelength correspond to imaginary or non-physical primaries that cannot be implemented in any display device or medium [Poynton 1996]. Using the CIE colour matching functions $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$ as examples, it is not possible to find three entirely positive spectral power distributions that when analysed by these functions yield the tristimulus values *(1, 0, 0)*, *(0, 1, 0)*, and *(0, 0, 1)* and hence realize the primaries ***X***, ***Y***, and ***Z***. Furthermore, it can also be shown that the ideal colour analysis functions corresponding to a set of physical primaries are not realizable because they contain negative portions. For example the physical primaries ***R***, ***G***, and ***B*** correspond to the colour matching functions $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, and $\bar{b}(\lambda)$ that are not physically realizable. A colour transformation is therefore necessary to map tristimulus values determined using realizable colour analysis functions with respect to imaginary primaries, into

tristimulus values corresponding to a physical set of primaries associated with colour reproduction.

The colour reproduction stage may be an electronic display such as a colour CRT, or a printing process using inks on paper. In either case the reproduced image is viewed by an observer in an environment with a source of illumination that in general will have a different spectral power distribution than that of the scene.

3-4.21 Objectives of Colour Reproduction

The design of a colour acquisition and reproduction system is dependent on the colorimetric objectives of the colour reproduction stage. Hunt has identified six main types of colour reproduction [Hunt 1970].

1. *Spectral colour reproduction.* This describes a reproduction that is a precise match of the spectral reflectance or spectral power distribution of the original. Spectral colour reproduction will deliver absolute colour accuracy under all illuminants.
2. *Colorimetric colour reproduction.* This describes a reproduction that has the same tristimulus values as the original with respect to the system white point.
3. *Exact colour reproduction.* This describes a reproduction that has not only the same tristimulus values as the original, but has the same absolute luminance.
4. *Equivalent colour reproduction.* This describes a reproduction that under its conditions of viewing is identical to the original under the conditions of viewing of the original. This type of reproduction makes allowances for:
   (a) change of white point.
   (b) differences in levels of illumination or luminance.
   (c) differences in the type of image surround.
5. *Corresponding colour reproduction.* This describes a reproduction that takes items 4(a) and 4(c) into consideration but neglects 4(b). The objective of corresponding colour reproduction is therefore a reproduction that has the same appearance as the original would have if the illumination was the same as that of the reproduction.
6. *Preferred colour reproduction.* This describes a reproduction that allows some colours to be more colourful than in the original. The preferred colours are in accordance with the observer or customers subjective preferences, for example blue sky is preferred to pale, colourless sky.

Not all types of colour reproduction are relevant for all applications [Sproson 1983]. For example spectral colour reproduction is not possible with colour CRT displays but may be desirable for some high quality colour printing applications. Colorimetric colour reproduction

can apply to colour CRT displays if the original scene has the same white point as the display being used. Exact colour reproduction is not usually possible with colour CRT displays because the absolute luminance of the display is necessarily limited and most natural scenes have peak white luminance considerably in excess of this value. Sproson suggests that corresponding colour reproduction is a reasonable and realistic aim for colour television and video systems. Typically however, no allowance is made for differences in the type of image surround suggested in 4(c). Achieving corresponding colour reproduction will be discussed with reference to colour solid-state imager sensors and colour CRT displays in the remainder of this section.

3-4.22 Display Primaries

All practical colour CRT displays use phosphors whose spectral power distributions are relatively broadband as compared to the monochromatic primaries ***R***, ***G***, and ***B*** of the 1931 CIE Standard Colorimetric Observer. Display primaries are selected not only on a colorimetric basis, but on considerations such as cost, suitability for manufacture, and achieving adequate display luminance. The primaries of a colour CRT display are usually specified in chromaticity coordinates along with the white point of the display. As an example the primaries for the NTSC television system with a D_{65} white point are given in Table 3-2 [Poynton 1996].

Color	x	y	z
red	0.67	0.33	0.00
green	0.21	0.71	0.08
blue	0.14	0.08	0.78
white D_{65}	0.3127	0.3290	0.3582

Table 3-2. Chromaticity coordinates of the NTSC primaries and D_{65} white point.

The NTSC primaries and corresponding gamut are shown on the chromaticity diagram of Figure 3-12. Note that while the NTSC primaries have been denoted ***R***, ***G***, and ***B*** they are in fact different from the 1931 CIE primaries introduced in Section 3-4.4 that were also designated ***R***, ***G***, and ***B***. For the remainder of this thesis ***R***, ***G***, and ***B*** will refer to the display primaries and not the 1931 CIE primaries.

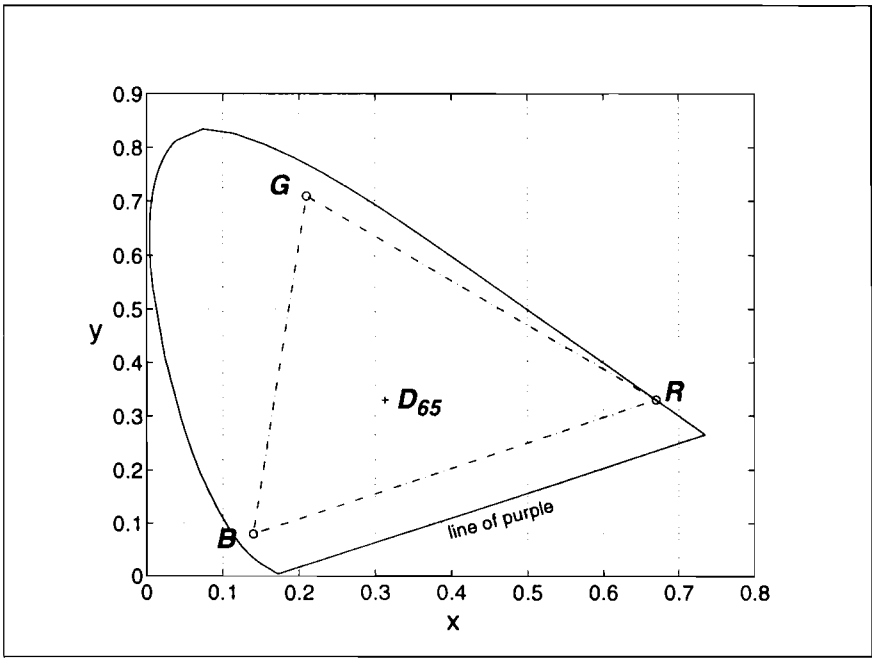


Figure 3-12. The NTSC primaries and colour gamut together with the D_{65} white point (+) on the 1931 CIE chromaticity diagram. The spectral locus is graphed with a solid trace and together with the line of purple enclose the gamut of real colours. The gamut of colours that can be reproduced by positive amounts of the NTSC primaries ***R***, ***G***, and ***B*** is defined by the triangle with these primaries at its vertices. Note that these primaries are different to the 1931 CIE primaries denoted ***R***, ***G***, and ***B*** shown in Figure 3-10.

With reference to Figure 3-12 it can be seen that many real colours lie outside the NTSC gamut and cannot be reproduced on CRT displays that use this set of primaries. This is particularly true of very saturated blue-green colours and colours generated by monochromatic stimuli that lie on the spectral locus.

If the chromaticity coordinates of the display primaries and system white point are known, a linear transformation between the 1931 CIE *(X, Y, Z)* tristimulus values and the *(R, G, B)* tristimulus values in terms of the display primaries can always be found [Sproson 1983]. For the NTSC primaries and D_{65} white point given in Table 3-2 the transformation is given by:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1.9709 & -0.5494 & -0.2974 \\ -0.9538 & 1.9364 & -0.0274 \\ 0.0638 & -0.1294 & 0.9814 \end{bmatrix} \begin{bmatrix} X \\ Y \\ Z \end{bmatrix} \quad (3\text{-}18)$$

The NTSC standard was adopted in 1953 and the specified primaries are representative of phosphors used in colour CRTs of that era. Since that time the phosphors used in colour CRTs have changed and the original NTSC primaries are now obsolete. A number of different stand-

ards now exist such as Rec. 709, EBU Tech. 3213, and SMPTE RP 145 [Poynton 1996]. However, in practice there can be significant variations between the primaries of colour CRTs that profess to adhere to the same standard, either by design or due to manufacturing tolerances. For applications requiring the highest level of colorimetric accuracy the chromaticities of the display primaries and white point should be measured and the exact transformation determined.

3-4.23 Ideal Colour Analysis Functions

The ideal colour analysis functions that correspond to a given set of display primaries can be found from the 1931 CIE Standard Colorimetric Observer colour matching functions $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$ by applying the appropriate transformation of the type given by (3-18). Furthermore it can be shown that the shape of the ideal colour analysis functions are completely determined by the chromaticities of the display primaries and are independent of the choice of white point [Sproson 1983]. Changing the white point simply alters the relative scaling of the colour analysis functions. The ideal colour analysis functions for the NTSC primaries with a $\boldsymbol{D_{65}}$ white point are shown in Figure 3-13. They support the argument of Section 3-4.20 that colour analysis functions corresponding to physical primaries contain negative portions that render them physically unrealizable.

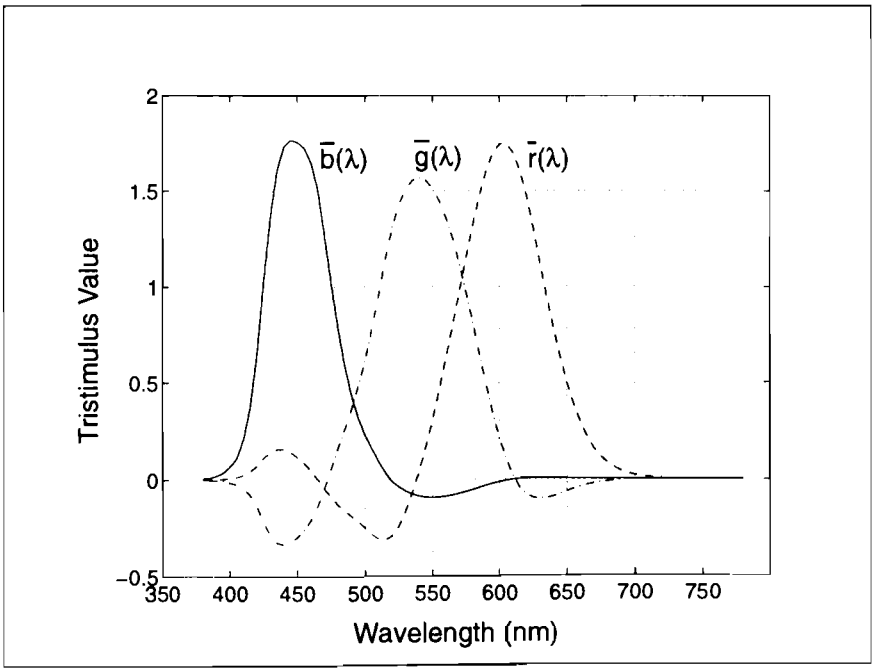


Figure 3-13. The ideal colour analysis functions $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, and $\bar{b}(\lambda)$ corresponding to the NTSC primaries with a $\boldsymbol{D_{65}}$ white point. Note that the ideal NTSC colour analysis functions denoted $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, and $\bar{b}(\lambda)$ should not be confused with the 1931 CIE colour matching functions also designated $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, and $\bar{b}(\lambda)$ in Figure 3-7.

3-4.24 Practical Colour Analysis Functions

Practical colour analysis functions must be entirely positive and are realized using a set of optical filters whose transmittance as a function of wavelength in the visible portion of the spectrum has been carefully designed. In theory the CIE colour matching functions $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$ or any linear combination would make suitable colour analysis functions. A linear transformation could then be found to map each set of tristimulus values precisely to the corresponding colour in terms of the display primaries. In practice finding practical colour analysis functions and the required transformation is significantly more complex due to the performance limitations of solid-state image sensors. The influence of sensor performance on colour processing for solid-state cameras can be illustrated with reference to Figure 3-14. To realize three colour analysis functions denoted $\bar{k}(\lambda)$, $\bar{l}(\lambda)$, and $\bar{m}(\lambda)$ respectively, three optical filters denoted $\tau_k(\lambda)$, $\tau_l(\lambda)$, and $\tau_m(\lambda)$, respectively are selected. However, a characteristic of solid-state image sensors is that their quantum efficiency $\eta(\lambda)$ is not uniform as a function of wavelength. As a consequence the shape of the colour analysis functions $\bar{k}(\lambda)$, $\bar{l}(\lambda)$, and $\bar{m}(\lambda)$ are determined not only by the transmission characteristics of the optical filters $\tau_k(\lambda)$, $\tau_l(\lambda)$, and $\tau_m(\lambda)$, but the shape of the sensor quantum efficiency function $\eta(\lambda)$.

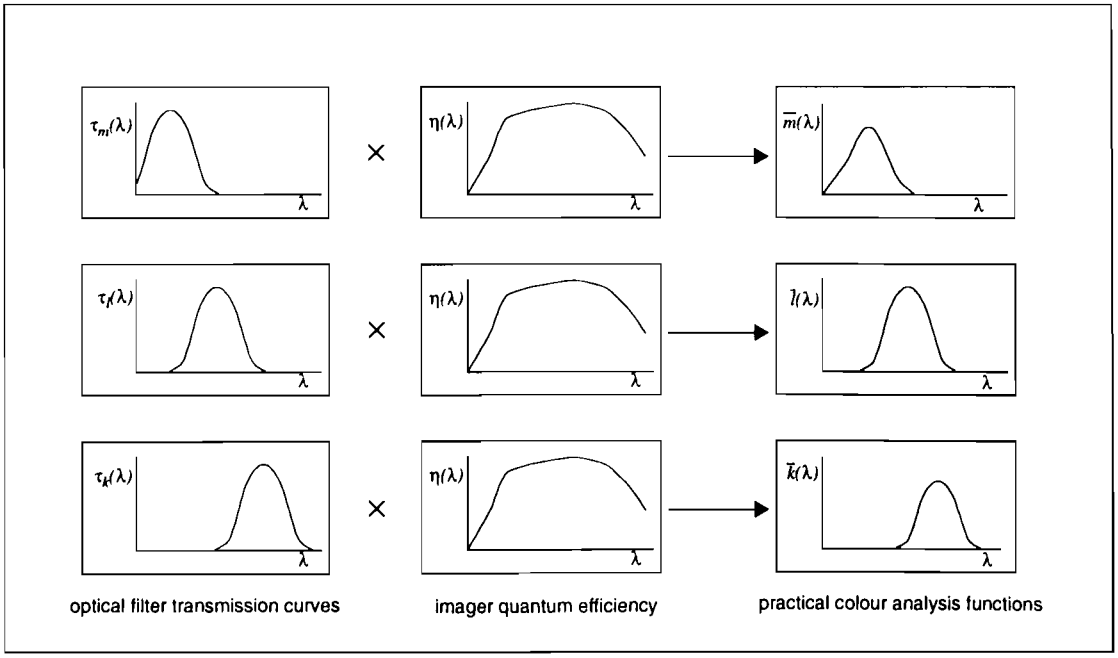


Figure 3-14. Practical colour analysis functions are realized as the combination of the optical colour filter curves and the shape of sensor quantum efficiency.

The form of the colour analysis functions $\bar{k}(\lambda)$, $\bar{l}(\lambda)$, and $\bar{m}(\lambda)$ determine the number of photon generated carriers collected by the corresponding *K*, *L*, and *M* pixels when exposed to a given spectral power distribution. Under normal operating conditions the signal-to-noise ratio (SNR) of a solid-state image sensor is proportional to the square root of the number of carriers

collected [Theuwissen 1995]. Therefore it is possible that some choices for $\bar{k}(\lambda)$, $\bar{l}(\lambda)$, and $\bar{m}(\lambda)$ may be optimal in terms of colour rendition but may not provide adequate SNR performance.

Finding the optimum shapes for the filter set $\tau_k(\lambda)$, $\tau_l(\lambda)$, and $\tau_m(\lambda)$ with respect to all of these factors is a significant design task [Engelhardt and Seitz 1993, Vrhel and Trussell 1995]. Typically the cost of accurately manufacturing the optimal filter set means that such designs are only associated with high-end cameras or colour scanners. Consequently the choice of filter sets for high-volume consumer products is restricted to those that can be economically produced with compatibility to the silicon integrated circuit fabrication process. The filters $\tau_k(\lambda)$, $\tau_l(\lambda)$, and $\tau_m(\lambda)$ used with most solid-state colour cameras are drawn from the three primary colours, red, green, and blue, or from the complementary colours, cyan, magenta, and yellow, or from suitable combinations of both primary and complementary colours. A transparent or "white" filter is also often used with complementary schemes. Typical primary and complementary filter sets are shown in Figure 3-15(a) and (b) respectively. From a colorimetric point of view the colour fidelity provided by either primary or complementary filters can be equivalent, depending on the exact form of the characteristics [Parulski 1985].

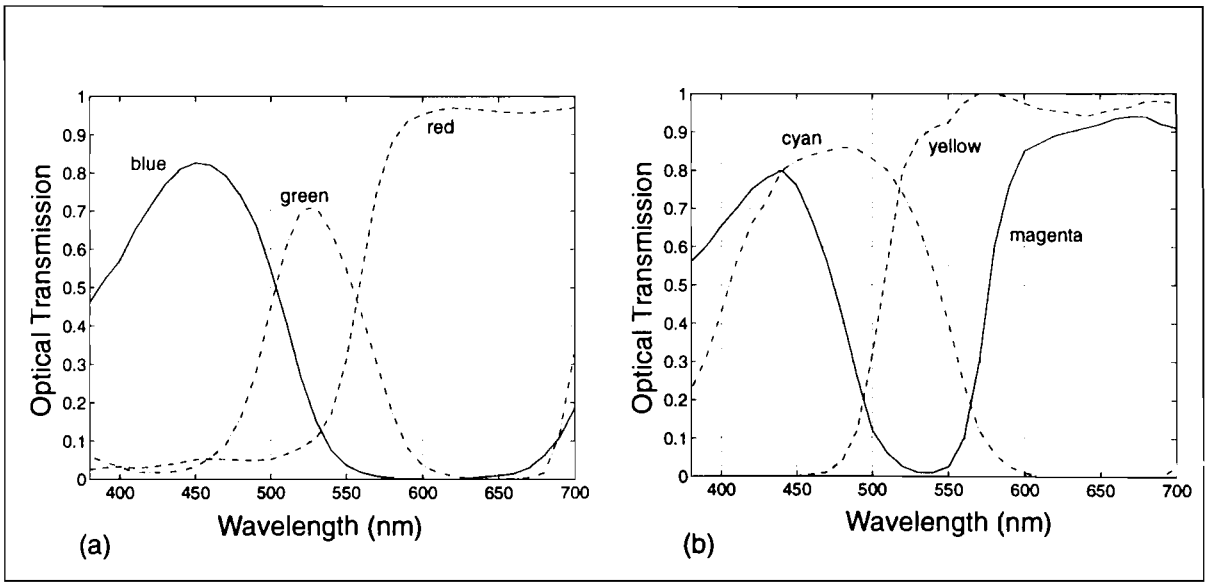


Figure 3-15. Practical colour analysis functions (a) primary (b) complementary.

It can be seen from Figure 3-15 that several of the transmission characteristic have significant optical transmission outside of the visible spectrum. While such characteristics are simpler to manufacture they require the use of a global colour compensating filter to eliminate infrared and ultraviolet wavelengths [Engelhardt and Seitz 1993]. A typical colour compensating filter characteristic is shown in Figure 3-16.

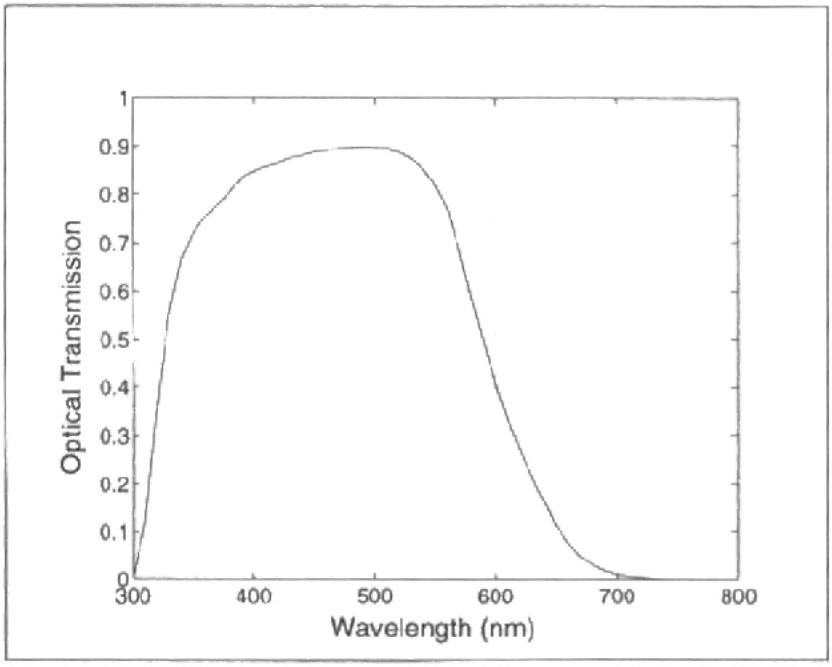


Figure 3-16. Colour compensating filter characteristic.

3-4.25 Colour Filter Arrays

Colour images can be obtained from a single solid-state imager by using a *Colour Filter Array* (CFA) where optical filters are deposited over each pixel in the imaging array so that it responds selectively to a restricted wavelength band [Dillon et al. 1976]. Examples of three different primary CFA patterns and a complementary CFA pattern are shown in Figure 3-17.

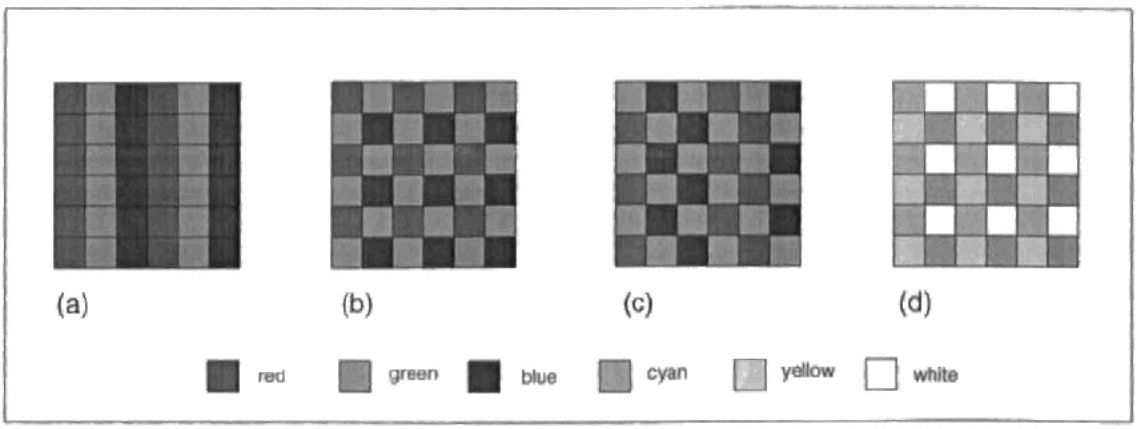


Figure 3-17. (a) Striped red, green, and blue primary CFA (b) mosaic or checkerboard primary CFA (c) alternative checkerboard primary CFA (d) cyan, white, yellow, and green mosaic complementary CFA. Note that each small square outlined in black corresponds to one pixel.

The selection of the CFA used for a camera is important as it significantly determines the obtainable image quality, the camera sensitivity, and the camera signal processing require-

ments [Parulski 1985]. Primary schemes yield simpler colour processing but complementary filters are easier to manufacture [Theuwissen 1995]. In addition to colorimetric considerations the choice of colour filter array design is also determined by the corresponding spatial interpolation scheme.

3-4.26 Spatial Interpolation

The use of a colour filter array requires an interpolation operation to reconstruct three colour components for each pixel from other pixels in close spatial proximity. In the case of a complementary CFA this operation is usually combined with the application of a matrix operation to generate the equivalent red, green, and blue components from the complementary values obtained from the imaging array.

As discussed in Section 2-5.7.2 a solid-state image sensor is a two-dimensional spatial sampling array and as such is subject to spatial aliasing. As the spatial sampling period of each colour component in a CFA is greater than that of the imaging array, aliasing for the colour components in a solid-state colour camera is greater than for the corresponding monochrome camera. Colour aliasing artifacts in interpolated images are particularly visible at sharp colour transitions in the scene, or regions of the scene which contain periodic structure with a high spatial frequency [Holst 1996].

To reduce the visibility of colour aliasing several techniques are commonly employed. It is possible to minimize colour aliasing by optimizing the choice and geometric arrangement of the colour components in the CFA pattern with respect to some analytic criterion [Knop and Morf 1985]. Similarly, interpolation and matrix schemes can be derived to reduce aliasing at certain critical spatial frequencies [Imaide et al. 1986, Ozawa and Takahashi 1991]. Several adaptive interpolation methods using a heuristic approach have also been developed [Hibbard 1995]. The other main technique to reduce colour aliasing is the use of optical low-pass filters made from birefringent crystals to spatially bandlimit the image formed by the camera optical system [Holst 1996].

The choice and optimization of the CFA as well as the interpolation scheme are different for interlace and progressive scan sensor read-out. Optimization must also include the hardware and performance cost of implementing the interpolation scheme as part of a camera system. Evaluation of anti-aliasing schemes must take into account the non-linear performance characteristics of the human visual system. Results obtained from sampling theory do not always yield the desired subjective improvements in image quality.

High-end colour solid-state cameras avoid the need for a colour filter array and spatial interpolation by using a prism to split the light from the camera lens onto three separate solid-state image sensors each with a different colour filter [Theuwissen 1995]. This technique minimizes

colour aliasing but requires careful physical alignment of the optical system and is not as compact or cost effective for consumer applications as using a single solid-state imager and a CFA.

3-4.27 Colour Transformations for Practical Colour Analysis

The colour analysis functions realized with solid-state cameras $\bar{k}(\lambda)$, $\bar{l}(\lambda)$, and $\bar{m}(\lambda)$ are rarely exact linear transformations of the CIE colour matching functions $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$; hence colorimetric errors are introduced during the colour acquisition process. As a consequence an exact transformation between the *(K, L, M)* tristimulus values and the tristimulus values of the display primaries *(R, G, B)* does not exist and it becomes important to find a transformation that minimizes the colorimetric error. In this process it is useful to consider the transformation between the *(K, L, M)* tristimulus values and the tristimulus values of the display primaries *(R, G, B)* as consisting of two consecutive linear transformations denoted ***H*** and ***P*** as shown in Figure 3-18. The transformation ***H*** takes tristimulus values obtained from practical colour analysis *(K, L, M)*, and maps them to CIE *(X, Y, Z)* tristimulus values. The second transformation ***P*** takes the *(X, Y, Z)* tristimulus values and maps them to tristimulus values *(R, G, B)* corresponding to the display primaries.

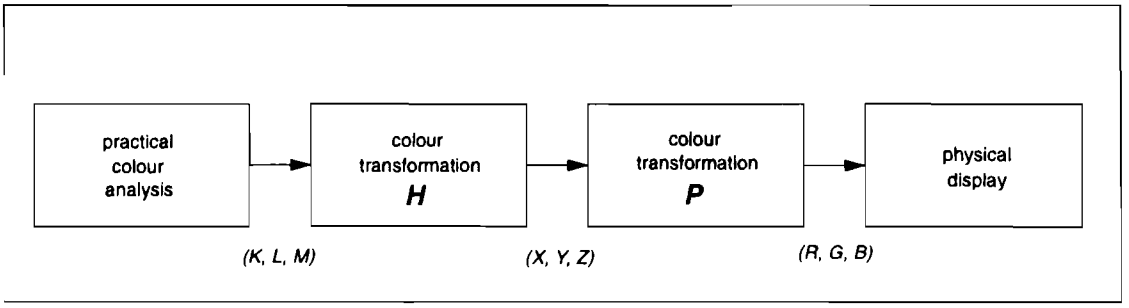


Figure 3-18. The colour transformation between a practical colour analysis and a physical display can be considered as two consecutive transformations, ***H*** and ***P***.

As discussed in Section 3-4.22 if the chromaticity coordinates of the display primaries and system white point are known, an exact transformation ***P*** between the CIE *(X, Y, Z)* tristimulus values and the *(R, G, B)* tristimulus values of the display can always be found [Sproson 1983]. The key task then becomes that of determining the matrix ***H***.

3-4.27.1 Finding the Matrix *H*

The transformation ***H*** that relates *(K, L, M)* and *(X, Y, Z)* tristimulus values can be expressed in the form of (3-19) where the matrix ***H*** is formed from coefficients h_{ij}.

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} & h_{13} \\ h_{21} & h_{22} & h_{23} \\ h_{31} & h_{32} & h_{33} \end{bmatrix} \begin{bmatrix} K \\ L \\ M \end{bmatrix} \text{ or } \begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \boldsymbol{H} \begin{bmatrix} K \\ L \\ M \end{bmatrix} \tag{3-19}$$

The coefficients h_{ij} of the transformation $\boldsymbol{H}$ are usually determined using a number of colour samples for which both the *(K, L, M)* and *(X, Y, Z)* tristimulus values are known. In principle only three such colour samples are required to find the nine unknowns of (3-19). In practice however this approach yields a transformation that gives satisfactory results for the samples used to find the matrix coefficients, but poor results for other colours. This is because it is not possible to find a transformation $\boldsymbol{H}$ that will correctly map the *(K, L, M)* tristimulus values to the corresponding *(X, Y, Z)* tristimulus values for all colours. Most practical techniques for determining the matrix elements h_{ij} use a greater number of colour samples and optimize $\boldsymbol{H}$ to minimize a colour error metric over the range of the colour samples [Suzuki et al. 1990, Engelhardt and Seitz 1993, Lenz and Lenz 1996]. Such optimization schemes for finding $\boldsymbol{H}$ can be generalized as follows:

1. *Selection of Colour Samples.*

   A number of colour samples are selected for the optimization procedure. The choice of colour samples strongly determines the colorimetric performance of the final matrix $\boldsymbol{H}$ delivered by the optimization process. For accurate colour analysis over a large gamut it is desirable to choose colour samples that are evenly distributed over the desired gamut including highly saturated colours and colours at several luminance levels. The uniformity of the distribution of the colours samples can be analysed in a perceptually uniform colour space such as the CIE $L^*u^*v^*$ or CIE $L^*a^*b^*$ colour spaces. Alternatively an application might deem that certain colours are more important than others, for example skin tones, and hence the samples selected might be representative of these colours rather than the complete gamut of possible colours [Sproson 1983]. The number of colour samples n used in the optimization procedure is also important and can range from 15 for a television camera to many hundred for applications requiring high colorimetric precision [Sproson 1983, Suzuki et al. 1990].

2. *Determining Tristimulus Values for the Colour Samples.*

   Once the colour samples have been selected it is necessary to determine the *(K, L, M)* and *(X, Y, Z)* tristimulus values for each of them. The *(K, L, M)* tristimulus values for each colour sample are obtained directly from the camera response with the optical filters $\tau_k(\lambda)$, $\tau_l(\lambda)$, and $\tau_m(\lambda)$. The corresponding *(X, Y, Z)* tristimulus values for each colour sample can be measured using a *colorimeter*[1]. It is important that the *(K, L, M)* and *(X, Y, Z)* tristimulus values are obtained using the same illuminant.

3. *Selection of a Colour Error Metric.*

When the transformation matrix $\boldsymbol{H}$ is applied to the (K, L, M) tristimulus values for each colour sample, estimates of the corresponding (X, Y, Z) tristimulus values are obtained which can be denoted $(\hat{X}, \hat{Y}, \hat{Z})$. A metric is employed to quantify the colorimetric error between (X, Y, Z) and $(\hat{X}, \hat{Y}, \hat{Z})$ that forms the cost function to be minimized by the optimization procedure. The choice of colour error metric has a significant impact on the optimization scheme in terms of the colorimetric performance obtained and the computational effort required.

The simplest error metric to use is the mean squared error (MSE) in the XYZ colour space according to:

$$MSE_{XYZ} = \frac{1}{n}\sum_{r=1}^{n}\left(\left(X_r - \hat{X}_r\right)^2 + \left(Y_r - \hat{Y}_r\right)^2 + \left(Z_r - \hat{Z}_r\right)^2\right) \tag{3-20}$$

However, the *XYZ* colour space is not perceptually uniform. This means that an error metric such as (3-20) does not yield an equal measure of colour error between the (X, Y, Z) and $(\hat{X}, \hat{Y}, \hat{Z})$ tristimulus values for colour samples in different portions of the *XYZ* colour space. For this reason most optimization procedures used in practice employ colour error metrics based on either the CIE $L^*u^*v^*$ or CIE $L^*a^*b^*$ perceptually uniform colour spaces [Suzuki et al. 1990, Engelhardt and Seitz 1993, Lenz and Lenz 1996]. The (X, Y, Z) and $(\hat{X}, \hat{Y}, \hat{Z})$ tristimulus values of each of the colour samples are transformed into the desired perceptually uniform colour space and a colour error metric is then evaluated. For example the MSE in the CIE $L^*u^*v^*$ colour space can be formulated as shown in (3-21) where the (X, Y, Z) and $(\hat{X}, \hat{Y}, \hat{Z})$ tristimulus values for each colour sample have been transformed into (L^*, u^*, v^*) and $(\hat{L}^*, \hat{u}^*, \hat{v}^*)$ tristimulus values respectively using (3-15).

$$MSE_{L^*u^*v^*} = \frac{1}{n}\sum_{r=1}^{n}\left(\left(L^*_r - \hat{L}^*_r\right)^2 + \left(u^*_r - \hat{u}^*_r\right)^2 + \left(v^*_r - \hat{v}^*_r\right)^2\right) \text{ or}$$

$$MSE_{L^*u^*v^*} = \frac{1}{n}\sum_{r=1}^{n}\left(\Delta E^*_{uv}\right)^2 \tag{3-21}$$

1. A colorimeter is an instrument that directly measures the (X, Y, Z) tristimulus values or (Y, x, y) coordinates of a colour sample [Wyszecki and Stiles 1982].

4. *Optimization Procedure for Colour Error Metric Minimization.*

The chosen colour error metric forms a cost function to be minimized by the optimization procedure. The choice of colour error metric determines the computation effort required to minimize the cost function. If the MSE is formulated in the *XYZ* colour space or a colour space linearly related to it, then a closed-form analytical solution can be found using least squares methods. If the MSE is formulated in the CIE $L^*u^*v^*$ or CIE $L^*a^*b^*$ colour space, it is not possible to find a closed-form analytical solution [Vrhel and Trussell 1994]. Instead numerical optimization techniques based on iterative gradient descent methods must be employed [Reklaitis et al. 1983, Chong and Zak 1996].

3-4.27.2 Colour Correction

The transformations $\boldsymbol{H}$ and $\boldsymbol{P}$ are normally determined off-line and combined to yield a single matrix $\boldsymbol{C}$ known as the *colour correction matrix.* The matrix $\boldsymbol{C}$ directly maps the *(K, L, M)* tristimulus values generated by the camera colour analysis to the *(R, G, B)* tristimulus values expressed in terms of the display primaries as described by:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \boldsymbol{C} \begin{bmatrix} K \\ L \\ M \end{bmatrix} \text{ where } \boldsymbol{C} = \boldsymbol{PH} \tag{3-22}$$

The colour correction matrix is implemented in hardware in solid-state cameras and significantly improves the colorimetric accuracy by electronically realizing the negative excursions of the colour analysis functions required for ideal colour analysis [Parulski 1985]. However, in addition to improving the colour rendition the colour correction matrix increases the noise in the reproduced image. This is because the matrix typically includes coefficients whose absolute value is greater than one. As the noise in the *K, L,* and *M* pixels is independent, the output noise variance in the *R, G,* and *B* values is increased in proportion to the square root of the sum of the squares of the corresponding matrix coefficients. The colour correction matrix also amplifies colour aliasing artifacts generated by the spatial interpolation operation. As a consequence the signal-to-noise performance of the solid-state image sensor used as the basis of a colour camera must have sufficient margin prior to the application of the colour correction matrix to support high image quality.

3-4.28 Colour Constancy and White Balance

One of the most important practical uses of colour is as an aid to the recognition of objects. However objects can be illuminated under a large range of conditions in terms of the luminance and colour of the illuminant. The human visual system is extremely adept at compensating for such changes in illuminance and objects tend to be recognized as having nearly the

same colour under many different illuminants [Hunt 1995]. This adaptive behaviour of the human visual system is known as *colour constancy.*

Providing colour constancy with an electronic imaging system poses a number of challenges. In principle for each different scene illuminant the colour correction matrix C could be re-determined using the procedure outlined in Section 3-4.27. However, this is not generally practical and instead techniques based on maintaining *white balance* are employed. To ensure that scene white appears white in the reproduced image the relative gains of the *(K, L, M)* channels are adjusted to give *(1, 1, 1)* under changes in the illuminant. As typical scenes may not contain a satisfactory reference white, practical white balance algorithms must make various assumptions to achieve white balance, for example that the integrated tristimulus values of an entire image correspond to white. The success of white balance methods is determined in part by the structure and colour of objects within the image scene [Morimura et al. 1990, Liu et al. 1995].

3-5. Digital Colour Camera Architecture

The principles of colour science and characteristics of electronic display devices both play a role in determining digital camera architecture. Having introduced the relevant concepts in each of these areas the architecture of a generic digital cameras can now be discussed with reference to Figure 3-19.

3-5.1 Optical Components and Image Sensor

The optical lens assembly may include a mechanical shutter, iris, and zoom function. With the exception of high-end cameras most digital cameras use a single solid-state image sensor with a colour filter array.

3-5.2 Analog Processing and Analog-to-Digital Conversion

The output from the image sensor is an analog voltage and it is usual to apply several analog signal conditioning techniques such as correlated-double sampling (CDS) and automatic gain control (AGC). This improves the signal-to-noise ratio (SNR) and maximizes the utilization of the analog-to-digital converter input range. Due to reliability, ease of design, and the ability to realize drift-free manufacturable systems with no adjustable components, the remainder of the camera processing is normally performed in the digital domain [D'Luna and Parulski 1991]. Digital processing also allows the accurate implementation of complex image processing algorithms to improve image quality [Netravali and Haskell 1988]. An analog-to-digital converter is therefore required to digitize the pixel values.

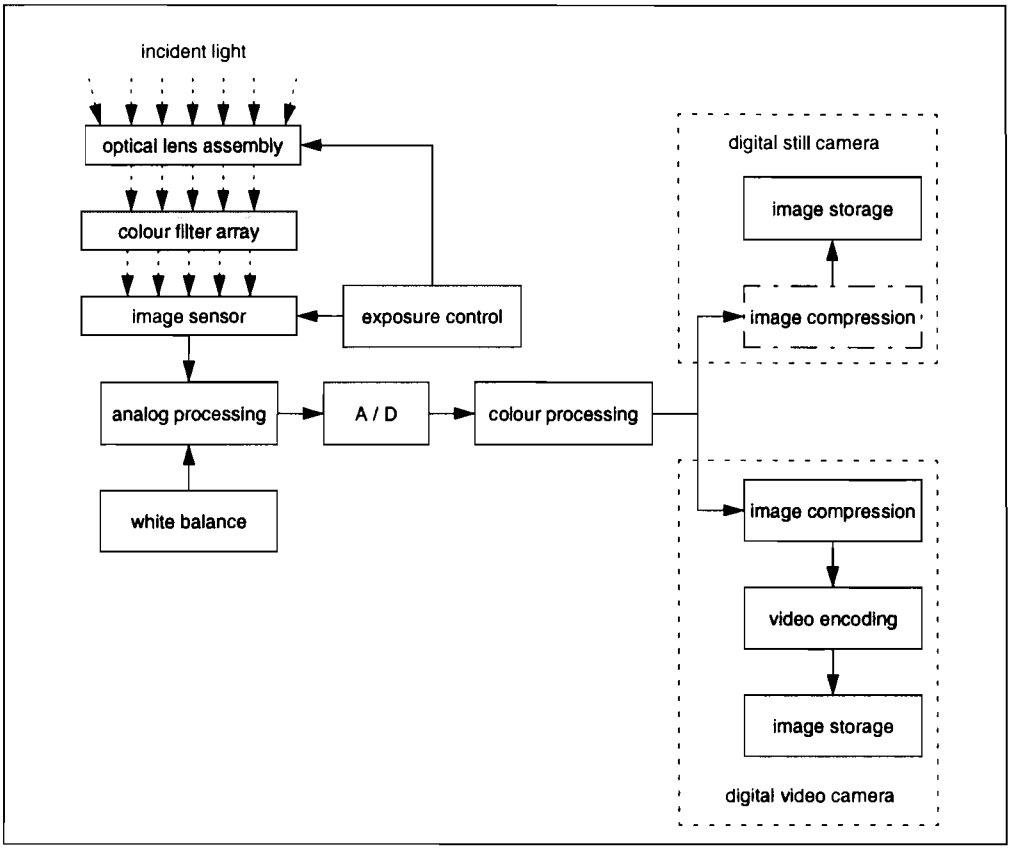


Figure 3-19. Generic architecture of a digital colour camera system. Note that high-end digital still cameras generally do not perform image compression, and tethered digital cameras do not usually store images internally [Parulski and Jameson 1996].

3-5.3 Colour Processing

A significant proportion of the architecture of digital colour cameras is associated with colour processing. The typical colour processing stages are shown in Figure 3-20.

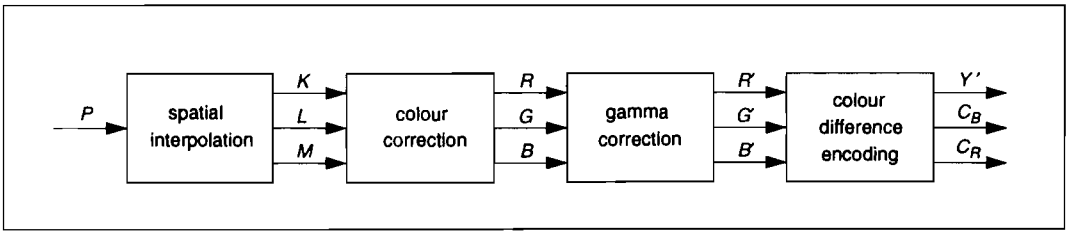


Figure 3-20. Colour processing stages for a digital camera. P represents digitized pixel values from the image sensor, *(K, L, M)* and *(R, G, B)* represent linear tristimulus values from spatial interpolation and colour correction respectively, *(R', G', B')* represent non-linear tristimulus values after gamma correction, and the *(Y', C_B, C_R)* represent non-linear luma and chroma components [Poynton 1996].

Spatial interpolation, colour correction, and gamma correction have already been discussed in Section 3-4.26, Section 3-4.27.2, and Section 3-3.5 respectively. Colour difference encoding is a requisite step for efficient image compression schemes such as JPEG or MPEG. The human visual system has considerably less spatial acuity for colour information than brightness [Poynton 1996]. As a consequence it is advantageous to transform the image colour information into a component representative of brightness, known as luma Y', and blue and red chroma components, C_B and C_R respectively. The standard transformation is given by:

$$\begin{bmatrix} Y' \\ C_B \\ C_R \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.144 \\ -0.169 & -0.331 & 0.5 \\ 0.5 & -0.419 & -0.081 \end{bmatrix} \begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} \tag{3-23}$$

Once the colour difference signals C_B and C_R have been formed they can be subsampled using decimation filters to reduce bandwidth or data size without a perceivable loss in image quality [Poynton 1996]. Two common digital colour difference image formats known as 4:2:0, sometimes called 4:2:2, and 4:1:1 respectively are illustrated in Figure 3-21.

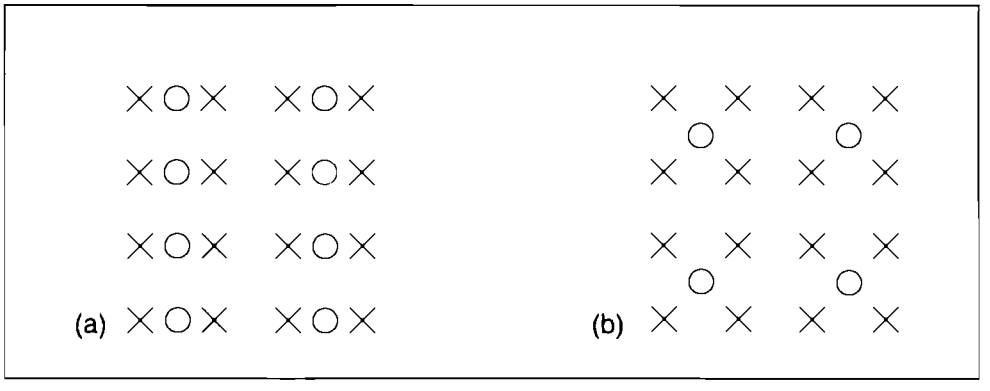


Figure 3-21. (a) 4:2:0 (4:2:2), and (b) 4:1:1 colour difference formats. The luma Y' and red and blue chroma components C_B and C_R are represented by X and O respectively [Poynton 1996].

3-5.4 Image Compression, Digital Video Encoding, and Image Storage

The cost of a digital camera is significantly determined by the storage medium employed for the image data. The available storage technologies include EPROM, hard drives, and magnetic tape. Due to the cost per megabyte of storage, image compression techniques are normally employed with the EPROM technology used in low-end digital still cameras [Izawa et al. 1990]. High-end digital still cameras do not perform compression to maintain the highest possible level of image quality, and instead use a hard drive to store the large amount of image data [Parulski and Jameson 1996]. Digital video is recorded on a magnetic tape after image

compression and error correction techniques have been applied as part of the video encoding process [Doyle]. In general, image storage is not provided by tethered digital cameras and image data is directly transferred to the host computer as it is acquired. However, to satisfy the bandwidth limitations of the digital interface used to transfer the image data, it is often necessary to perform image compression [Connectix]. This may require a frame store. The image compression techniques used in digital cameras range from adaptive discrete cosine transform (ADCT) methods such as JPEG and MPEG that require the image data in $Y'C_BC_R$ format, to proprietary techniques that operate directly on the pre-interpolated pixel data produced by the image sensor with a CFA [Izawa et al. 1990, Parulski and Jameson 1996].

3-5.5 Exposure Control and White Balance

To prevent image saturation sensor exposure can be controlled using a number of methods such as a mechanical shutter or iris, electronic shutter, and gain control prior to analog-to-digital conversion [Theuwissen 1995]. The sensor exposure level is measured using a metric either computed from the image data, or determined directly by an additional calibrated light sensing device inside the camera optical assembly. Automatic exposure control is provided by algorithms that adjust the exposure level based on an exposure metric using one or more of the aforementioned methods [Morimura et al. 1990, Andersson and Shelby 1994].

To maintain accurate colour rendition under changes in the colour of the scene illuminant, the gains applied to each of the tristimulus components produced by the image sensor are modified. Automatic white balance algorithms are based on colour metrics computed from the image data, or measured using additional calibrated colour sensors placed inside the camera optical assembly [Hanma et al. 1983, Imaide et al. 1990, Morimura et al. 1990, Liu et al. 1995]. Shifts in the colour temperature of the illuminant are detected and the gains required to maintain white balance are determined and applied.

3-5.6 Advanced Camera Features

Many digital colour cameras support features in addition to those shown in Figure 3-19. These include aperture correction, defect concealment, automatic focus and zoom, and image stabilization [Chan and Youe 1995, Liu et al. 1995, Holst 1996].

3-6. Conclusion

The system level requirements for realizing a digital colour camera are largely independent of the solid-state sensor technology. For example, the colour processing used with a CCD sensor can be employed in an identical fashion with a CMOS sensor. As the incumbent technology, CCDs are at present used in almost all digital camera products released to date [Parulski

and Jameson 1996]. This means that hardware implementation of the various subsystems is partitioned between a number of CMOS integrated circuits in addition to the CCD sensor. Achieving reductions in power dissipation, size, and cost without further camera system integration is difficult.

In comparison, CMOS APS technology is fully compatible with camera system integration. Furthermore, CMOS image sensors are inherently lower power than their CCD counterparts. This presents the possibility of extremely low-power, compact digital cameras manufactured in CMOS. For this proposition to be successful, two key questions must be answered: "Can a colour CMOS APS sensor deliver the imaging performance required?", and "What influence will significant camera system integration have on sensor performance?". These issues will be addressed in Chapter 4 and Chapter 5, respectively.

CHAPTER 4 Performance Analysis of a Colour CMOS Photogate Image Sensor

4-1. Introduction

CMOS active pixel sensor technology (APS) has been promoted as an alternative solid-state imaging technology to CCD that has significant advantages in terms of low power dissipation, scaling to high resolution formats, and compatibility with camera system integration [Fossum 1993]. Techniques based on correlated-double sampling (CDS) have been developed to reduce fixed-pattern noise (FPN) due to mismatch in the read-out circuits, traditionally the factor limiting the performance of CMOS image sensors [Mendis et al. 1994a]. The possibility of manufacturing high performance image sensors in a standard CMOS fabrication process could substantially lower the technology barrier and allow many new players to enter the solid-state imaging market. However, despite the intense interest in CMOS active pixel sensors in recent years, a detailed performance comparison between CMOS APS technology and CCD technology has not yet been reported. Furthermore, the performance limitations of the present generation of CMOS APS image sensors have not been rigorously established. The identification of these performance limitations is essential to guide the development of future generations of CMOS APS sensors. In this chapter the performance of a state-of-the-art colour CMOS photogate active pixel sensor is experimentally evaluated and compared with that of other CMOS and CCD sensors. The sensor performance limitations are identified and directions for research needed to address these issues are presented.

This chapter is lengthy and divided into 12 main sections in addition to the introduction and conclusion. The first section describes the architecture and operation of the photogate sensor, and the details of the colour filter array. The following section briefly introduces the acquisi-

tion system and the performance definitions used to evaluate the sensor. The performance of the photogate sensor is then analysed in terms of ten important performance characteristics, namely dark current, read noise, optical sensitivity, signal-to-noise ratio, dynamic range, charge transfer noise, conversion gain, fixed-pattern noise, quantum efficiency, and colorimetric accuracy. Each of these topics forms a section in which the corresponding experiment(s) are described, relevant analysis is performed, the results compared to values reported for other CMOS and CCD sensors, and implications for the development of future generations of CMOS APS sensors are discussed. The performance analysis of the photogate sensor is summarized in the final section of this chapter, and conclusions are drawn regarding the production of high quality image sensors in CMOS.

4-2. The Photogate Active Pixel Sensor

A 352 × 288 photogate active pixel sensor was used as the subject of this experimental investigation. This sensor was designed by Sunetra Mendis, a former member of technical staff at Bell Laboratories, and fabricated in a Lucent Technologies, single-poly, 0.8-μm CMOS process. To improve optical sensitivity and quantum efficiency the formation of silicide on the photogates was blocked during manufacture. A colour version of this photogate sensor was produced by the deposition of a colour filter array (CFA). Colour photogate sensors were also manufactured with microlenses to increase the effective pixel fill factor, a technique widely used with CCD sensors to improve the optical sensitivity [Theuwissen 1995]. In this section the architecture and operation of the photogate sensor are described, together with the photogate pixel design, and the CFA pattern and transmission characteristics.

4-2.1 Architecture of the Photogate Sensor

The architecture of the sensor follows prior single-poly photogate designs with the inclusion of a crowbar circuit to support a second level of correlated-double sampling [Mendis et al. 1994a, Dickinson et al. 1995a]. The architecture of the photogate sensor is shown in Figure 4-1.

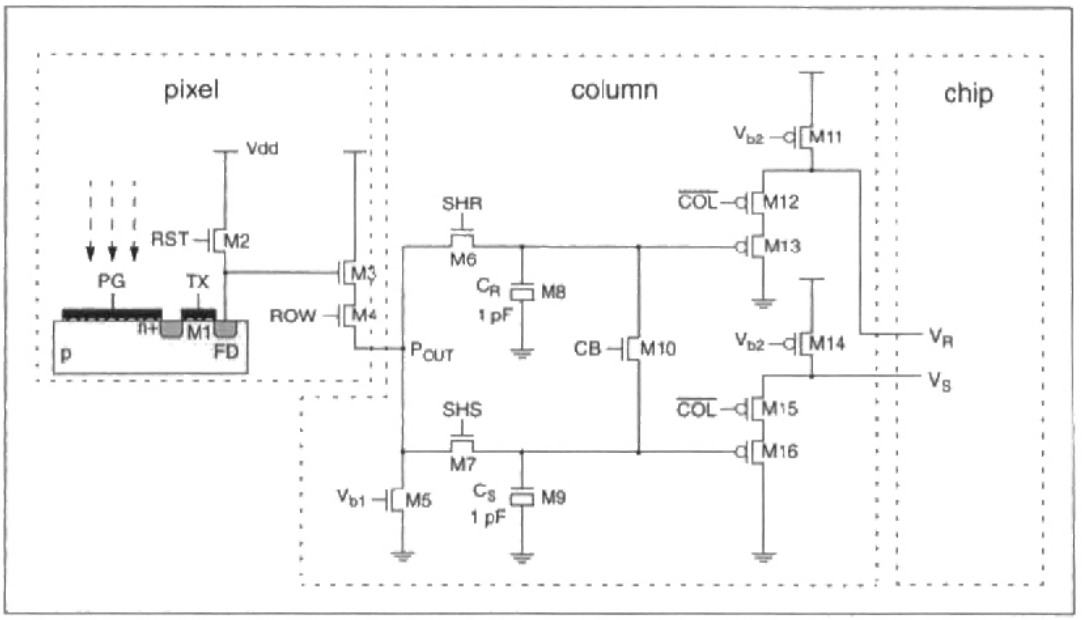


Figure 4-1. Photogate sensor architecture.

In addition to the circuits given in Figure 4-1, to perform two levels of correlated-double sampling requires a configuration of differential amplifiers and sample-and-hold stages as shown in Figure 4-2. These components were not realized as part of the sensor chip and instead were implemented at the board level.

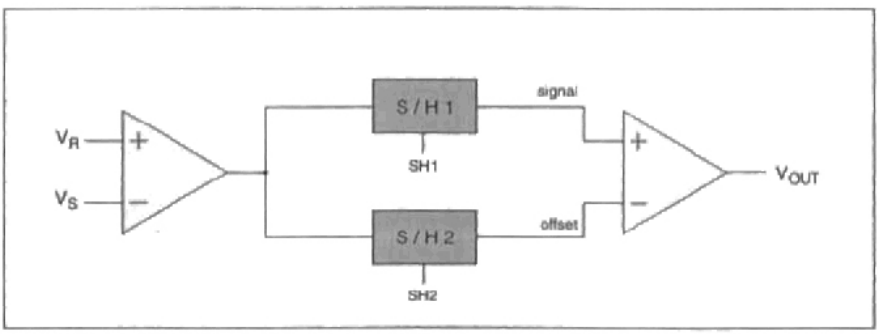


Figure 4-2. Additional circuitry required for correlated double sampling.

4-2.2 Photogate Sensor Operation

The operation of the photogate image sensor can be explained with the aid of the timing diagram shown in Figure 4-3. During integration the polysilicon photogate *PG* is held at *Vdd* and photon generated electrons are collected in the potential well beneath the gate. The transfer device *M1* is DC biased at 0.7V isolating the collected charge under the photogate from the floating diffusion node *FD*. For sensor read-out each row is addressed in turn with the row decoding logic (not shown in Figure 4-1) driving the appropriate row line *ROW* to *Vdd*. The

FD node of the pixels in the row are reset to a voltage approximately one threshold voltage drop below *Vdd* by pulsing *RST*. The reset operation introduces uncertainty into the *FD* reset level due to thermal noise and the threshold voltage drop across *M2*. The reset level is buffered by the source follower formed by devices *M3-M5* and is sampled on the gate capacitance C_R by pulsing *SHR*. Electrons collected under the photogate are then transferred to the *FD* node via transfer device *M1* by pulsing *PG* to ground. The signal electrons displace the *FD* voltage and this level is sampled on the gate capacitance C_S by pulsing *SHS*. The sampling of the pixel reset and signal levels by the column circuits is carried out in parallel for each pixel in the selected row and occurs in the line blanking interval.

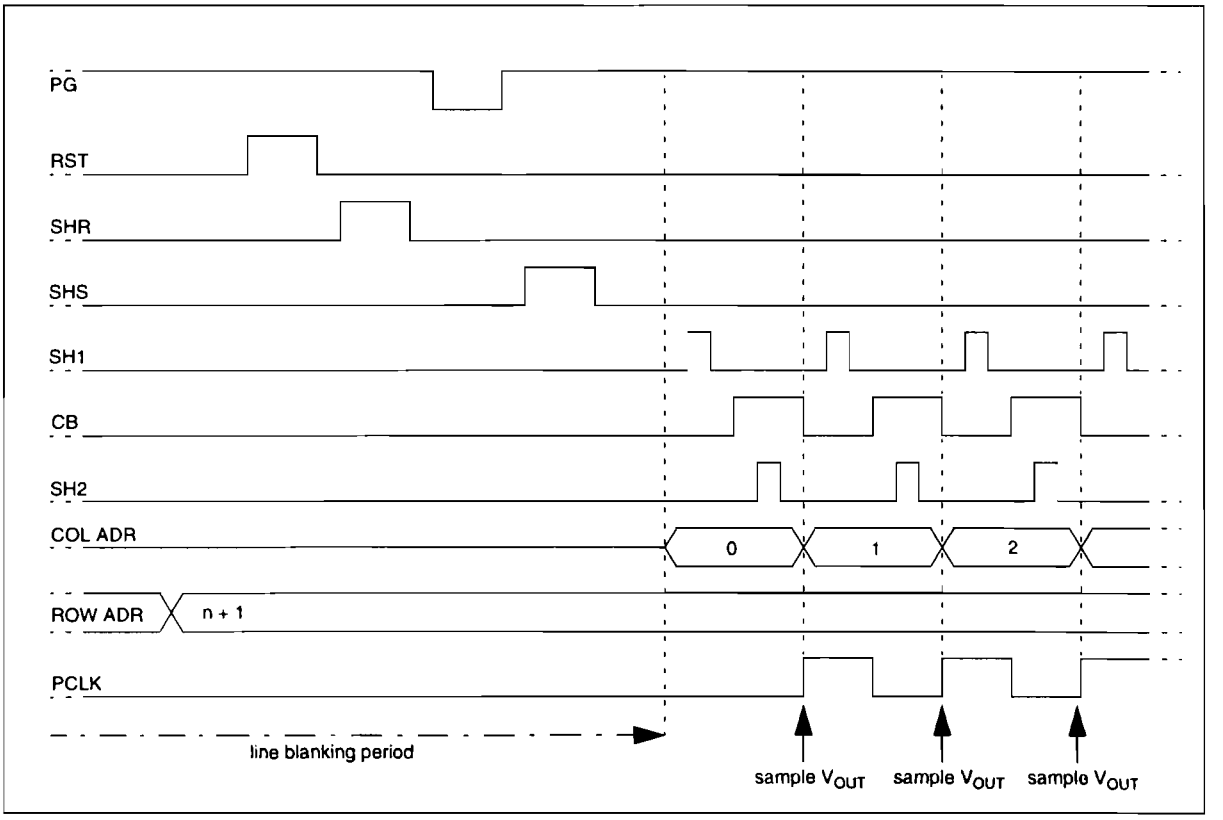


Figure 4-3. Timing diagram for the photogate sensor.

To generate the image signal, each column of the sensor is then addressed in turn by the column decoding logic (not shown in Figure 4-1) by driving the $\overline{COL}$ signal to ground. The column source followers formed by devices *M11-M16* buffer the sampled reset and signal levels onto common buses denoted V_R and V_S respectively. To perform the first stage of CDS the first differential amplifier in Figure 4-2 subtracts the signal and reset levels. This removes the reset noise component and pixel offset mismatch due to devices *M2*, *M3*, and *M4*. This signal level is stored in sample-and-hold stage S/H1 by pulsing *SH1*. To perform the second level of CDS, also known as crowbar, the *CB* signal is driven high and the first differential amplifier forms the offset difference of the column source followers. This offset is stored in sample-and-hold

stage S/H2 by pulsing *SH2*. A final differential amplifier delivers the image signal V_{OUT} with column offsets removed that is digitized on the rising edge of the pixel clock *PCLK*.

4-2.3 Photogate Pixel Design

The layout of the photogate pixel is given in Figure 4-4. Vertical buses in metal1 are used for *Vdd* and P_{OUT} while horizontal buses in metal2 are used for the *PG*, *ROW*, and *RST* signals. The *TX* bias voltage is supplied by a horizontal bus in polysilicon. The large shaded area is the polysilicon photogate which occupies 35% of the pixel area. The pixel dimensions are 16.0μm × 16.0μm and the drawn pixel fill factor is 35%.

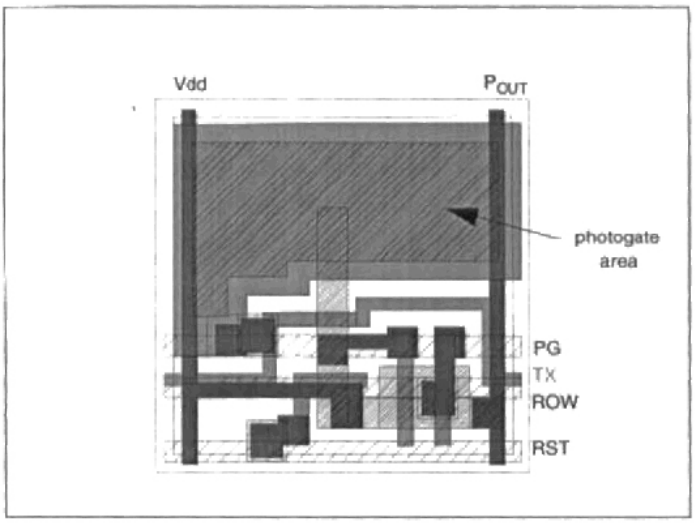


Figure 4-4. Photogate pixel layout.

4-2.4 Colour Filter Array Pattern

A colour photogate sensor was produced from the monochrome imager by the deposition of a polyamide CFA [Dillon et al. 1976]. The CFA pattern used was the Bayer checkerboard as shown in Figure 4-5 [Bayer 1976]. The checkerboard pattern provides superior horizontal resolution than stripe CFA patterns at the expense of diagonal resolution where the acuity of the eye is poor [Parulski 1985]. A primary CFA was used in preference to a complementary CFA to simplify the subsequent stages of colour processing.

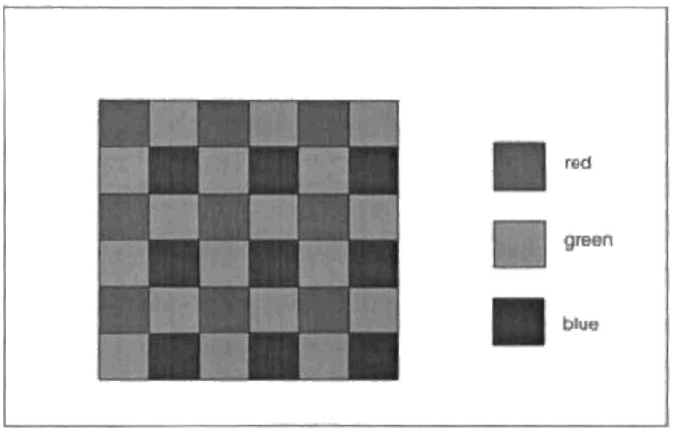


Figure 4-5. Colour filter array checkerboard pattern.

4-2.5 Colour Filter Array Transmission Characteristics

The design of optimal colour filter transmission characteristics for colour solid-state image sensors is a complex procedure [Engelhardt and Seitz 1993, Vrhel and Trussell 1995]. Many applications do not require the additional colorimetric accuracy afforded by optimal colour filter transmission characteristics, or the cost of manufacturing custom colour filter transmission characteristics precludes their use. As the photogate sensor was targeted towards low cost video conferencing and multi-media applications a set of colour filter transmission characteristics was selected from a range supplied by a manufacturer. The CFA transmission characteristics of the colour photogate sensor are given in Figure 4-6.

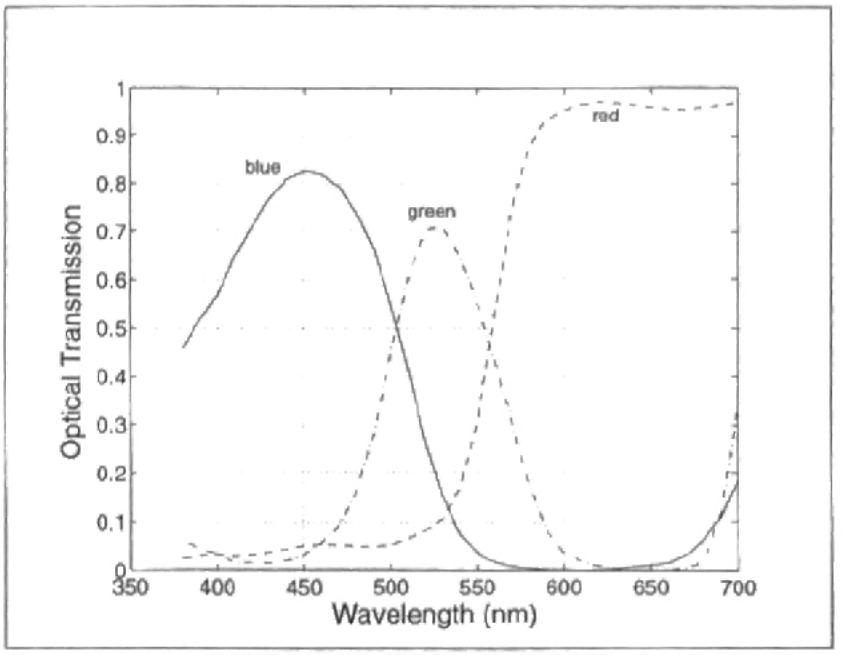


Figure 4-6. Colour filter optical transmission characteristics.

It can be seen from Figure 4-6 that the red transmission characteristic realizes a high-pass rather than a bandpass filter and so a global colour compensating filter was used to eliminate infrared wavelengths. Two different colour compensating filters were used with the colour photogate sensor depending on the experimental setup. A Newport BG0.40 filter was employed as part of the optical sensitivity measurement in Section 4-6 and a CM-500M filter was used in Section 4-13 as part of the colorimetric performance evaluation. Both filters have similar transmission characteristics as shown in Figure 4-7.

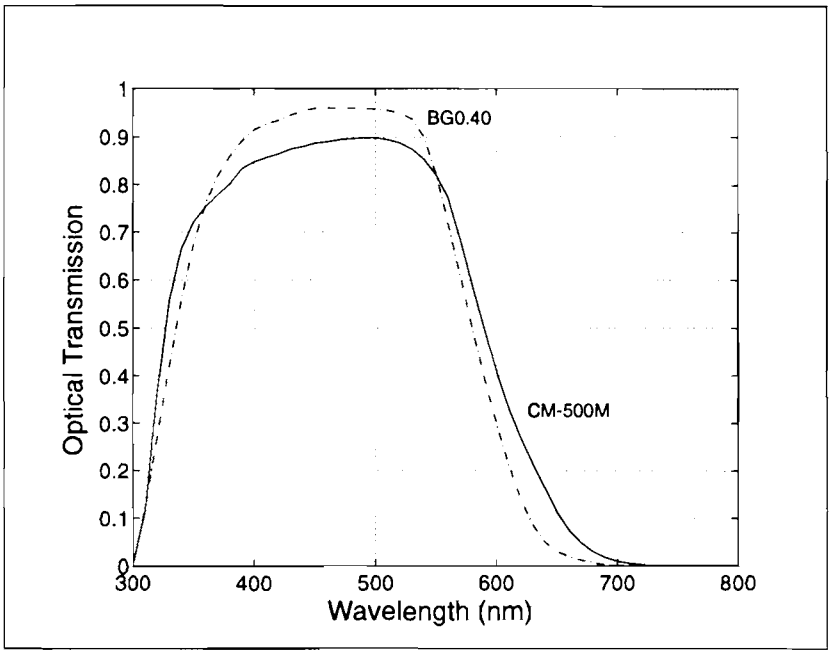


Figure 4-7. Optical transmission characteristics of the two different colour compensating filters used as part of the photogate sensor performance evaluation.

4-3. Experimentally Evaluating the Photogate Sensor

4-3.1 The Acquisition System

To enable the experimental characterization of the photogate sensor a digital acquisition system was developed to allow image data to be acquired from the sensor. It included a board containing circuits to provide two levels of correlated-double sampling, a 12-bit analog-to-digital converter, and a PC with a digital framegrabber. The acquisition system is described in more detail in Section A-1.

4-3.2 Definitions of Photogate Sensor Performance Measures

To measure the performance of the photogate sensor a number of statistical definitions were developed for the mean signal level of the sensor denoted μ, the RMS temporal noise σ_t, the

RMS pixel fixed-pattern noise σ_p, and the RMS column fixed-pattern noise σ_c. At each experimental data point 100 frames were acquired and the mean and standard deviation of each pixel value, μ_{ij} and σ_{ij},were computed. The mean signal level μ was calculated as the average of the pixel means μ_{ij}'s, and the RMS temporal noise σ_t was computed as the square root of the mean of pixel variances σ_{ij}^2's. To quantify the sensor FPN a mean image F was formed from the μ_{ij}'s. Then the RMS pixel fixed-pattern noise σ_p was measured as the square root of the average variance down the columns of F, while the RMS column fixed-pattern noise σ_c was quantified as the square root of the average variance of the pixels along the rows of F. By measuring the gains on the board, the system signal and noise components could be referred back to the sensor output. Furthermore, calibration procedures were used to remove the contribution of noise sources associated with correlated-double sampling at the board level, and the digital acquisition system. The formal definitions for μ, σ_t, σ_p, and σ_c are given in Section A-2 together with a more detailed account of the acquisition process.

4-4. Dark Current

4-4.1 The Dark Current Measurement

The sensor dark current parameters were determined while the sensor was not exposed to light. To ensure that the sensor was not subject to any illumination it was covered by a chip lid and the circuit board placed under a black cloth and the room lights extinguished. A Tektronix J11 photometer with a J1811 illuminance head measured 0-lux when placed in the same environment. Data was acquired from the sensor under these conditions for values of integration time ranging from $30ms$ to $500ms$. For each value of integration time the mean signal level of the sensor μ, the sensor RMS temporal noise σ_t, and the RMS pixel fixed-pattern noise σ_p were computed.

4-4.2 Mean Dark Signal

The mean signal μ under dark conditions is known as the mean dark signal μ_{dark}. The measured values for μ_{dark} at 25°C have been graphed in Figure 4-8 as a function of integration time.

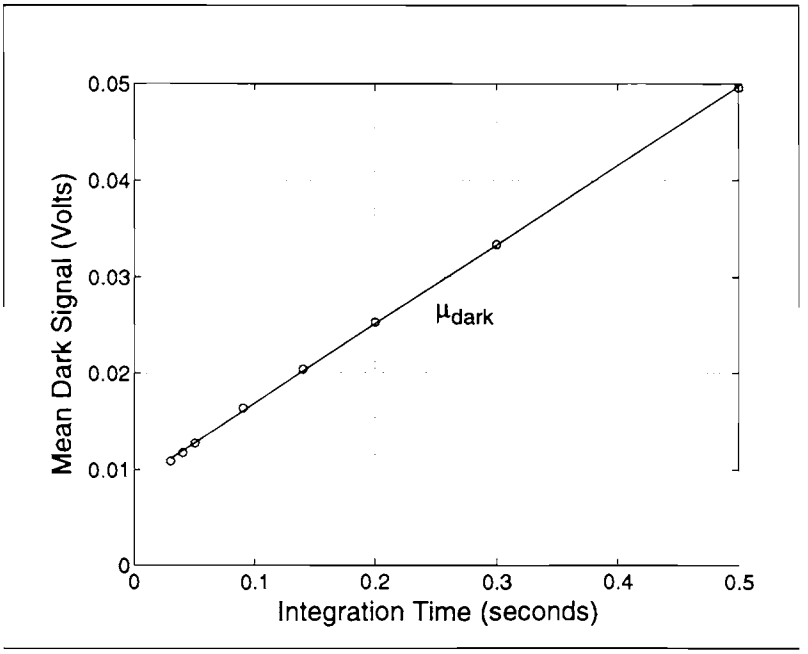


Figure 4-8. Mean dark signal μ_{dark} as a function of integration time T_{int} at 25°C. The open circles represent the measured points. A straight line has been fitted to the measured data in a least squares sense.

4-4.3 Dark Current Density

4-4.3.1 Computing the Dark Current Density

Dark current is characterized using a current density J_{dark}. To determine J_{dark} the mean dark signal μ_{dark} was measured as a function of integration time T_{int} as shown in Figure 4-8.

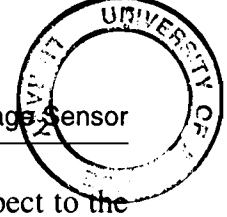
Rearrangement of (2-19) and substitution of (2-20) allows J_{dark} to be expressed as:

$$J_{dark} = \frac{q\mu_{dark}}{GA_{pixel}T_{int}} \quad Amps/cm^2 \tag{4-1}$$

where A_{pixel} is the total pixel area in square centimetres and q is the electronic charge.

The slope of the fitted line in Figure 4-8 was found to be:

$$\frac{\mu_{dark}}{T_{int}} = 82.1 mV/s \tag{4-2}$$



Equation (4-1) yields the characteristic dark current density normalized with respect to the pixel area as $J_{dark} = 183.2\ pA/cm^2$ at 25°C where values of $28\ \mu V/electron$ and $2.56 \times 10^{-6} cm^2$ have been used for the conversion gain and pixel area respectively.

Dark Current Density J_{dark}	$183.2\ pA/cm^2$ at 25°C

4-4.3.2 Dark Current Density Comparison

The sensor dark current density is compared to values reported for other CMOS and CCD image sensors in Table 4-1.

Sensor	Architecture	Process	Pixel Size (μm × μm)	J_{dark} (pA/cm^2)	*Vdd* (*Volts*)	Temp. (°C)
[Wong et al. 1998]	Photogate APS	0.25μm CMOS	7.0 × 7.0	14000	1.8	25
	Photodiode APS	0.25μm CMOS	7.0 × 7.0	4000	1.8	25
[Mendis et al. 1997b]	Photogate APS	0.35μm CMOS	8.0 × 8.0	11000	3.3	Not given
	Photodiode APS	0.35μm CMOS	8.0 × 8.0	2600	3.3	Not given
[Mansoorian et al. 1997]	Photogate APS	0.55μm CMOS	11.0 × 11.0	3530*	3.3	23
	Photodiode APS	0.55μm CMOS	11.0 × 11.0	938*	3.3	22
[Hurwitz et al. 1997]	Photodiode APS	0.8μm CMOS	10.8 × 10.8	206*	5.0	25
This sensor	**Photogate APS**	**0.8μm CMOS**	**16.0 × 16.0**	**183**	**5.0**	**25**
[Nixon et al. 1996b]	Photogate APS	1.2μm CMOS	20.4 × 20.4	105*	5.0	Not given
[Smith et al. 1997]	Frame-Interline-Transfer	1.5μm CCD	11.5 × 13.5	100	Not given	25
[Bosiers et al. 1995]	Frame-Transfer	0.8μm CCD	6.9 × 12.6	79**	10.0	28
[Schaeffer et al. 1994]	Frame-Transfer with Charge Pumping	Not given	7.5 × 7.5	31**	10.0	28
[Ozaki et al. 1994]	Interline-Transfer with Pinned Photodiodes	0.8μm CCD	7.3 × 7.6	15**	9.0	28
[Bosiers et al. 1995]	Frame-Transfer with Surface Pinning	0.8μm CCD	6.9 × 12.6	3**	10.0	28

Table 4-1. Dark current density of CMOS and CCD image sensors. The J_{dark} values marked with * have been computed using (4-1) from reported data.The J_{dark} values marked with ** have been computed from their value at 60°C assuming that dark current doubles every 8°C [Theuwissen 1995].

The dark current density J_{dark} of the photogate sensor is at the low end of values reported for other CMOS active pixel sensors, but almost a factor of 2 times larger than the nearest values reported for CCD sensors without the use of charge pumping or surface pinning, and more than an order of magnitude larger than values reported for CCD sensors using such advanced dark current management techniques. Furthermore, Table 4-1 highlights that for photogate and photodiode APS image sensors manufactured in the same CMOS process, the photogate sensor will have a substantially higher level of dark current [Mansoorian et al. 1997, Mendis et al. 1997b]. This is because the Si-SO_2 interface of the photogate pixel that forms the collection site also corresponds to the greatest concentration of defects responsible for dark current generation. Furthermore the Si-SO_2 interface is depleted with no free carriers available to quench these interface states (Section 2-5.1.4). In comparison the collection site of the photodiode

pixel is the depletion region formed between the *n*-diffusion and the substrate with only a small portion of it being in contact with the Si-SO_2 interface. As a consequence dark current in the photodiode sensor is considerable lower. The clear trend of Table 4-1 is that the dark current density of CMOS sensors increases significantly as the process feature dimensions are reduced. Consequently, to build CMOS image sensors that have dark current performance competitive with CCD sensors in deep sub-micron technology will require intervention in the fabrication process to improve cleanliness and/or realize pixels with surface pinning [Guidash et al. 1997].

4-4.4 Dark Current Non-Uniformity

Spatial variations in the dark current density J_{dark} can be characterized by the spatial RMS variation in the number of dark electrons $\sigma_{N_{dark}}$ derived from (2-19) and given by:

$$\sigma_{N_{dark}} = \frac{\sigma_{J_{dark}} A_{pixel} T_{int}}{q} \quad electrons\ RMS \tag{4-3}$$

where $\sigma_{J_{dark}}$ is the RMS spatial variation of J_{dark}.

$\sigma_{N_{dark}}$ produces an RMS voltage variation at the sensor output σ_{dark} according to:

$$\sigma_{dark} = G\,\sigma_{N_{dark}} \tag{4-4}$$

where G is the sensor conversion gain.

The sensor pixel FPN σ_p can be assumed to consist of independent components due to dark current non-uniformity σ_{dark} and residual device mismatch not suppressed by CDS $\sigma_{device\ mismatch}$ according to:

$$\sigma_p = \sqrt{\sigma_{dark}^2 + \sigma_{device\ mismatch}^2} \quad Volts\ RMS \tag{4-5}$$

As a function of integration time $\sigma_{device\ mismatch}$ will remain constant and it can be seen from (4-3) and (4-4) that σ_{dark} will linearly increase with integration time.

The sensor dark current non-uniformity $\sigma_{N_{dark}}$ was determined by measuring the pixel FPN σ_p as part of the dark current experiment. As column FPN is independent of dark current non-uniformity it was not considered during this experiment, and only one level of CDS was used to cancel reset noise and suppress pixel FPN due to device mismatch.

4-4.4.1 Dark Pixel Fixed-Pattern Noise

The pixel FPN σ_p under dark conditions is shown graphed as a function of integration time in Figure 4-9. A straight line has been fitted to the data points in a least squares sense demon-

strating that σ_p under dark conditions is a linear function of integration time. This suggests that pixel FPN is dominated by dark current non-uniformity rather than residual device mismatch. This result that will be confirmed shortly.

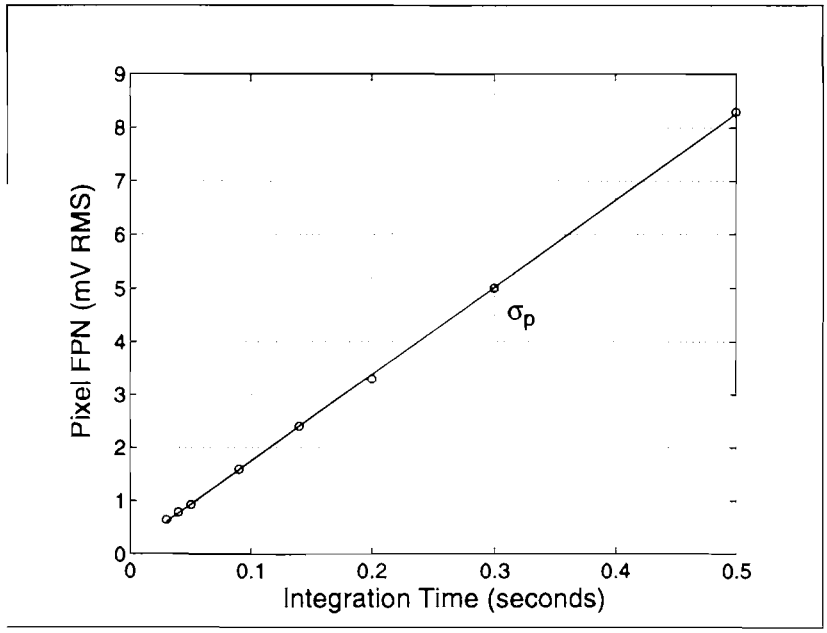


Figure 4-9. Dark pixel FPN σ_p at 25°C with one level of CDS. The open circles represent the data points and a straight line has been fitted in a least squares sense.

4-4.4.2 Demonstrating the Accuracy of the FPN Measurement

At this juncture it can be demonstrated that computing σ_p as the square root of the average variance down the columns of the image formed from the μ_{ij}'s (Section A-2) does in fact characterize pixel FPN and not errors in the measurement process. This can be shown by comparing the calculated value of σ_p at a given measurement point with the confidence intervals for the μ_{ij}'s at the same measurement point. If it is assumed that errors in the measurement process are normally distributed, the 95% confidence interval for each pixel mean μ_{ij} is given by:

$$\mu_{ij} - 1.96\frac{\sigma_{ij}}{\sqrt{M}} \leq \mu_{ij} \leq \mu_{ij} + 1.96\frac{\sigma_{ij}}{\sqrt{M}} \tag{4-6}$$

where σ_{ij} is the standard deviation of the pixel (i, j) estimated using M samples [Kreyszig 1988]. If the largest confidence interval for the μ_{ij}'s is much smaller than the computed value of σ_p, it is clear that σ_p is quantifying a genuine difference between mean pixel values μ_{ij} and not inaccuracies in their measurement. Using as an example the data point in Figure 4-9 corresponding to a 30ms integration period, the largest confidence interval for the μ_{ij}'s was found to be $\mu_{98,5} = 88.4 \pm 0.98 ADU$ estimated from $M = 100$ samples[1]. Comparing the confidence interval $\pm 0.98 ADU$ to $\sigma_p = 5.138 ADU\ RMS$ computed from the same data

set demonstrates that σ_p is in fact characterizing a genuine pixel FPN. Similar results are obtained for all FPN data points presented in this chapter.

4-4.4.3 Pixel FPN is Dominated by Dark Current Non-Uniformity and not Residual Device Mismatch

In (4-5) the pixel FPN σ_p was assumed to consist of independent components due to dark current non-uniformity σ_{dark} and residual device mismatch not suppressed by CDS $\sigma_{device\ mismatch}$. As a function of integration time $\sigma_{device\ mismatch}$ will remain constant and σ_{dark} will linearly increase. Furthermore, at zero integration time σ_{dark} will be zero. Extrapolation of the fitted line in Figure 4-9 gives $\sigma_{circuit\ mismatch} \approx 130\mu V\ RMS$. This is very small compared to σ_p for the measured values of integration time. Therefore pixel FPN is dominated by dark current non-uniformity and CDS effectively cancels all pixel FPN caused by device mismatch.

When the sensor is not illuminated $\sigma_{dark} \approx \sigma_p$ and hence values for $\sigma_{N_{dark}}$ can be found for a given integration time from Figure 4-9 by re-arrangement of (4-4). For example, at an integration period of 30ms $\sigma_{N_{dark}}$ = 23 *electrons RMS* at 25°C.

4-4.4.4 Dark Current Non-Uniformity Comparison

The spatial variation in the number of sensor dark electrons $\sigma_{N_{dark}}$ is compared to values reported for two CCD sensors in Table 4-2. The drawn pixel active area of each sensor has been computed as the Si-SiO_2 interface may be considered the area of each pixel primarily responsible for dark current generation [Toren and Bisschop 1994].

Sensor	Architecture	Process	Pixel Size (μm × μm)	Pixel Drawn Active Area (μm^2)	$\sigma_{N_{dark}}$ (*electrons RMS*)	Temp. (°C)
This sensor	**Photogate APS**	**0.8μm CMOS**	**16.0 × 16.0**	**90**	**23**	**25**
[Bosiers et al. 1995]	Frame-Transfer	0.8μm CCD	6.9 × 12.6	87*	8**	28
	Frame-Transfer with Surface Pinning	0.8μm CCD	6.9 × 12.6	87*	1**	28

Table 4-2. RMS spatial variation in the number of dark electrons of CMOS and CCD image sensors for a 30ms integration period. The entries marked with * have been calculated assuming 100% fill-factor. The values marked with ** have been computed from reported data at 60°C and 20ms integration assuming that N_{dark} doubles every 8°C and increases linearly with integration time [Theuwissen 1995].

It can be concluded from Table 4-2 that the spatial variation in dark current for the photogate sensor is approximately 3 times greater than that of a frame-transfer CCD sensor without advanced dark current management techniques, and about 20 times larger than that of a frame-transfer CCD sensor with surface pinning.

1. Note that ADU refers to A/D units. If it is desired to refer that quoted values to equivalent volts at the sensor output then (A-3) can be used where $A_{VDA1} = 3.86$ and $A_{VDA2} = 1$.

4-5. Read Noise

4-5.1 Sensor RMS Temporal Noise Under Dark Conditions

The RMS temporal noise of the sensor σ_t under dark conditions is composed of two components, dark current shot noise $\sigma_{t_{dark\ shot}}$ and read noise $\sigma_{t_{read}}$. These components are independent so they add in quadrature according to:

$$\sigma_t = \sqrt{\sigma^2_{t_{dark\ shot}} + \sigma^2_{t_{read}}} \quad Volts\ RMS \tag{4-7}$$

4-5.1.1 RMS Dark Current Shot Noise

The number of RMS electrons representing the shot noise on the dark current $n_{dark\ shot}$ is given by the square root of the number of electrons representing the dark current as expressed in (2-21). Through the conversion gain G this corresponds to an RMS voltage variation on the mean dark signal denoted $\sigma_{t_{dark\ shot}}$ that can be computed using (2-22). As (2-19) shows that N_{dark} is linearly dependent on the integration time, (2-21) and (2-22) predict that $\sigma_{t_{dark\ shot}}$ is a function of the square root of the integration time and hence should have a slope of *0.5* when plotted on a log-log graph.

4-5.1.2 RMS Read Noise

In addition to the dark current shot noise component, the sensor RMS temporal noise σ_t also contains a noise contribution from the on-chip pixel and column circuits $\sigma_{t_{read}}$. The sensor read noise is thermal noise associated with the pixel and column circuits and is not cancelled by correlated-double sampling. Thermal noise is white in nature and consequently the magnitude of the sensor read noise $\sigma_{t_{read}}$ is independent of integration time.

4-5.1.3 Expected Form of the Sensor RMS Temporal Noise Under Dark Conditions

The expected form of the sensor RMS temporal noise σ_t under dark conditions can be determined from (4-7) and is shown in Figure 4-10 for arbitrary units. σ_t changes from a constant value to a linear slope of 0.5 on a log-log plot at the value of integration time where $\sigma_{t_{dark\ shot}}$ becomes equal in value to $\sigma_{t_{read}}$.

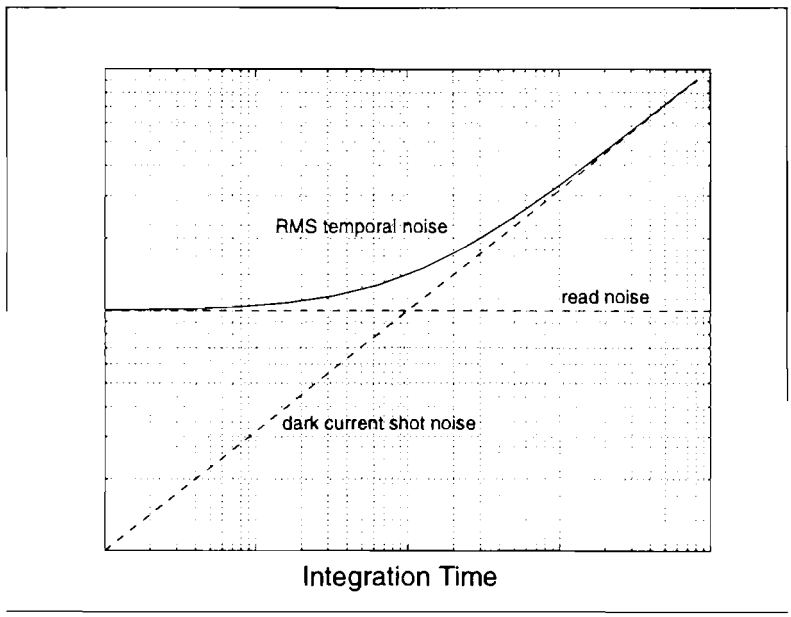


Figure 4-10. The expected form of the sensor RMS temporal noise σ_t as given by (4-7) and its constituent dark current shot noise $\sigma_{t_{dark\ shot}}$ and read noise $\sigma_{t_{read}}$ components as a function of integration time on a log-log plot with arbitrary units.

4-5.1.4 The Measured Mean Dark Signal and RMS Temporal Noise

The measured mean signal and sensor RMS temporal noise are graphed in Figure 4-11 as a function of integration time. It can be seen that the trend predicted for the sensor RMS temporal noise is not observed in Figure 4-11. This indicates that $\sigma_{t_{read}}$ for the photogate sensor is very small in comparison to $\sigma_{t_{dark\ shot}}$. It will be shown that the reason for this outcome is that the in-pixel conversion gain G_{FD} is very large which ensures that the sensor noise performance is dominated by noise components introduced at the pixel level.

4-5.2 Computing the Sensor Read Noise from Measured Data

As a preliminary step to find the sensor RMS read noise $\sigma_{t_{read}}$, the dark current shot noise component $\sigma_{t_{dark\ shot}}$ was computed. To improve the accuracy of the calculation data corresponding to an integration time of 200ms rather than 30ms was used as the precision of the procedure employed to determine σ_t is greater when the sensor noise is larger (Section A-2.5).

For 200ms integration (2-19) gives the number of dark electrons as $N_{dark} = 586\ electrons$ using values of $J_{dark} = 183.2\ pA/cm^2$ and $A_{pixel} = 2.56 \times 10^{-6} cm^2$.

Combining (2-21) and (2-22) and using $G = 28\ \mu V/electron$, the value of the dark current shot noise referred to the sensor output is $\sigma_{t_{dark\ shot}} = 678.0 \mu V\ RMS$ $(24\ electrons\ RMS)$ for 200ms integration.

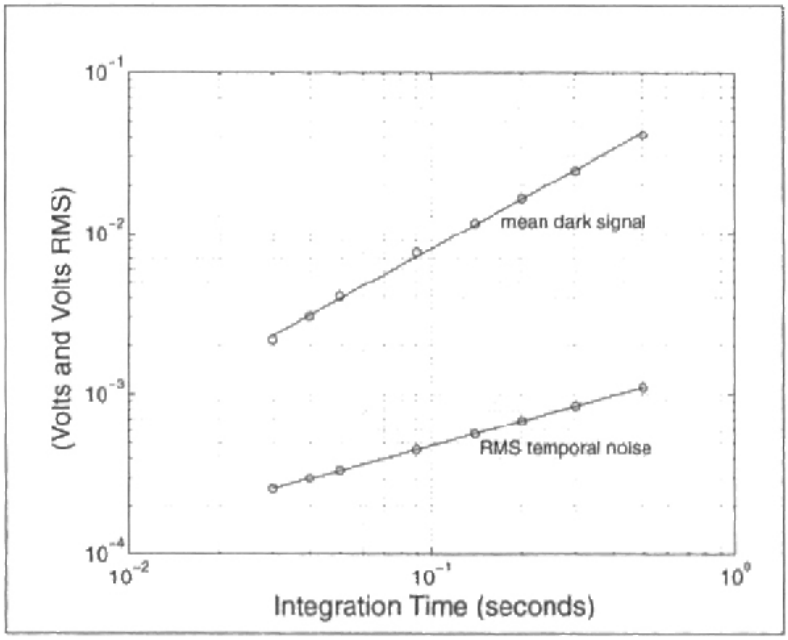


Figure 4-11. Mean dark signal μ_{dark} and sensor RMS temporal noise σ_t at 25°C. The open circles represent the data points. The *y*-intercept of Figure 4-8 has been subtracted from the mean dark signal data to enable a line of slope 1.0 to be fitted in a least squares sense. A straight line of slope 0.5 was fitted directly to the measured RMS temporal noise.

From Figure 4-11 for an integration time of $200ms$ the total sensor RMS temporal noise σ_t was measured to be $688.7\mu V\ RMS$. Re-arranging (4-7) and solving for the read noise gives $\sigma_{t_{read}} = 121.5\mu V\ RMS$. This corresponds to 4 *electrons RMS* referred to the pixel floating diffusion node.

Sensor Read Noise $\sigma_{t_{read}}$	$121.5\mu V\ RMS$

4-5.3 Computing the Sensor Read Noise from Theory

A theoretical noise analysis by Nixon et al. approximates the read noise of a photogate sensor with the same architecture by:

$$\sigma_{t_{read}} = \sqrt{2kT\left(\frac{A_{sf}^2}{C_h + C_{col}} + \frac{1}{C_h}\right)} \quad Volts\ RMS \tag{4-8}$$

where A_{sf} is the gain of the pixel source follower, C_h is the value of the sample-and-hold capacitors (C_R and C_S), and C_{col} is the capacitance of the column bus [Nixon et al. 1996b].

From the sensor layout dimensions the values for C_h and C_{col} are estimated to be $1pF$ and $1.25pF$ respectively. Circuit simulations give $A_{sf} \approx 0.7$. At $T = 300K$ (4-8) gives the theoretical value for the sensor read noise as $100.4\mu V\ RMS$.

The theoretical value for the sensor read noise is lower than the measured value for the sensor read noise. While this could be due to measurement inaccuracy there exists an alternative explanation. In Section 4-9 an additional temporal noise component of the photogate sensor called *charge transfer noise* is identified and it can be shown that (4-7) should be amended as follows:

$$\sigma_t = \sqrt{\sigma^2_{t_{dark\ shot}} + \sigma^2_{t_{read}} + \sigma^2_{t_{charge\ transfer}}} \quad Volts\ RMS \tag{4-9}$$

where $\sigma_{t_{charge\ transfer}}$ is the RMS charge transfer noise.

Consequently the sensor read noise is moderately over-estimated by (4-7) and the measured value of $121.5\mu V\ RMS$ contains a contribution from charge transfer noise. As it was not possible to determine the magnitude of the charge transfer noise $\sigma_{t_{charge\ transfer}}$ at this sensor operating point, the precise value for $\sigma_{t_{read}}$ could not be found from re-arrangement of (4-9). For simplicity and with modest loss of accuracy, all subsequent calculations involving the sensor read noise use the value of $121.5\mu V\ RMS$.

4-5.4 Sensor Read Noise Including CDS Circuits

The read noise as found in Section 4-5.2 and Section 4-5.3 is read noise associated with the photogate sensor chip itself. However, for normal operation of the sensor in a camera system, two levels of CDS are implemented by the circuit shown in Figure 4-2. The thermal noise contributed by the CDS circuits is not included in the read noise value of $121.5\mu V\ RMS$ measured in Section 4-5.2. When comparing the read noise of the photogate sensor with that of other solid-state image sensors the temporal noise associated with the CDS circuits should also be considered. If the read noise contribution of the CDS circuits is denoted $\sigma_{t_{read\ CDS}}$ then the total read noise of the camera system $\sigma_{t_{read\ camera}}$ is given by:

$$\sigma_{t_{read\ camera}} = \sqrt{\sigma^2_{t_{read}} + \sigma^2_{t_{read\ CDS}}} \quad Volts\ RMS \tag{4-10}$$

where $\sigma_{t_{read}}$ is the read noise of the photogate sensor chip found in Section 4-5.2, and $\sigma_{t_{read\ CDS}}$ is determined according to the procedure outlined in Section A-2.4.

The measured value of $\sigma_{t_{read\ CDS}}$ is $438.4\mu V\ RMS$ referred to the input of the first differential amplifier of the CDS circuit of Figure 4-2, which is equivalent to being referred to the output of the sensor chip. Equation (4-10) yields a total read noise for the camera system of

455.0μ*V RMS* referred to the sensor output. This corresponds to 16 *electrons RMS* referred to the pixel floating diffusion node.

Camera Read Noise $\sigma_{t_{read\ camera}}$	455.0μ*V RMS*

4-6. Optical Sensitivity

4-6.1 The Optical Sensitivity Experiment

The optical sensitivity of both the monochrome and colour photogate sensors were determined by measuring the mean signal level μ as a function of illumination for a fixed value of integration time. The experimental setup is shown in Figure 4-12.

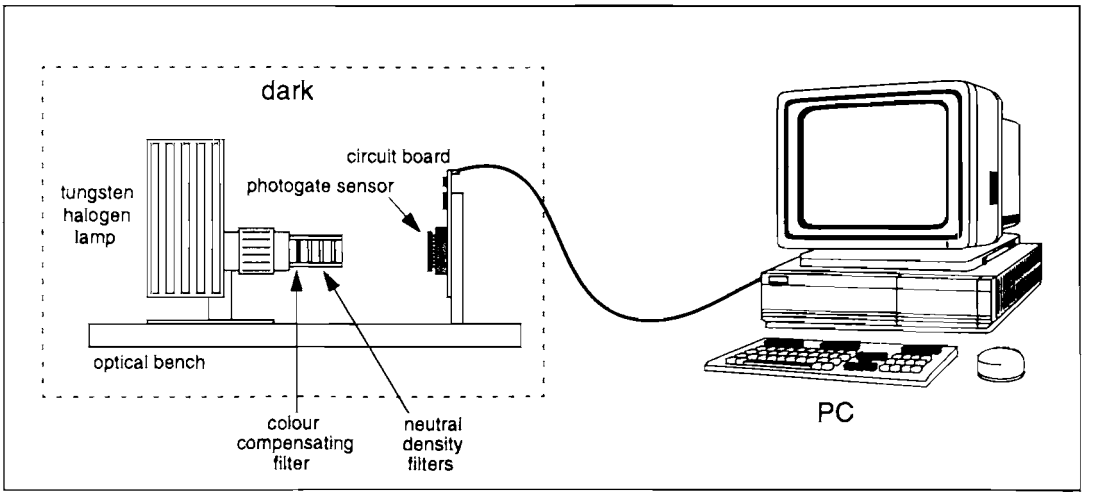


Figure 4-12. Photogate sensor experimental setup.

4-6.1.1 Illuminant Source

A Newport Model 780 tungsten halogen lamp with a correlated colour temperature of 3200K was used to provide the source of illumination. When measuring the optical sensitivity of a solid-state image sensor it is customary to use a colour compensating filter to eliminate infrared. The spectral irradiance of the lamp and transmission characteristic of the BG0.40 colour compensating filter are shown in Figure 4-13.

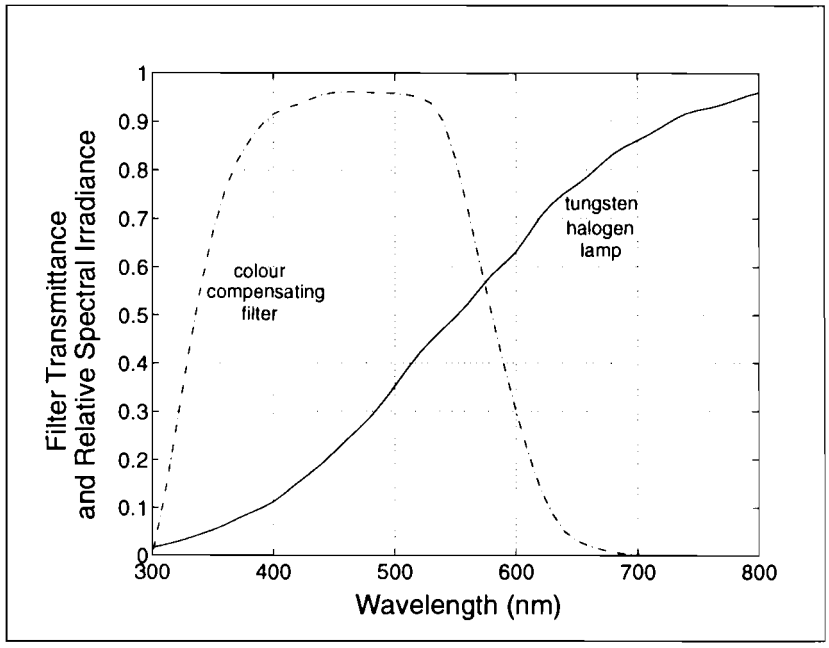


Figure 4-13. Filter transmittance of the Newport BG0.40 colour compensating filter and relative spectral irradiance of the Newport Model 780 tungsten halogen lamp.

4-6.1.2 Controlling Sensor Exposure Using Neutral Density Filters

The sensor exposure for the optical sensitivity experiment was controlled through the use of combinations of neutral density filters. The *density* of an optical filter D is defined as the logarithm to the base 10 of the filter transmittance T as given by [Hunt 1995]:

$$D = -log_{10}(T) \tag{4-11}$$

Filter density is a useful concept because when cascading filters the densities add to yield the total density value achieved by the filter combination. A *neutral density filter* has a constant value of optical density for all wavelengths across the optical portion of the spectrum.

The combinations of neutral density filters used in the optical sensitivity experiment are listed in Table 4-3. The illuminance at the sensor faceplate for each combination of neutral density filters was measured using a Tektronix J17 photometer with a J1811 illuminance head.

Neutral Density Filter Combinations	Total Density (Density)	Illuminance (lux)
OD200, ND2, ND1, ND0.3	5.3	0.086
OD200, ND2, ND1, ND0.1	5.1	0.128
OD200, ND2, ND1	5.0	0.167
OD200, ND2, ND0.5	4.5	0.455
OD200, ND2, ND0.3	4.3	0.702
OD200, ND2, ND0.1	4.1	1.096
OD200, ND2	4.0	1.332
OD200, ND1, ND0.5, ND0.3	3.8	2.032
OD200, ND1, ND0.5, ND0.1	3.6	3.242
OD200, ND1, ND0.5	3.5	3.940
OD200, ND1, ND0.3, ND0.1	3.4	5.051
OD200, ND1, ND0.3	3.3	6.241
OD200, ND1, ND0.1	3.1	9.475
OD200, ND1	3.0	11.65
OD200, ND0.5, ND0.3, ND0.1	2.9	16.70
OD200, ND0.5, ND0.3	2.8	20.22
OD200, ND0.5	2.5	38.31

Table 4-3. The measured value of illuminance for the combinations of neutral density filters used in the optical sensitivity experiment.

4-6.1.3 Verifying the Neutrality of the Filters

As the photogate sensor response and the definition of illuminance E_v given by (2-3) both have a substantial dependence on wavelength, it was important to ensure that the shape of the spectral power distribution at the sensor faceplate remained unchanged as the illuminance level was changed. To this end the neutrality of the combinations of filters was assessed by plotting the measured illuminance values of Table 4-3 as a function of the total density for each combination as shown in Figure 4-14. The close fit to a straight line with a slope near 1.0 indicates that the filters are approximately[1] neutral as for each unit of density the illumination is reduced by an order of magnitude.

1. To prove the neutrality of the filters unequivocally would require the direct measurement of the spectral power distribution of the illuminant for each filter combination. For the purposes of the optical sensitivity experiment this was not deemed practical or necessary by the author.

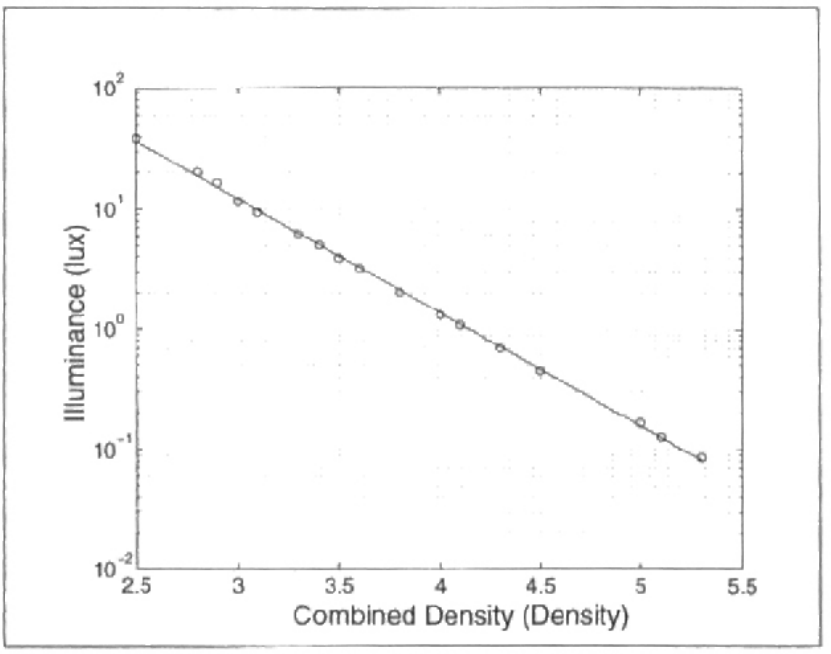


Figure 4-14. The illuminance at the sensor faceplate as a function of the total density of the neutral density filter combinations listed in Table 4-3. The open circles represent the measured data points and a straight line has been fitted in a least squares sense.

4-6.1.4 Ensuring Spatially Uniform Illumination

Before proceeding with the optical sensitivity experiment it was necessary to establish the spatial uniformity of the illumination at the sensor faceplate. The experimental setup shown in Figure 4-12 was arranged so that the sensor faceplate was centred with the optical axis of the light beam from the tungsten halogen lamp. The dimensions of the sensor corresponded to approximately 20% of the beam radius with the lamp specifications claiming only a 5% variation in intensity across this distance. To demonstrate that a sufficient level of spatial uniformity had been attained, a series of images F were acquired with the sensor rotated at different angles around the optical axis of the lamp or shifted slightly off the optical axis of the lamp. By comparing the spatial profiles along the rows and columns of F for these images it was concluded that the spatial non-uniformity of the beam was substantially less than the spatial non-uniformity of the sensor and should not significantly degrade the accuracy of any fixed-pattern noise measurements that would be made.

4-6.1.5 Experimental Procedure

For each value of illumination the mean signal level of the sensor μ, the sensor RMS temporal noise σ_t, RMS pixel fixed-pattern noise σ_p, and RMS column fixed-pattern noise σ_c were computed. To prevent extraneous illumination or "light leaks" the lamp, filters, and circuit board assembly shown in Figure 4-12 was placed under a black cloth with the room lights extinguished. To maintain measurement accuracy through the course of the experiment it was

necessary to change the circuit board gain and offset at a number of different points along each optical sensitivity curve as discussed in Section A-1.

4-6.1.6 Computing the Mean Optical Sensitivity

Under illumination the mean signal level at the sensor output μ is the sum of the optical signal level μ_{signal} and the mean dark signal μ_{dark}:

$$\mu = \mu_{signal} + \mu_{dark} \quad Volts \tag{4-12}$$

Inserting (2-13) into (4-12) yields:

$$\mu = S_o E_v T_{int} + \mu_{dark} \quad Volts \tag{4-13}$$

The mean dark signal μ_{dark} was defined by (2-19) and (2-20) and can be considered as a constant offset in (4-13) independent of illumination for a given value of integration time. If the value of μ_{dark} corresponding to a given value of integration time T_{int} is subtracted from (4-13), the mean optical sensitivity S_o can be determined from the slope of the measured mean signal μ as a function of sensor illuminance E_v according to:

$$S_o = \frac{1}{T_{int}} \cdot \frac{\mu_{signal}}{E_v} \quad Volts/lux \cdot second \tag{4-14}$$

The optical sensitivity referred to the pixel S_p can be found by dividing by the conversion gain:

$$S_p = \frac{S_o}{G} \quad electrons/lux \cdot second \tag{4-15}$$

4-6.2 Mean Optical Sensitivity of the Monochrome Sensor

The mean optical sensitivity of the monochrome photogate sensor was determined by measuring the mean signal level μ as a function of the illumination provided by the 3200K tungsten halogen lamp and BG0.40 colour compensating filter, and subtracting the appropriate value of mean dark signal μ_{dark}. The mean signal of the monochrome sensor as a function of this illuminant is shown in Figure 4-15 for integration times of 30ms and 90ms.

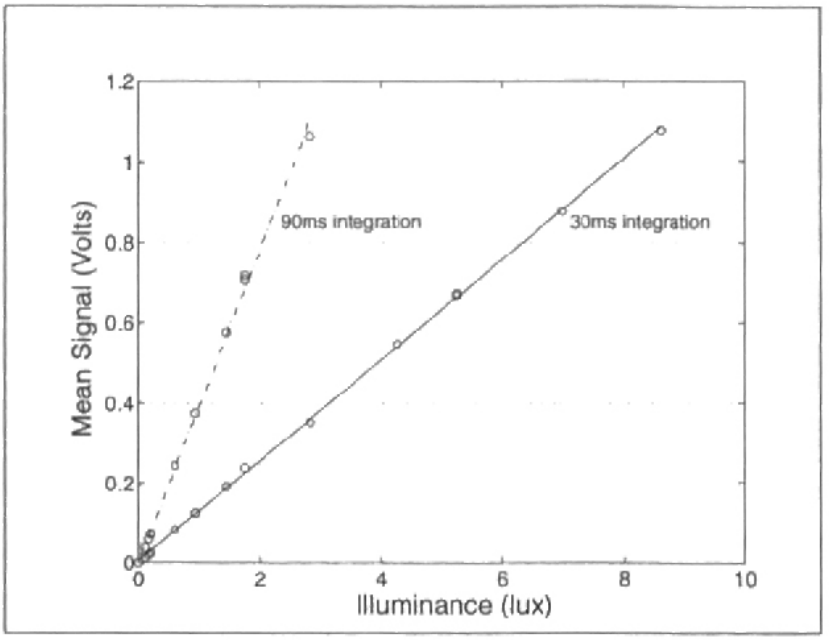


Figure 4-15. The mean signal level μ_{signal} of the monochrome sensor as a function of faceplate illuminance E_v for integration times of 30ms and 90ms. The appropriate values of μ_{dark} have been subtracted from the data points and straight lines fitted in a least squares sense. Only data points prior to sensor saturation have been plotted. The illuminant used was a 3200K tungsten halogen lamp with BG0.40 colour compensating filter.

The slope of the fitted lines in Figure 4-15 give the ratio of μ_{signal} to E_v as 125.6 mV/lux and 388.1 mV/lux for integration times of 30ms and 90ms respectively. Dividing these values by their respective integration times according to (4-14) gives values for S_o of 4.187 $V/lux.s$ and 4.312 $V/lux.s$. Averaging yields the mean optical sensitivity referred to the monochrome sensor output as $S_o = 4.25 V/lux.s$.

Using (4-15) the mean optical sensitivity of the monochrome sensor referred to the pixel S_p is equal to 152 $K\ electrons/lux.s$ using a value for the conversion gain of 28 $\mu V/electron$.

S_o	$4.25 V/lux.s$
S_p	$152\ K\ electrons/lux.s$

Table 4-4. Optical sensitivity of the monochrome photogate sensor. The illuminant used was a 3200K tungsten halogen lamp with BG0.40 colour compensating filter.

4-6.3 Optical Sensitivity Performance Comparison

The optical sensitivity of the monochrome sensor is compared to reported data for other CMOS and CCD image sensors in Table 4-5. To enable a fair comparison a figure of merit S_{FOM} based on the optical sensitivity of a sensor per unit pixel area was defined:

$$S_{FOM} = \frac{S_p}{A_{pixel}} \; electrons/lux \cdot second/\mu m^2 \tag{4-16}$$

Sensor	Architecture	Process	Pixel Size (μm × μm)	Fill Factor	S_p (Ke / lux.s)	S_{FOM} (Ke / lux.s / μm²)
[Itakura et al. 1995]	Frame-Interline Transfer (with microlenses)	0.7μm CCD	6.7 × 11.05	Not given	422 (Not given)	5.70
[Hurwitz et al. 1997]	Photodiode APS	0.8μm CMOS	10.8 × 10.8	26%	400 (Not given)	3.43
[Akimoto et al. 1991]	Interline-Transfer (with microlenses)	1.0μm CCD	6.4 × 7.5	Not given	152 (2854K)	3.17
[Morimoto et al. 1995]	Frame-Interline Transfer (with microlenses)	Not Given	6.8 × 7.5	Not given	150 (3200K, color compensating filter)	2.94
[Schaeffer et al. 1994]	Frame-Transfer	Not Given	7.5 × 7.5	Not given	150 (530nm)	2.67
This sensor	**Photogate APS**	**0.8μm CMOS**	**16.0 × 16.0**	**35%**	**152 (3200K, color compensating filter)**	**0.59**

Table 4-5. Optical performance comparison of CMOS and CCD image sensors. Monochrome values of the optical sensitivity referred to the pixel S_p have been quoted along with the corresponding illumination source. Except where indicated it was not reported whether a colour compensating filter was used or not. The optical sensitivity figure of merit S_{FOM} has been computed using (4-16).

It can be concluded from the data presented in Table 4-5 that the optical sensitivity of the photogate sensor is approximately 4.5 times lower than a frame-transfer CCD, and almost 6 times lower than a photodiode APS image sensor or interline-transfer CCD. The sensitivity of the CMOS photodiode is competitive with that of both frame-transfer and interline-transfer CCDs. However, care must be taken when comparing the optical sensitivities of sensors determined using different illuminants. The figure of merit S_{FOM} does not normalize reported optical sensitivity values with respect to differences in the spectral power distribution of the illuminant used. A more rigorous measure of optical performance independent of the illuminant is given by the sensor quantum efficiency. This is discussed in Section 4-12 together with reasons for the poor sensitivity of the photogate sensor.

4-6.4 Mean Optical Sensitivity of the Colour Sensor

The mean optical sensitivity of the colour photogate sensor was determined by measuring the mean signal level μ as a function of illumination for the red, green, and blue pixels and subtracting the mean dark signal μ_{dark}. The mean optical signal μ_{signal} as a function of illumination for the colour sensor is shown in Figure 4-16 for integration times of 30ms and 90ms.

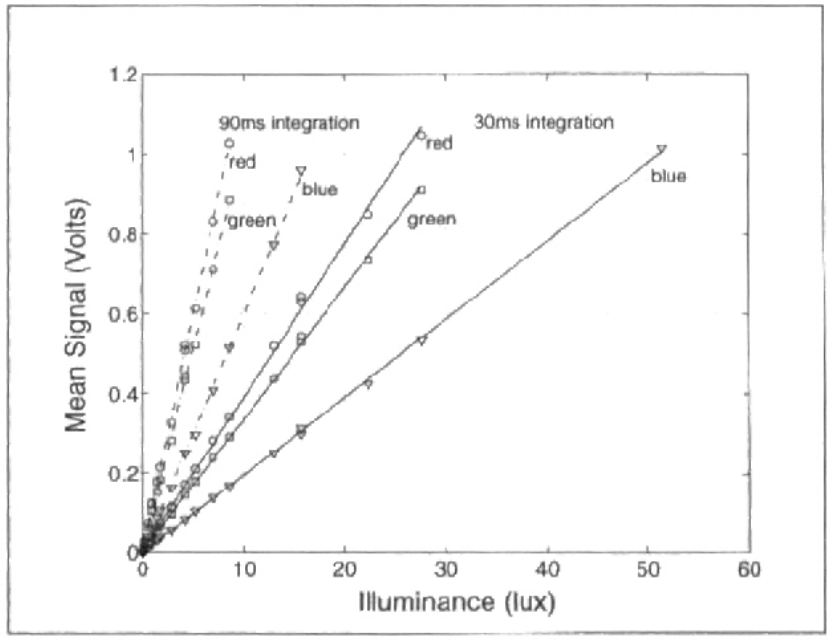


Figure 4-16. The mean signal level μ_{signal} of the colour sensor as a function of faceplate illuminance E_v for integration times of 30ms and 90ms represented by solid and dashed traces respectively. The red, green, and blue data points are represented by open circles, squares, and triangles respectively. The appropriate values of μ_{dark} have been subtracted and straight lines have been fitted in a least squares sense. Only data points prior to sensor saturation have been plotted. The illuminant used was a 3200K tungsten halogen lamp with BG0.40 colour compensating filter.

In the same manner as described for the monochrome sensor in Section 4-6.2, the mean optical sensitivity of the red, green, and blue pixels were determined and are given in Table 4-6. The optical sensitivity of the colour sensor is significantly lower than that of the monochrome sensor due to the use of the colour filters, and the shape of the photogate sensor quantum efficiency as a function of wavelength. Accurate colour rendition requires the use of optical bandpass filters realized as the combination of the colour compensating filter shown in Figure 4-13, and the colour filter array characteristics given in Figure 4-6. However, these filters reduce the number of photons incident on each pixel in the colour sensor. Furthermore, the sensor quantum efficiency is highly dependent on the wavelength of the incident light as will be shown in Section 4-12. In particular the quantum efficiency at wavelengths in the blue portion of the spectrum is much lower than it is for wavelengths in the green and red portions of

the spectrum. As a consequence of these factors the sensitivity of the blue pixels is particularly poor.

Pixel Type	S_p (K electrons / lux second)	S_o (volts per lux second)
monochrome	152	4.25
red	46.4	1.30
green	40.0	1.12
blue	23.6	0.66

Table 4-6. Optical sensitivity of the monochrome and colour photogate sensor. The illuminant was a 3200K tungsten halogen lamp and BG0.40 colour compensating filter.

4-6.5 Mean Optical Sensitivity of the Colour Sensor with Microlenses

Colour photogate sensors with microlenses were fabricated to improve the optical sensitivity. The mean optical sensitivity of a colour photogate sensor with microlenses was determined by measuring the mean signal level μ as a function of illumination for the red, green, and blue pixels and subtracting the appropriate value of mean dark signal μ_{dark}. The mean optical signal μ_{signal} as a function of illumination for colour sensors with and without microlenses is shown in Figure 4-17 for an integration time of 90ms.

In the same manner as described for the monochrome sensor in Section 4-6.2, the mean optical sensitivities of the red, green, and blue pixels of the colour photogate sensor with microlenses were found and are given in Table 4-7.

Pixel Type	S_p (K electrons / lux second)	S_o (volts per lux second)	Improvement due to Microlenses
red	61.7	1.73	33%
green	50.7	1.42	27%
blue	27.2	0.76	15%

Table 4-7. Optical sensitivity of the colour photogate sensor with microlenses. The illuminant was a 3200K tungsten halogen lamp and BG0.40 colour compensating filter.

Improvements in sensitivity due to the use of microlenses are typically of the order of 35%. For example Daemen and Peek investigated the application of microlenses to a monochrome frame-transfer CCD and reported a 36% improvement in sensitivity [Daemen and Peek 1994]. While the percentage improvement in sensitivity for the red and green pixels of the photogate sensor are of this order, the percentage improvement for the blue pixels is less than half of this. This indicates that the effectiveness of the microlenses employed with the photogate have a substantial dependence on the wavelength of the incident light. This will be quantified in

Section 4-12.5 where the quantum efficiency of the colour sensor with and without microlenses is reported.

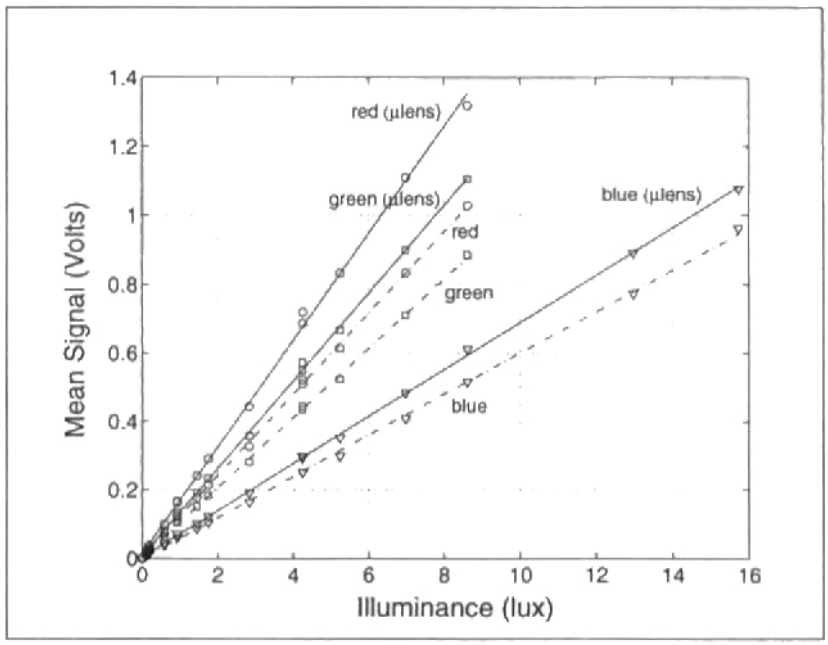


Figure 4-17. The mean signal level μ_{signal} for colour sensors with and without microlenses as a function of faceplate illuminance E_v for an integration time of 90ms are represented by solid and dashed traces respectively. The red, green, and blue data points are represented by open circles, squares, and triangles respectively. The appropriate values of μ_{dark} have been subtracted and straight lines have been fitted in a least squares sense. Only data points prior to sensor saturation have been plotted. The illuminant used was a 3200K tungsten halogen lamp with BG0.40 colour compensating filter.

4-7. Signal-to-Noise Ratio

4-7.1 Sensor RMS Temporal Noise Under Illumination

The RMS temporal noise of the illuminated sensor is composed of three components, photon shot noise $\sigma_{t_{photon\ shot}}$, dark current shot noise $\sigma_{t_{dark\ shot}}$, and sensor read noise $\sigma_{t_{read\ sensor}}$. These components are independent so they add in quadrature according to:

$$\sigma_t = \sqrt{\sigma^2_{t_{photon\ shot}} + \sigma^2_{t_{dark\ shot}} + \sigma^2_{t_{read\ sensor}}} \quad Volts\ RMS \tag{4-17}$$

Equations (2-12), (2-23), and (2-24) can be used to show that the photon shot noise $\sigma_{t_{photon\ shot}}$ increases in proportion to the square root of the illuminance E_v for a constant value of integration time. Under these same conditions the dark current shot noise $\sigma_{t_{dark\ shot}}$ and read noise $\sigma_{t_{read\ sensor}}$ are constant. For values of illuminance where the photon shot noise exceeds the

dark current shot noise and read noise, the RMS temporal noise of the sensor will have a slope of *0.5* when plotted on a log-log graph.

The RMS temporal noise σ_t of the monochrome sensor was measured as a function of the illumination provided by the 3200K tungsten halogen lamp and BG0.40 colour compensating filter. It has been plotted along with the mean signal μ_{signal} as a function of illuminance E_v in Figure 4-18 for an integration time of 30ms. The sensor saturates at an output voltage of 1.38 Volts. This corresponds to 10-lux for a 30ms integration period. Once the sensor is saturated the output is not affected by noise and consequently the measured RMS temporal noise falls dramatically as seen in Figure 4-18.

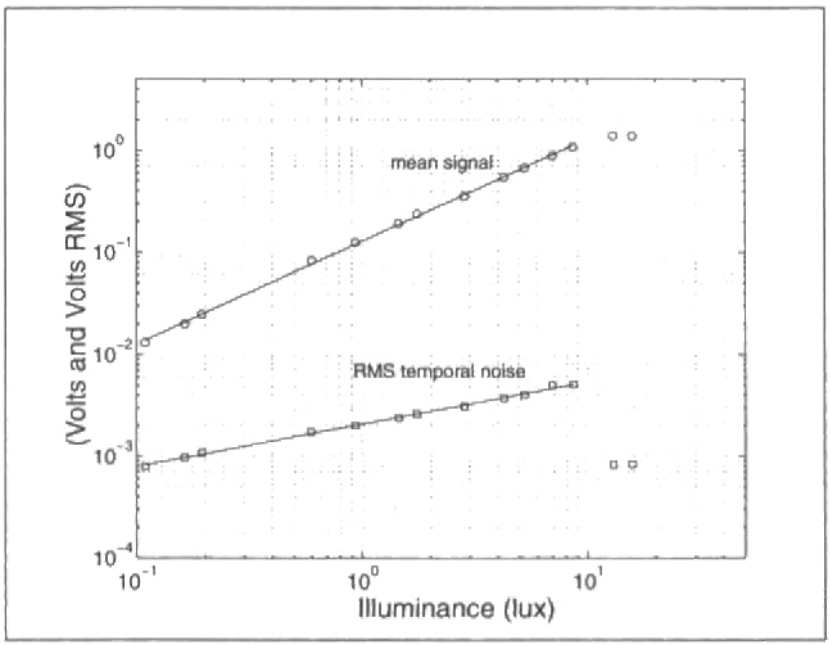


Figure 4-18. The mean signal level μ_{signal} and RMS temporal noise σ_t for the monochrome sensor as a function of faceplate illuminance E_v for an integration time of 30ms represented by open circles and squares respectively. The value of μ_{dark} for 30ms integration has been subtracted from the μ_{signal} data points. Straight lines have been fitted to data points prior to saturation in a least squares sense. The illuminant used was a 3200K tungsten halogen lamp with BG0.40 colour compensating filter.

As the slope of the sensor RMS temporal noise σ_t in Figure 4-18 is close to 0.5 it can be concluded that the photon shot noise component $\sigma_{t_{photon\ shot}}$ is much larger than the dark current shot noise $\sigma_{t_{dark\ shot}}$ and read noise $\sigma_{t_{read\ sensor}}$ for all values of illuminance measured.

4-7.2 Graphing the RMS Temporal Noise Components

For a given value of integration time the dark current shot noise component of the sensor RMS temporal noise is constant, independent of illuminance. Equations (2-19), (2-21), and

(2-22) yield the dark current shot noise as $262.2\mu V\ RMS$ ($9\ electrons\ RMS$) for an integration period of 30ms using values of $J_{dark} = 183.2\ pA/cm^2$, $A_{pixel} = 2.56 \times 10^{-6} cm^2$, and $G = 28\ \mu V/electron$.

The sensor read noise component $\sigma_{t_{read\ noise}}$ is independent of integration time and illuminance and was computed in Section 4-5.2 as $121.5\mu V\ RMS$ ($4\ electrons\ RMS$).

The photon shot noise component $\sigma_{t_{photon\ shot}}$ can be determined from the sensor RMS temporal noise σ_t by re-arrangement of (4-17). For example, the first σ_t data point in Figure 4-18 is $791.1\mu V\ RMS$ at 0.1-lux. Re-arranging (4-17) and substituting yields $\sigma_{t_{photon\ shot}}$ as $736.4\mu V\ RMS$ ($26\ electrons\ RMS$), significantly larger than the dark current shot noise and read noise components.

In this manner the photon shot noise was determined for the monochrome and colour photogate sensor with microlenses as a function of illuminance E_v for an integration period of 30ms. This data is plotted in Figure 4-19 together with the mean signal levels and the dark current shot noise and read noise components.

4-7.3 Computing the Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) of the photogate sensor is defined as the ratio of the mean signal level μ_{signal} to the total RMS temporal noise of the sensor σ_t:

$$SNR = \frac{\mu_{signal}}{\sigma_t} \tag{4-18}$$

The signal-to-noise ratio can be expressed in dB using:

$$SNR_{dB} = 20log_{10}(SNR) \tag{4-19}$$

As demonstrated by Figure 4-19 the RMS temporal noise σ_t of the monochrome and colour photogate sensors is dominated by photon shot noise $\sigma_{t_{photon\ shot}}$ when the sensor is illuminated. Under such conditions $\sigma_t \approx \sigma_{t_{photon\ shot}}$ and the signal-to-noise ratio can be written as:

$$SNR = \frac{\mu_{signal}}{\sigma_{t_{photon\ shot}}} \tag{4-20}$$

An equivalent expression for the signal-to-noise ratio can be found in terms of the number of signal electrons N_{signal} and number of RMS electrons representing the photon shot noise $n_{photon\ shot}$:

$$SNR = \frac{N_{signal}}{n_{photon\ shot}} \tag{4-21}$$

This can be simplified using (2-23) to give:

$$SNR = \sqrt{N_{signal}} \tag{4-22}$$

Substituting (2-12) enables the signal-to-noise ratio to be expressed as a function of the optical sensitivity referred to the pixel S_p, the sensor faceplate illuminance E_v, and the integration time T_{int}:

$$SNR = \sqrt{S_p E_v T_{int}} \tag{4-23}$$

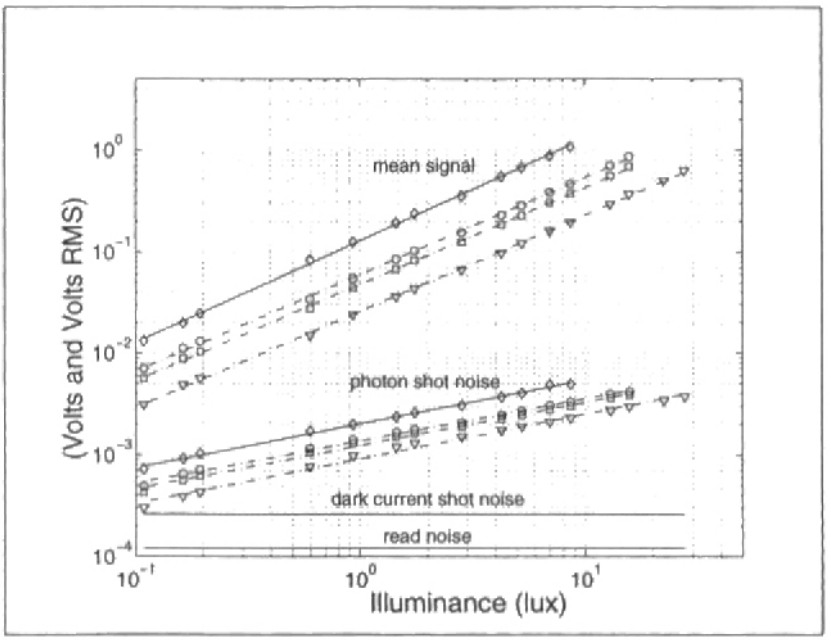


Figure 4-19. The mean signal level μ_{signal}, photon shot noise $\sigma_{t_{photon\ shot}}$, dark current shot noise $\sigma_{t_{dark\ shot}}$, and read noise $\sigma_{t_{read}}$ components for the monochrome sensor and colour sensor with microlenses as a function of faceplate illuminance for an integration time of 30ms. Data for the monochrome sensor is represented by open diamonds while the red, green, and blue pixels of the colour sensor are represented by open circles, squares, and triangles respectively. Only data points prior to saturation have been plotted. The illuminant used was a 3200K tungsten halogen lamp with BG0.40 colour compensating filter.

Table 4-8 gives the signal-to-noise ratio for the monochrome and colour sensor with microlenses for 1-lux faceplate illumination and an integration time of 30ms. The SNR of the blue pixels is significantly lower than that of the red and green pixels due to the poor optical sensi-

tivity of the blue pixels. The low SNR of the blue pixels is problematic for subsequent stages of colour processing and is discussed further in Section 4-13.7.

Pixel Type	SNR	SNR (dB)
monochrome	67.5	36.6
red (with microlenses)	43.0	32.7
green (with microlenses)	39.0	31.8
blue (with microlenses)	28.6	29.1

Table 4-8. The signal-to-noise ratio for the monochrome and colour sensor with microlenses for 1-lux faceplate illumination and an integration time of 30ms.

4-8. Dynamic Range

The dynamic range (DR) of a solid-state image sensor is defined as the ratio of the signal saturation level μ_{sat} to the RMS temporal noise floor $\sigma_{t_{floor}}$ according to [Theuwissen 1995]:

$$DR = \frac{\mu_{sat}}{\sigma_{t_{floor}}} \text{ or } DR_{dB} = 20 log_{10}\left(\frac{\mu_{sat}}{\sigma_{t_{floor}}}\right) \tag{4-24}$$

Alternatively the dynamic range may be expressed in terms of the number of electrons corresponding to sensor saturation N_{sat} and the number of RMS electrons representing the sensor RMS temporal noise floor n_{floor} as given by:

$$DR = \frac{N_{sat}}{n_{floor}} \text{ or } DR_{dB} = 20 log_{10}\left(\frac{N_{sat}}{n_{floor}}\right) \tag{4-25}$$

4-8.1 Sensor Saturation

The photogate sensor saturates at a signal level of $\mu_{sat} = 1.38V$ for a supply voltage $Vdd = 5.0V$. The number of electrons corresponding to sensor saturation N_{sat} can be found using:

$$N_{sat} = \frac{\mu_{sat}}{G} = \frac{1.38V}{28\mu V/electron} = 49 Kelectrons \tag{4-26}$$

where a value of $G = 28\mu V/electron$ was used.

A simple calculation demonstrates that at the onset of sensor saturation the potential well under the photogate is not full of electrons.

4-8.1.1 Full-Potential Well

The theoretical maximum number of electrons that could be collected under the photogate can be computed using:

$$N_{sat} = \frac{C_{ox}A_{PG}(V_{PG} - V_{tn})}{q} \quad electrons \tag{4-27}$$

where C_{ox} is the capacitance of the gate oxide per unit area, A_{PG} is the area of the photogate, V_{PG} is the voltage applied to the photogate during integration, and V_{tn} is the threshold voltage of an n-transistor. Using values of $C_{ox} = 265nF/cm^2$, $A_{PG} = 896 \times 10^{-9} cm^2$, $V_{PG} = 5.0V$, and $V_{tn} = 0.7V$ gives $N_{sat} = 6.38Melectrons$.

The saturation level of the sensor is clearly not set by filling the potential well under the photogate with photon generated electrons. Instead sensor saturation is determined by read-out circuit considerations and high in-pixel conversion gain G_{FD}.

4-8.1.2 Saturation of the Read-Out Circuits

The available signal swing at the output is determined by the pixel reset level and the transfer characteristic of the pixel source follower as modified by the combined gain of the pixel and column source followers. The cumulative transfer characteristics of the pixel and column source followers of the photogate architecture given in Figure 4-1 are shown in Figure 4-20. The sensor reset level is limited by the inability to reset the pixel floating diffusion node *FD* to the *Vdd* voltage as a result of the threshold voltage drop V_{tn} across the pixel reset device *M2*. Furthermore, the pixel source follower formed by devices *M3*, *M4*, and *M5* turns off for input voltages V_{FD} less than V_{tn}. Thus the maximum swing of the *FD* node that will be buffered by the pixel source follower is:

$$V_{FD_{sat}} \approx Vdd - 2V_{tn} \quad Volts \tag{4-28}$$

Dividing by the conversion gain at the *FD* node G_{FD} gives the corresponding number of signal electrons:

$$N_{sat} = \frac{V_{FD_{sat}}}{G_{FD}} \approx \frac{(Vdd - 2V_{tn})}{G_{FD}} \quad electrons \tag{4-29}$$

It will be shown in Section 4-10 that $G_{FD} = 70\mu V/electron$. Using $Vdd = 5.0V$ and $V_{tn} = 0.7V$ yields $N_{sat} \approx 51Kelectrons$, in close agreement with (4-26). Once this number of signal electrons has been collected by the pixel during the integration period the pixel source follower is saturated and any further electrons collected will not result in additional displacement of the output voltage of the pixel source follower P_{OUT} (see Figure 4-1). The effec-

tive signal swing of the pixel source follower is limited by high in-pixel conversion gain, incomplete reset of the *FD* node, and the source follower turning off for $V_{FD} < V_{tn}$

The maximum swing available at the output of the sensor is given by:

$$\mu_{sat} = A_{SF} V_{FD_{sat}} \approx A_{SF}(Vdd - 2V_{tn}) \quad Volts \tag{4-30}$$

where A_{SF} is the combined gain of the pixel and column source followers.

Circuit simulations give the combined gain of the pixel and column source followers under the bias conditions used for the experiments performed in the chapter as $A_{SF} \approx 0.4$. Using $Vdd = 5.0V$ and $V_{tn} = 0.7V$ in (4-30) yields $\mu_{sat} = 1.4V$ which agrees well with the measured value of $\mu_{sat} = 1.38V$.

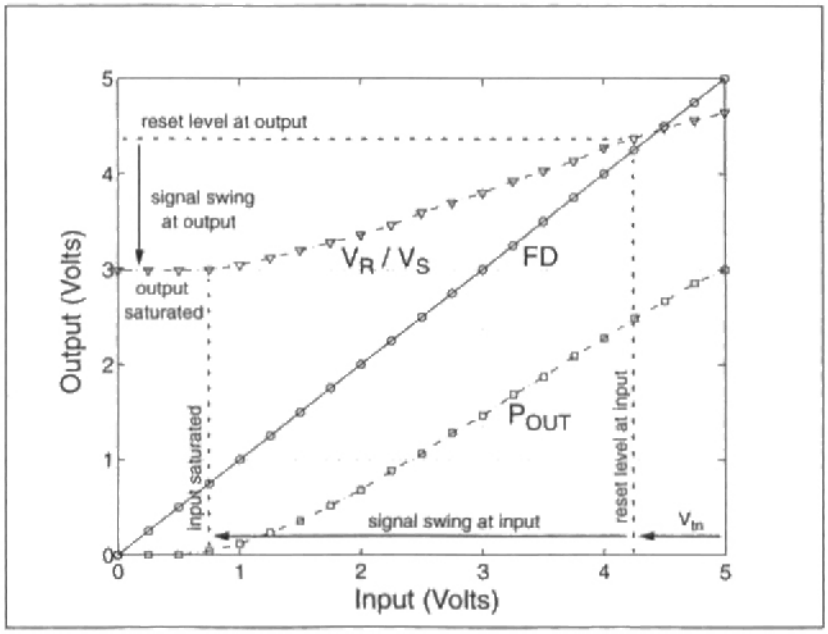


Figure 4-20. Cumulative transfer characteristics of the pixel and column source followers obtained from circuit simulation. With reference to Figure 4-1 a DC voltage ramp is applied at the FD node. P_{OUT} is the output of the pixel source follower and V_R / V_S represents the output of the column source followers.

4-8.2 Sensor RMS Temporal Noise Floor

The RMS temporal noise floor of the sensor $\sigma_{t_{floor}}$ comprises the dark current shot noise $\sigma_{t_{dark\ shot}}$ and the sensor read noise $\sigma_{t_{read\ sensor}}$ according to:

$$\sigma_{t_{floor}} = \sqrt{\sigma^2_{t_{dark\ shot}} + \sigma^2_{t_{read\ sensor}}} \quad Volts\ RMS \tag{4-31}$$

In Section 4-7.2 the dark current shot noise was found to be $\sigma_{t_{dark\ shot}} = 262.2\mu V\ RMS$ for a 30ms integration period at 25°C.

In Section 4-5.2 the sensor read noise was computed as $\sigma_{t_{read\ sensor}} = 121.5\mu V\ RMS$.

Equation (4-31) gives the RMS temporal noise floor as $\sigma_{t_{floor}} = 289.0\mu V\ RMS$ for 30ms integration time at 25°C. This is equivalent to $n_{floor} = 10\ electrons\ RMS$.

4-8.3 Dynamic Range of the Photogate Sensor

The dynamic range of the photogate sensor is therefore:

$$DR = \frac{1.38V}{289.0\mu V\ RMS} = 4775 \tag{4-32}$$

or 73.6 *dB* for a 30ms integration period.

Sensor Dynamic Range ($T_{int} = 30ms$, 25°C)	73.6 *dB*

4-8.4 Camera RMS Temporal Noise Floor

To enable fair comparisons with other solid-state image sensors it is necessary to include the temporal read noise of the CDS circuits $\sigma_{t_{read\ CDS}}$ in the definition of the RMS temporal noise floor $\sigma_{t_{floor}}$:

$$\sigma_{t_{floor}} = \sqrt{\sigma^2_{t_{dark\ shot}} + \sigma^2_{t_{read\ sensor}} + \sigma^2_{t_{read\ CDS}}}\ \ Volts\ RMS \tag{4-33}$$

In Section 4-7.2 the dark current shot noise was found to be $\sigma_{t_{dark\ shot}} = 262.2\mu V\ RMS$ for a 30ms integration period at 25°C.

In Section 4-5.2 the sensor read noise was computed as $\sigma_{t_{read\ sensor}} = 121.5\mu V\ RMS$.

In Section 4-5.4 the read noise of the CDS circuits was given as $\sigma_{t_{read\ CDS}} = 438.4\mu V\ RMS$.

Equation (4-33) gives the RMS temporal noise floor of the camera system as $\sigma_{t_{floor}} = 525.1\mu V\ RMS$ for 30ms integration time at 25°C. This is equivalent to 19 *electrons RMS*.

4-8.5 Dynamic Range of the Photogate Camera System

The dynamic range of the photogate camera system is:

$$DR = \frac{1.38V}{525.1\mu V\ RMS} = 2628 \tag{4-34}$$

or 68.4 *dB* for a 30ms integration period.

Camera Dynamic Range (T_{int} = 30ms, 25°C)	68.4 *dB*

4-8.6 Dynamic Range Comparison

To compare the dynamic range of the photogate sensor to values reported for other CMOS and CCD sensors the dynamic range of the photogate camera system including the CDS circuits was used. This is because the dynamic range values quoted for other image sensors implicitly contain the read noise contribution of similar signal conditioning circuits. The comparative data is given in Table 4-9.

Sensor	Architecture	G (μV / electron)	n_{floor} (electrons RMS)	N_{sat} (electrons)	Dynamic Range (dB)
[Itakura et al. 1995]	Frame-Interline-Transfer	20	8	75K	80
[Bosiers et al. 1995]	Frame-Transfer	12	15**	60K	72
[Bosiers et al. 1995]	Frame-Transfer	12	17**	60K	71
This sensor	**Photogate APS**	**28**	**19**	**49K**	**68**
[Schaeffer et al. 1994]	Frame-Transfer	8	32**	75K	67
[Hurwitz et al. 1997]	Photodiode APS	10	55*	100K	65
[Smith et al. 1997]	Frame-Interline-Transfer	3	40	60K	64

Table 4-9. Dynamic range comparison of CMOS and CCD image sensors based on an integration time T_{int} of 30ms and at 25°C. The noise floor of the photodiode senor denoted * includes the contribution from pixel reset noise of 52 electrons RMS. The noise floor of the sensors marked ** were computed from reported data at 60°C assuming that the dark current doubles every 8°C [Theuwissen 1995].

The dynamic range of the photogate sensor is competitive with values reported for other CMOS and CCD image sensors. However, the factors limiting the dynamic range of the CMOS and CCD sensors are quite different.

4-8.6.1 Saturation in CMOS and CCD Sensors

In Section 4-8.1 it was shown that the signal saturation level μ_{sat} of the CMOS photogate sensor is determined by the read-out circuits and high in-pixel conversion gain G_{FD}, and not saturation of the pixel collection site itself. A general expression for estimating the number of electrons corresponding to saturation N_{sat} for CMOS sensors using the source follower architecture of Figure 4-1 is given by (4-29). As feature dimensions shrink with each new generation of CMOS fabrication technology, the value of the in-pixel conversion gain G_{FD} increases as the capacitance of the pixel floating diffusion node C_{FD} decreases. Furthermore, the values of Vdd and V_{tn} are also generally reduced. This means that N_{sat} will decrease with on-going advancements in mainstream CMOS technology [Wong 1996].

While N_{sat} for CMOS sensors is determined by saturation of the read-out circuits and the value of in-pixel conversion gain, N_{sat} for CCD sensors is determined by the electron capacity of the CCD stages used for signal read-out. Hence N_{sat} is dependent on the clock voltages, the physical dimensions of the CCD stage, and doping profiles of the CCD stage [Mutoh et al. 1995]. As the trend in CCD sensor design is towards lower voltages for reduced power dissipation, and smaller pixels for higher resolution, it is difficult for CCDs to maintain N_{sat} while achieving these other performance goals [Mutoh et al. 1997, Yamaguchi et al. 1997]. Therefore in the context of maintaining high dynamic range it becomes crucial to minimize the temporal noise floor n_{floor} or $\sigma_{t_{floor}}$ for both CMOS and CCD sensors.

4-8.6.2 Temporal Noise Floor of CMOS and CCD Sensors

The temporal noise floor of both CMOS and CCD sensors is composed of dark current shot noise and read noise introduced by the sensor read-out circuits and signal conditioning circuits at the sensor output. The natural units for dark current shot noise are electrons RMS referred to the floating diffusion node. For comparative purposes it is convenient to refer the total read noise $\sigma_{t_{read\ total}}$ to RMS electrons at the floating diffusion node also using:

$$n_{read\ total} = \frac{\sigma_{t_{read\ total}}}{G} \quad electrons\ RMS \tag{4-35}$$

where G is the sensor conversion gain.

The temporal noise floor in RMS electrons n_{floor} can be considered in terms of the dark current shot noise $n_{dark\ shot}$ and total read noise contribution $n_{read\ total}$ according to:

$$n_{floor} = \sqrt{n^2_{dark\ shot} + n^2_{read\ total}} \quad electrons\ RMS \tag{4-36}$$

Reported values for the noise floor n_{floor} and constituent dark current shot noise $n_{dark\ shot}$ and read noise components $n_{read\ total}$ for the CMOS and CCD image sensors of Table 4-9 are given in Table 4-10.

As shown in Section 4-4 dark current in CMOS sensors is significantly greater than that of CCD sensors. Consequently the dark current shot noise component $n_{dark\ shot}$ is larger for CMOS photogate and photodiode sensors than values reported for the CCD sensors. Due to CDS cancelling the pixel reset noise, the total read noise $n_{read\ total}$ for the photogate sensor is much lower than that of the photodiode sensor where CDS does not cancel pixel reset noise. In Section 4-5 it was shown that the dominant component of the photogate sensor read noise is due to the CDS circuits. This is because they operate at twice the pixel clock frequency and consequently they have a larger noise bandwidth than the pixel and column source followers. For the camera system used with the present photogate sensor the CDS circuits were realized

at the board level. The read noise of the photogate sensor is not competitive with values reported for CCD sensors if the respective pixel rates are considered. However, the read noise of the photogate sensor could be reduced by integrating the CDS circuits on-chip and/or using a number of parallel output stages to reduce the noise bandwidth. This latter technique is employed by the CCD sensors of Bosiers et al. which use two parallel output stages [Bosiers et al. 1991, Bosiers et al. 1995]. The other CCD sensors reported in Table 4-10 use a single output stage which results in a greater noise bandwidth and consequently higher read noise [Schaeffer et al. 1994, Smith et al. 1997].

Sensor	Architecture	Pixel Rate (MHz)	G (μV / electron)	$n_{dark\ shot}$ (electrons RMS)	$n_{read\ total}$ (electrons RMS)	n_{floor} (electrons RMS)
[Hurwitz et al. 1997]	Photodiode APS	5	10	15	55*	55
[Smith et al. 1997]	Frame-Interline-Transfer	14	3	5	40	40
[Schaeffer et al. 1994]	Frame-Transfer	40	8	2**	32	32
This sensor	**Photogate APS**	**3**	**28**	**9**	**19**	**21**
[Bosiers et al. 1991]	Frame-Transfer	7.5	12	3**	17	17
[Bosiers et al. 1995]	Frame-Transfer	13.5	12	< 1**	15	15

Table 4-10. Noise floor comparison of CMOS and CCD image sensors based on an integration time of 30ms and at 25°C. The pixel rate is per output stage in the case of Bosiers et al. The read noise of the photodiode senor labelled * includes the pixel reset noise of 52 electrons RMS. The dark current shot noise values marked ** were computed from reported data at 60°C using (2-19) and (2-20) assuming that the dark current doubles every 8°C [Theuwissen 1995].

4-8.6.3 Conversion Gain and Dynamic Range

The role of conversion gain in sensor dynamic range performance is different for CMOS and CCD architectures. An expression for the dynamic range of a CCD sensor can be developed by combining (4-25), (4-35), and (4-36) to give:

$$DR = \frac{N_{sat}}{\sqrt{\left(\frac{\sigma_{t_{read\ total}}}{G}\right)^2 + n_{dark}^2}} \tag{4-37}$$

where it can be seen that high conversion gain G decreases the read noise component and consequently increases the dynamic range.

The corresponding expression for a CMOS sensor with the architecture of Figure 4-1 where N_{sat} is determined by read-out circuit considerations can be found by substituting (4-29) into (4-37) and simplifying using (2-18) to yield:

$$DR = \frac{(Vdd - 2V_{tn})}{\sqrt{\left(\frac{\sigma_{t_{read\ total}}}{A_{SF}}\right)^2 + (G_{FD}n_{dark})^2}} \tag{4-38}$$

where it can be seen that for given values of Vdd and V_{tn} the dynamic range is degraded by high in-pixel conversion gain G_{FD}. As a consequence the in-pixel floating diffusion capacitance C_{FD} should be designed such that the value of G_{FD} does not cause the dark current shot noise term to exceed that of the read noise term. The read noise term can be reduced by ensuring that the combined gain of the read-out circuits A_{SF} are as close to 1 as possible. To achieve a significant improvement in gain would require finding alternatives to the source follower read-out architecture commonly used with photogate and photodiode active pixel sensors. This issue has been addressed by Loinaz et al. and will be discussed in Section 5-4.2 [Loinaz et al. 1998a].

4-9. Charge Transfer Noise

In the early stages of the optical sensitivity experiment described in Section 4-6 it became evident that the photogate sensor was subject to a previously unreported temporal noise component in additional to the photon shot noise, dark current shot noise, and sensor read noise components expected from theory. This unexplained noise phenomenon manifest itself at low signal levels resulting in measured values of the sensor RMS temporal noise σ_t far in excess of values predicted using (4-17). Furthermore, the shape of σ_t graphed on a log-log plot as a function of illumination did not follow the characteristic straight line with a slope of 0.5 expected for a sensor dominated by shot noise. Investigation suggested a temporal noise component associated with charge transfer within the photogate pixel itself as responsible.

4-9.1 The Charge Transfer Noise Experiment

An experiment was used to quantify the behaviour of what was dubbed *charge transfer noise* $\sigma_{t_{charge\ transfer}}$. With the experimental arrangement of Figure 4-12, the illumination level of the sensor E_v was held constant while the integration period of the sensor T_{int} was varied. The mean signal μ_{signal} and RMS temporal noise σ_t were measured as a function of T_{int} and are shown plotted in Figure 4-21 for E_v = 0.2 *lux*. This measurement was repeated after modifying the photogate timing with the result that the mean signal μ_{signal} was not changed, but the RMS temporal noise σ_t traced a straight line with a slope close to 0.5 on a log-log plot.

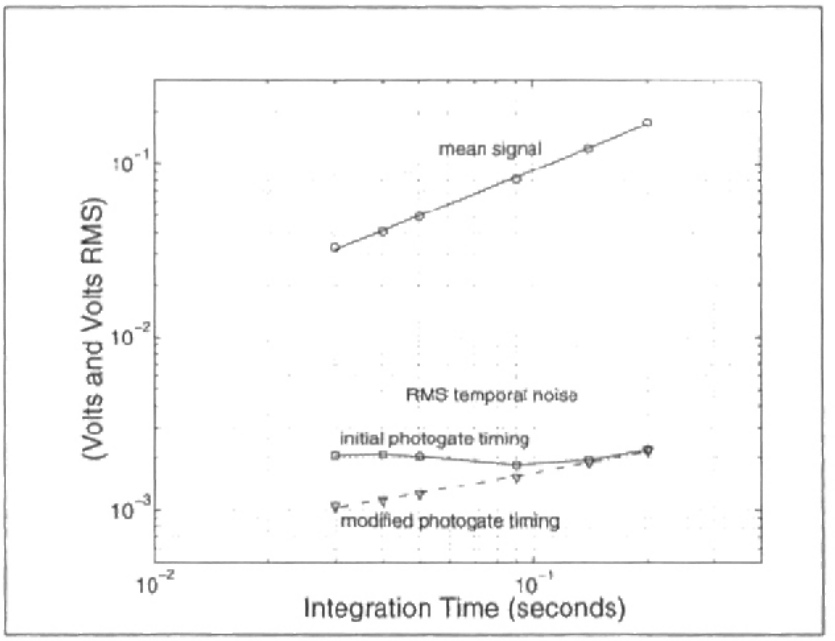


Figure 4-21. The mean signal level μ_{signal} and RMS temporal noise σ_t for the monochrome sensor as a function of integration time for a faceplate illuminance E_v of 0.2-lux. The open squares represent the σ_t data values for the initial photogate timing while the open triangles represent the σ_t data values for the modified photogate timing. The mean signal level was not changed by the modifications to the photogate timing. Straight lines have been fitted to the μ_{signal} and σ_t data values for the modified photogate timing in a least squares sense. The illuminant used was a 3200K tungsten halogen lamp with BG0.40 colour compensating filter.

The modifications necessary to the photogate timing to obtain a straight line for the RMS temporal noise σ_t with a slope close to 0.5 involved increasing the PG pulse width T_{PG}. A portion of the photogate sensor timing diagram of Figure 4-3 has been redrawn in Figure 4-22 to illustrate the PG pulse width T_{PG}.

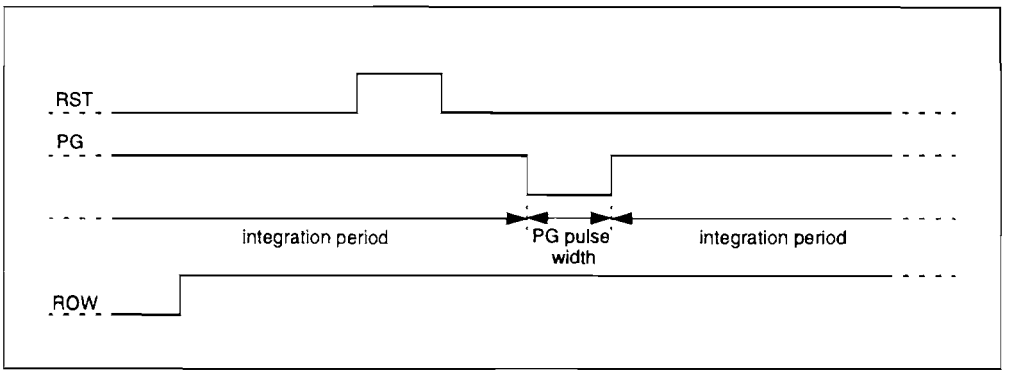


Figure 4-22. The photogate pixel timing redrawn to illustrate the integration period T_{int} during which time PG is held at Vdd, and the PG pulse of width T_{PG} during which time PG is driven to GND and electrons collected under the photogate are transferred to the pixel floating diffusion node FD.

It was found experimentally that T_{PG} has a significant influence on the magnitude of the charge transfer noise component $\sigma_{t_{charge\ transfer}}$ but does not change the mean signal level μ_{signal}. However, with the digital acquisition system used (and described in Section A-1) it was not possible to change the PG pulse width T_{PG} independently of the sensor integration time T_{int} as both of these parameters were derived from the same clock. Consequently, as the value of the PG pulse width was increased as part of the experiment, the integration time was also lengthened. To obtain the expected form for the sensor RMS temporal the value of T_{PG} was increased by a factor of four from the values used for the initial photogate timing. The values of T_{PG} for the initial and modified photogate timing data corresponding to Figure 4-21 are given in Table 4-11.

Integration Time T_{int}	**30ms**	**40ms**	**50ms**	**90ms**	**140ms**	**200ms**
T_{PG} for the initial timing	138ns	183ns	230ns	413ns	638ns	925ns
T_{PG} for the modified timing	550ns	730ns	920ns	1650ns	2550ns	3700ns

Table 4-11. PG pulse width T_{PG} as a function of the integration period T_{int} for the initial and modified photogate timing. These values were measured using a scope and correspond to the data points plotted in Figure 4-21.

4-9.2 Isolating the RMS Charge Transfer Noise Component

To isolate the charge transfer noise component $\sigma_{t_{charge\ transfer}}$ from the RMS temporal noise of the sensor σ_t it was assumed that $\sigma_{t_{charge\ transfer}}$ was independent of the other RMS temporal noise components. Equation (4-17) can be amended as:

$$\sigma_t = \sqrt{\sigma^2_{t_{photon\ shot}} + \sigma^2_{t_{dark\ shot}} + \sigma^2_{t_{read}} + \sigma^2_{t_{charge\ transfer}}} \quad Volts\ RMS \qquad (4\text{-}39)$$

where $\sigma_{t_{photon\ shot}}$ is the photon shot noise, $\sigma_{t_{dark\ shot}}$ is the dark current shot noise, and $\sigma_{t_{read}}$ is the read noise.

4-9.2.1 Changing the PG Pulse Width (and the Integration Time)

The photon shot noise $\sigma_{t_{photon\ shot}}$, dark current shot noise $\sigma_{t_{dark\ shot}}$, and read noise $\sigma_{t_{read}}$ were calculated theoretically for each of the data points in Figure 4-21 and subtracted in quadrature from the measured sensor RMS temporal noise σ_t to yield the corresponding values for the charge transfer noise $\sigma_{t_{charge\ transfer}}$.

The value for photon shot noise $\sigma_{t_{photon\ shot}}$ was calculated using:

$$\sigma_{t_{photon\ shot}} = G\sqrt{S_p E_v T_{int}} \quad Volts\ RMS \tag{4-40}$$

derived by combining (2-12), (2-23), and (2-24). Values of $G = 28\ \mu V/electron$, S_p = 152 $K\ electrons/lux.s$, and E_v = 0.2 lux were used where T_{int} takes on the values given in Table 4-11.

The dark current shot noise $\sigma_{t_{dark\ shot}}$ was calculated using:

$$\sigma_{t_{dark\ shot}} = G\sqrt{\frac{J_{dark}A_{pixel}T_{int}}{q}} \quad Volts\ RMS \tag{4-41}$$

derived by combining (2-19), (2-21), and (2-22). Values of $J_{dark} = 183.2\ pA/cm^2$ and $A_{pixel} = 2.56 \times 10^{-6}\ cm^2$ were used where again T_{int} takes on the values given in Table 4-11.

The read noise component $\sigma_{t_{read}}$ was computed in Section 4-5.2 as $121.5\mu V\ RMS$.

The individual components of the sensor RMS temporal noise plotted in Figure 4-21 are graphed in Figure 4-23 for the initial and modified photogate timing. A number of $\sigma_{t_{charge\ transfer}}$ data points were found to be imaginary and were not plotted. This occurred as the sensor RMS temporal noise approached the ideal slope of 0.5 on the log-log graph and reveals the accuracy limits of computing the $\sigma_{t_{charge\ transfer}}$ in this manner.

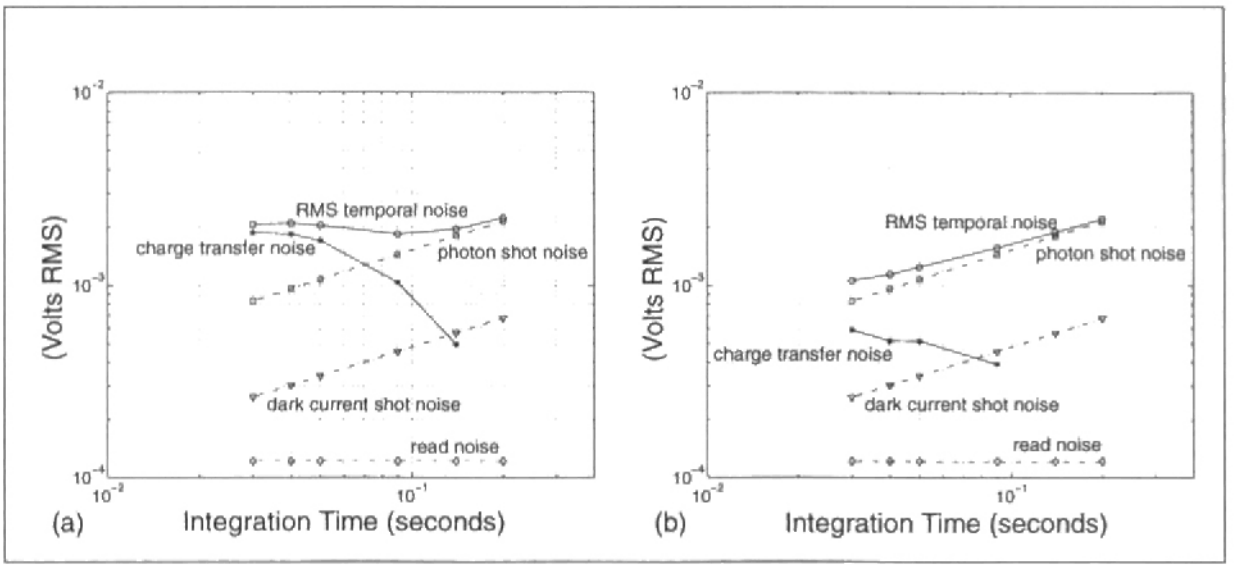


Figure 4-23. (a) RMS temporal noise components for the initial photogate timing and (b) modified photogate timing of Figure 4-21. The modified photogate timing used values of T_{PG} four times greater than the initial photogate timing for corresponding data points as listed in Table 4-11. Computed values for the charge transfer noise $\sigma_{t_{charge\ transfer}}$ that were found to be imaginary have not been plotted.

With reference to Figure 4-23 it is clear that the charge transfer noise $\sigma_{t_{charge\ transfer}}$ has a significant dependence on the PG pulse width T_{PG}. However as T_{PG} and the sensor integration time T_{int} could not be varied in an independent fashion during the experiment, the precise dependency of $\sigma_{t_{charge\ transfer}}$ on T_{PG} cannot be deduced. Furthermore, possible dependencies of $\sigma_{t_{charge\ transfer}}$ on other parameters, for example the mean signal level μ_{signal}, cannot be precluded.

4-9.2.2 Changing the TX Voltage

As part of the charge transfer experiment the voltage bias to the pixel transfer device M1 (Figure 4-1) was varied. The experiment of Section 4-9.1 was repeated for TX values of 0V and 0.1V in addition to the default value of 0.7V. Data was obtained for both the initial and modified photogate timing. The charge transfer noise $\sigma_{t_{charge\ transfer}}$ was calculated for each of these measurements in the same manner as Section 4-9.2.1 to produce Figure 4-24.

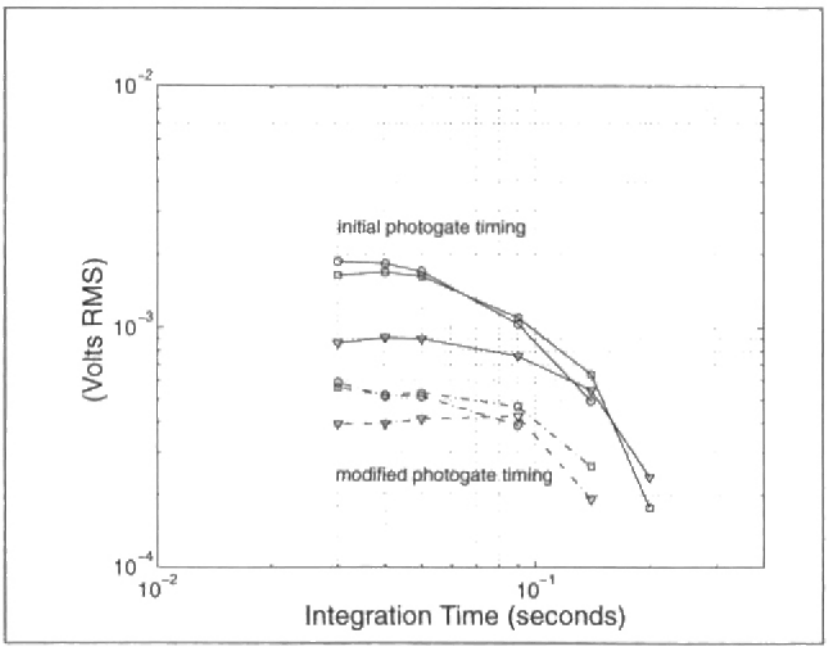


Figure 4-24. The charge transfer noise $\sigma_{t_{charge\ transfer}}$ for TX values of 0V, 0.1V, and 0.7V as represented by the open triangles, squares, and circles respectively. The solid traces correspond to the initial photogate timing and the dashed traces correspond to the modified photogate timing. Computed values for $\sigma_{t_{charge\ transfer}}$ that were found to be imaginary have not been plotted.

Figure 4-24 demonstrates the charge transfer noise $\sigma_{t_{charge\ transfer}}$ has a dependence on the TX voltage. The charge transfer noise for TX values of 0.1V and 0.7V is similar and significantly larger than that obtained at TX = 0V. This difference however becomes negligible for sufficiently large values of PG pulse width and integration time, suggesting that the TX voltage dependence is a secondary effect.

4-9.3 Proposed Explanation: Incomplete Charge Transfer

The inability to vary the PG pulse width independently of the integration time with the acquisition system meant that the photogate charge transfer noise could not be completely characterized. However, enough information was gathered to suggest an explanation for this phenomenon. It is proposed that incomplete charge transfer within the photogate pixel is responsible for charge transfer noise.

4-9.3.1 Incomplete Charge Transfer During Photogate Pixel Operation

Incomplete charge transfer within the photogate pixel will be discussed with reference to Figure 4-25 which illustrates the potential profiles during sensor operation, and Figure 4-26 which gives the photogate timing and the voltage at pixel nodes *S* and *FD*.

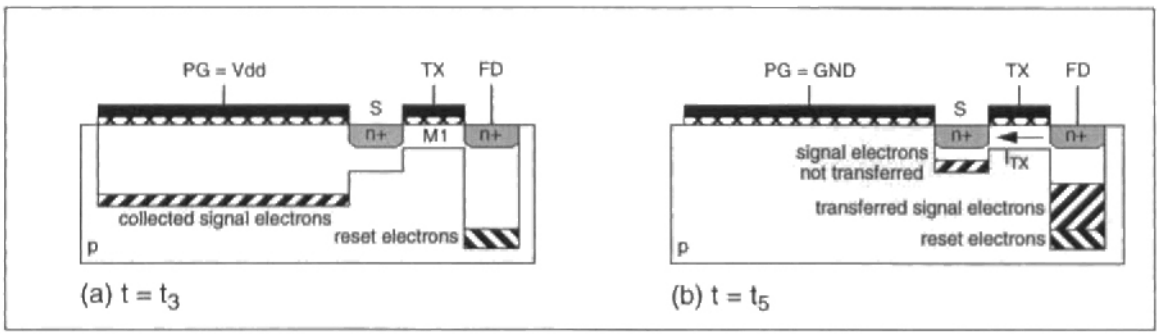


Figure 4-25. (a) Photogate pixel potential diagram at time t_3 and (b) at time t_5. Charge transfer through the transfer device M1 is via current I_{TX} (Note the convention that electrons flow in the opposite sense to the current direction).

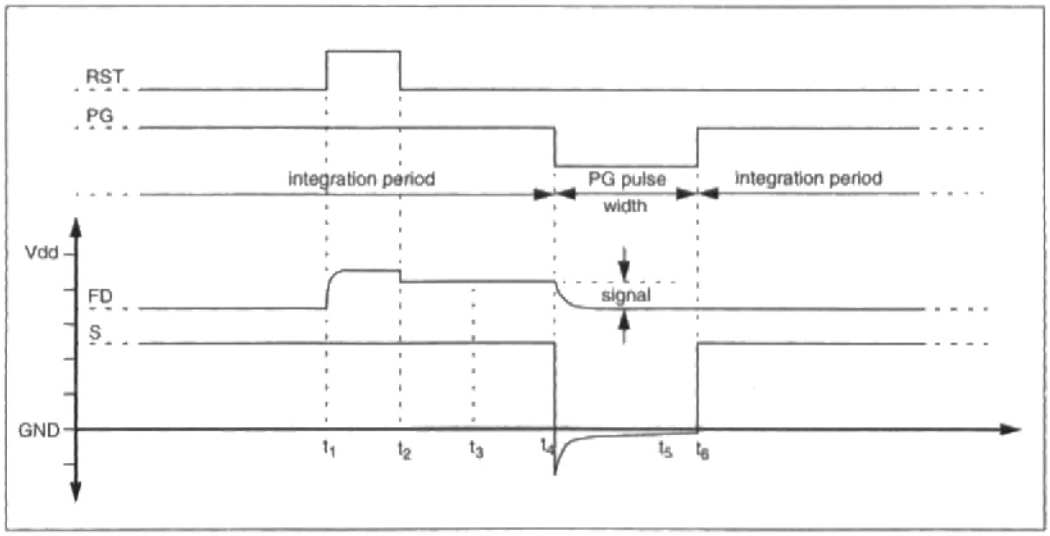


Figure 4-26. Photogate pixel timing and the voltage at nodes FD and S from circuit simulation. The FD and S traces are on the same axis and approximately to scale. The control signals RST and PG are not to scale and are only shown to give timing information.

During the integration period T_{int} the *PG* signal is held at *Vdd* and photon generated electrons are collected in the potential well formed under the pixel photogate. Prior to pixel read-out the pixel floating diffusion node *FD* is reset at time t_1 to approximately a threshold voltage drop below *Vdd* by device *M2*. At time t_2 the reset signal *RST* is de-asserted and the voltage at *FD* drops slightly due to reset clock feedthrough.

To effect pixel read-out the *PG* signal is pulsed to *GND* at time t_4. The voltage at the transfer device source *S* drops below ground due to the injection of the electrons collected under the photogate. The transfer device *M1* starts to turn on and electrons are transferred to the pixel floating diffusion node *FD* by the current I_{TX}. The transferred signal electrons displace the floating diffusion node voltage. The difference between this voltage level and the reset level of the *FD* node constitutes the signal voltage produced by the pixel. During the electron transfer the voltage at node *S* begins to rise and the transfer device starts turning off. For the final stage of electron transfer I_{TX} is a subthreshold current. It is proposed that a significant number of signal electrons N_S are retained in the depletion region of the transfer device source *S* and are not transferred. At time t_6 the *PG* signal is driven to *Vdd* and these electrons return to the potential well re-established under the pixel photogate and are added to the photon generated electrons collected during the next integration period.

4-9.3.2 Charge Transfer in the Steady State

If the number of electrons not transferred each read-out cycle i is a fraction ε of the total number of electrons collected under the pixel photogate for that cycle N_{PG_i}, then the number of electrons retained by the depletion region of *S* for that cycle N_{S_i} is given by:

$$N_{S_i} = \varepsilon N_{PG_i} \quad electrons \tag{4-42}$$

and the number of signal electrons transferred to the pixel floating diffusion node N_{signal_i} is given by:

$$N_{signal_i} = (1-\varepsilon) N_{PG_i} \quad electrons \tag{4-43}$$

The number of electrons collected under the pixel photogate each cycle N_{PG_i} consists of the electrons generated by photons $N_{photon\ generated_i}$, and those not transferred from the previous cycle $\varepsilon N_{PG_{i-1}}$ according to:

$$N_{PG_i} = N_{photon\ generated_i} + N_{S_{i-1}} = N_{photon\ generated_i} + \varepsilon N_{PG_{i-1}} \quad electrons \tag{4-44}$$

In the steady state under constant illumination and integration time the mean number of photons generated each cycle is constant and can be simply denoted $N_{photon\ generated}$. As necessarily $\varepsilon < 1$ it can be shown that under steady state conditions (4-44) converges to:

$$N_{PG} = \frac{N_{photon\ generated}}{1-\varepsilon} \quad electrons \tag{4-45}$$

and consequently (4-42) converges to:

$$N_S = \frac{\varepsilon}{1-\varepsilon} N_{photon\ generated} \quad electrons \tag{4-46}$$

and (4-43) converges to:

$$N_{signal} = N_{photon\ generated} \quad electrons \tag{4-47}$$

4-9.3.3 Charge Transfer Shot Noise in the Steady State

It is proposed that associated with incomplete charge transfer in the photogate pixel is a transfer loss noise similar to that found in CCD shift registers [Carnes and Kosonocky 1972]. For the photogate pixel shot noise is introduced to the signal electrons N_{signal} by the N_S electrons retained in the source S of the transfer device that are not transferred to the pixel floating diffusion node FD. This noise component can be represented as an RMS fluctuation $n_{charge\ transfer}$ about the mean number of signal electrons N_{signal} according to:

$$n_{charge\ transfer} = \sqrt{N_S} \quad electrons\ RMS \tag{4-48}$$

Substituting (4-46) and (4-47) gives the charge transfer noise in the steady state as:

$$n_{charge\ transfer} = \sqrt{\frac{\varepsilon}{1-\varepsilon} N_{signal}} \quad electrons\ RMS \tag{4-49}$$

The charge transfer noise expressed as an RMS voltage fluctuation $\sigma_{t_{charge\ transfer}}$ at the sensor output is given by:

$$\sigma_{t_{charge\ transfer}} = G n_{charge\ transfer} \quad Volts\ RMS \tag{4-50}$$

where G is the conversion gain.

4-9.3.4 Computing ε in the Steady State

Equation (4-49) can be re-arranged to express ε in the steady state as a function of $n_{charge\ transfer}$ and N_{signal} as given by:

$$\varepsilon = \frac{\dfrac{n^2_{charge\ transfer}}{N_{signal}}}{\left(1 + \dfrac{n^2_{charge\ transfer}}{N_{signal}}\right)} \tag{4-51}$$

Equations (4-50), (4-51), and (2-10) allow the fraction of charge not transferred ε to be determined from the computed values of $\sigma_{t_{charge\ transfer}}$ and measured values of μ_{signal}. This cal-

culation was performed for the data presented in Figure 4-23 and is shown in Figure 4-27 as a function of the width of the PG pulse T_{PG}.

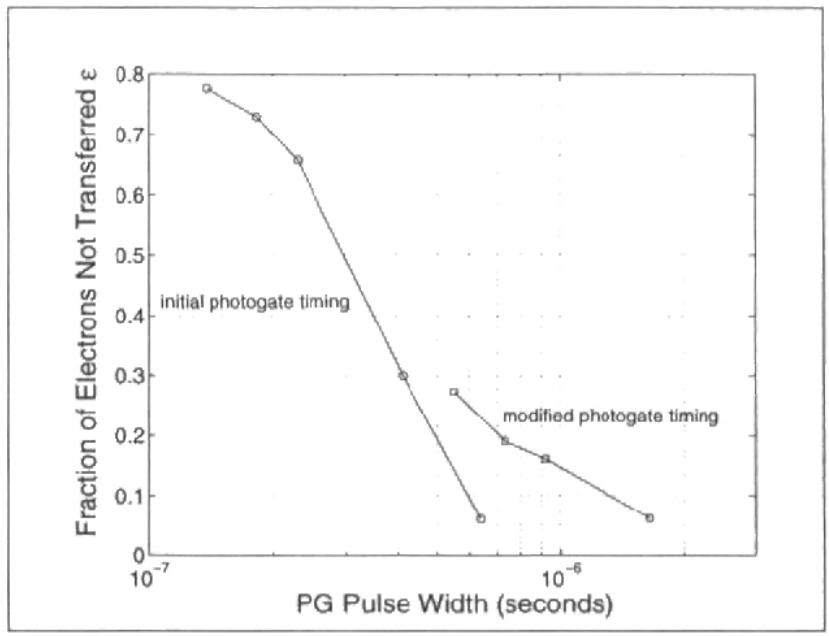


Figure 4-27. The fraction of electrons not transferred ε computed from the data of Figure 4-23 and plotted as a function of the PG pulse width T_{PG}. Table 4-11 was used to obtain the corresponding T_{PG} values from the T_{int} values employed in Figure 4-23. Only values of ε corresponding to non-imaginary calculated values of charge transfer noise have been graphed.

The curves plotted in Figure 4-27 indicate that the fraction of charge not transferred within the photogate pixel ε has a strong dependence on the PG pulse width T_{PG}. However, the fact that the two curves do not merge suggests that ε is not purely a function of the PG pulse width T_{PG}.

4-9.3.5 Charge Transfer Noise and the Transfer Device Source

It is instructive to substitute these computed values for ε into (4-46) to find the number of electrons N_S retained in the source of the transfer device as a function of T_{PG}. This data is graphed in Figure 4-28(a) along with the corresponding number of signal electrons N_{signal}. The N_{signal} curves in Figure 4-28(a) are increasing functions because the integration time T_{int} is not constant with T_{PG} as described in Table 4-11. The charge transfer noise expressed as an RMS electron fluctuation $n_{charge\ transfer}$ is plotted in Figure 4-28(b) as a function of T_{PG}.

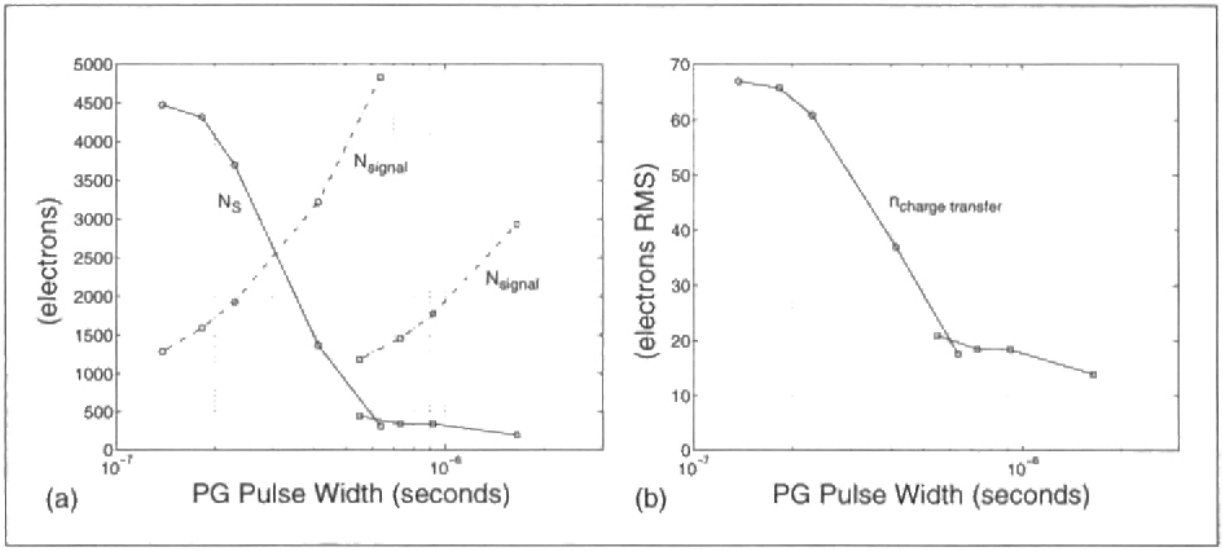


Figure 4-28. (a) The number of electrons N_S retained in the source S of the pixel transfer device and the number of signal electrons N_{signal} as a function of the PG pulse width T_{PG}. (b) The corresponding values of the charge transfer noise $n_{charge\ transfer}$ as a function of the PG pulse width T_{PG}. The open circles and squares are data points computed from the initial and modified photogate timing respectively.

The portions of the N_S and $n_{charge\ transfer}$ curves graphed in Figure 4-28 corresponding to the initial and modified photogate timing effectively merge and hence N_S and $n_{charge\ transfer}$ are monotonic decreasing functions of T_{PG}, independent of the number of signal electrons N_{signal}. This implies that in the steady state for a given value of T_{PG} a characteristic number of electrons N_S will be retained in the source of the transfer device. Furthermore, Figure 4-28(a) demonstrates that for sufficiently small values of T_{PG} it is possible that the number of electrons retained in the source can significantly exceed the number of photon generated signal electrons N_{signal} collected each integration period. This is possible as (4-44) describes how charge can be accumulated over any number of pixel integration/read-out cycles. Increasing T_{PG} reduces N_S and consequently $n_{charge\ transfer}$ by allowing more time for electrons to diffuse from the transfer device source S to the pixel floating diffusion node FD during pixel read-out. However, Figure 4-28 suggests that S will always retain a certain number of electrons during read-out regardless of the value of T_{PG} and consequently $n_{charge\ transfer}$ can never be reduced to zero.

The underlying physical cause of charge transfer noise is the retention of signal electrons by the depletion region of the source of the pixel transfer device during charge transfer. Therefore the number of electrons retained in the source N_S will also have a dependence on the physical geometry of the source structure, the doping concentrations of the source and substrate, and the

transfer device gate voltage *TX*. This last factor may support a plausible explanation of Figure 4-24.

4-9.3.6 The Mean Signal Level Under Steady-State Conditions

Equation (4-47) demonstrates that in the steady state the mean number of signal electrons transferred to the pixel floating diffusion node N_{signal} is independent of ε or N_S. This explains why the mean signal level μ_{signal} was the same for the initial and modified photogate timing described in Section 4-9.1.

4-9.3.7 The Mean Signal Level Under Dynamic Conditions

Equation (4-44) predicts that the photogate sensor will suffer from image lag. While lack of suitable equipment and time did not allow a quantitative investigation of image lag for the sensor, experience with imaging light sources in motion demonstrated that the photogate sensor is indeed subject to this phenomenon. Image lag has previously been reported for single-poly active photogate sensors with the *TX* device DC biased [Dickinson et al. 1995b].

4-9.3.8 Improving Charge Transfer in the Photogate Pixel

It has been reported that charge transfer in the single-poly photogate pixel can be improved by pulsing the *TX* gate to *Vdd* during the transfer operation rather than holding the TX gate voltage at a constant DC voltage [Dickinson et al. 1995b]. However, the row select circuitry of the photogate sensor under investigation did not support this option. Furthermore, it is the author's belief that this approach still does not guarantee complete charge transfer of electrons between the photogate and the floating diffusion node. It is likely that a number of electrons will be retained in the source of the transfer device and not transferred.

To ensure complete charge transfer the double-poly photogate pixel must be employed as this eliminates the source region of the transfer device. However, this requires the use of a CMOS fabrication process specialized for analog circuit design that supports two layers of polysilicon. If the photogate sensor is to be manufactured in a standard CMOS process only one layer of polysilicon is available. In this case the timing of the sensor read-out should be designed for a *PG* pulse width that is sufficient to minimize charge transfer noise.

To completely understand the mechanisms of charge transfer for the various photogate pixel designs would require the simulation of the three-dimensional potential profiles within each pixel structure. This procedure is routinely performed in the development of CCD architectures [Bosiers et al. 1995, Mutoh et al. 1995]. Suitable software was not available for the author to pursue this direction of investigation. It is the author's belief that the design of future generations of CMOS active pixel sensors will require such techniques.

4-9.4 Effect of Charge Transfer Noise on Parameter Calculation

As a consequence of identifying charge transfer noise as an additional temporal noise component of the photogate sensor, it is necessary to discuss how this affects a number of sensor parameters that have been already calculated. The measurements performed as part of the dark current and optical sensitivity experiments used the modified photogate timing in an attempt to minimize charge transfer noise.

In Section 4-5.2 the sensor read noise $\sigma_{t_{read}}$ was computed and shown to be larger than the value predicted from theory. It is likely that this is due to the presence of charge transfer noise $\sigma_{t_{charge\ transfer}}$ not accounted for in (4-7). As a consequence the true value for the sensor read noise is less than the measured value of $121.5\mu V\ RMS$ and perhaps closer to the theoretical value of $100.4\mu V\ RMS$.

The signal-to-noise ratio was computed in Section 4-7.3 on the assumption that when the sensor was illuminated the RMS temporal noise was dominated by photon shot noise, i.e. $\sigma_t \approx \sigma_{t_{photon\ shot}}$. This premise must be re-examined in the context of charge transfer noise. It is likely that at low light levels the charge transfer noise $\sigma_{t_{charge\ transfer}}$ may be comparable to the photon shot noise $\sigma_{t_{photon\ shot}}$ in which case equations (4-20) to (4-23) inclusive will over-estimate the sensor SNR. At sufficiently high levels of illumination the photon shot noise should dominate the charge transfer noise such that the sensor SNR can be calculated accurately using equations (4-20) to (4-23).

When computing the sensor dynamic range in Section 4-8 the value of sensor read noise used was $121.5\mu V\ RMS$. As a consequence the presence of charge transfer noise was already accounted for in that calculation.

4-10. Conversion Gain

4-10.1 Directly Measuring the Conversion Gain

The most direct technique for determining the sensor conversion gain is to inject a known number of electrons into the floating diffusion node and to measure the voltage swing at the sensor output [Yang et al. 1996]. However, for many sensors, including the CMOS photogate sensor being investigated, this option is not supported.

4-10.2 Determining the Conversion Gain by Indirect Means

The conversion gain of a solid-state image sensor can be found using an indirect technique that exploits the characteristic relationship between shot noise and the mean signal level.

4-10.2.1 Using Data from the Dark Experiment

The mean dark signal μ_{dark} and the dark current shot noise $\sigma_{t_{dark\ shot}}$ measured at the sensor output are related to the mean number of dark electrons N_{dark} and RMS electrons representing the shot noise $n_{dark\ shot}$ by the conversion gain G according to (2-20) and (2-22) respectively. Furthermore, the dark current shot noise has a square root dependence on the mean number of dark electrons as given by (2-21). This allows the conversion gain G to be written as a function of $\sigma_{t_{dark\ shot}}$ and μ_{dark} according to:

$$G = \frac{\sigma^2_{t_{dark\ shot}}}{\mu_{dark}} \quad Volts/electron \tag{4-52}$$

The mean dark signal μ_{dark} and the RMS temporal noise σ_t are given in Figure 4-11 as a function of integration time. The dark current shot noise component $\sigma_{t_{dark\ shot}}$ was determined from σ_t by re-arrangement of (4-39) given that under dark conditions the photon shot noise $\sigma_{t_{photon\ shot}}$ is zero, the read noise $\sigma_{t_{read}}$ was computed in Section 4-5.2, and assuming initially that the charge transfer noise $\sigma_{t_{charge\ transfer}}$ was negligible. Substituting the values for $\sigma_{t_{dark\ shot}}$ and μ_{dark} for each value of T_{int} into (4-52) yields data points for the conversion gain G which have been plotted as a function of mean dark signal μ_{dark} in Figure 4-29.

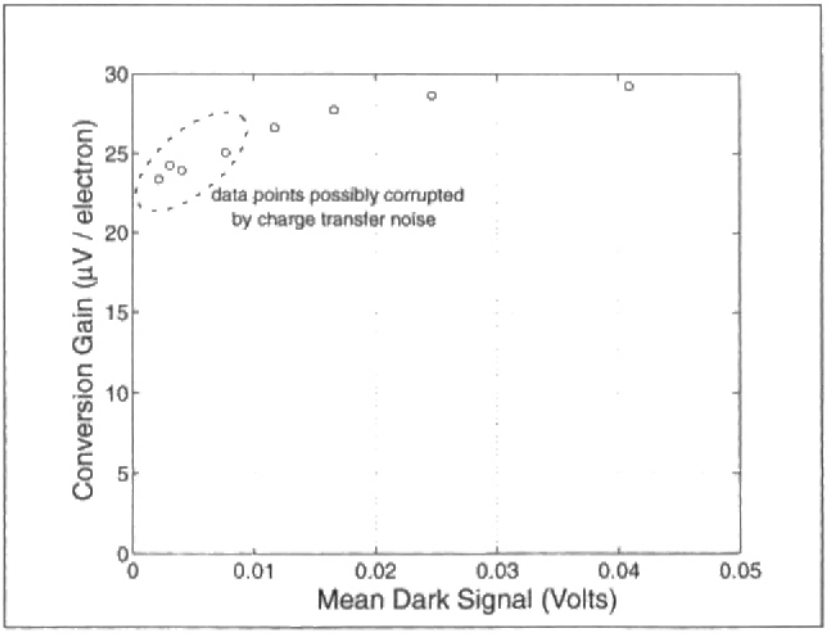


Figure 4-29. The conversion gain G as a function of mean dark signal μ_{dark} computed using (4-52) from the dark experiment data of Figure 4-11. It is possible that the data points indicated have been corrupted by charge transfer noise.

However, it is unlikely that the charge transfer noise can be neglected in the calculation of the conversion gain, despite using the modified photogate timing of Table 4-11 to obtain the

data for Figure 4-11, and consequently Figure 4-29. Inspection of Figure 4-23(b) suggests that charge transfer noise does not drop below the dark current shot noise level until a *PG* pulse width of 1650ns is used. In the modified photogate timing this corresponds to an integration time of 90ms (Table 4-11). Consequently the values of G computed from data corresponding to an integration time less than these values may be corrupted by charge transfer noise and have been labelled as such in Figure 4-29.

4-10.2.2 Using Data from the Optical Sensitivity and Charge Transfer Noise Experiments

The conversion gain G was also calculated from data from the optical sensitivity experiment of Section 4-6, and the charge transfer noise experiment of Section 4-9. When the sensor is illuminated the total mean signal at the sensor output μ can be written as:

$$\mu = \mu_{signal} + \mu_{dark} = G(N_{signal} + N_{dark}) \ \ Volts \tag{4-53}$$

using (4-12), (2-10) and (2-20).

Initially assuming the charge transfer noise component $\sigma_{t_{charge\ transfer}}$ is negligible, (4-39) can be re-arranged to compute the quadrature sum of the photon shot noise $\sigma_{t_{photon\ shot}}$ and dark current shot noise $\sigma_{t_{dark\ shot}}$ from the measured sensor RMS temporal noise σ_t and sensor read noise $\sigma_{t_{read}}$ according to:

$$\sqrt{\sigma^2_{t_{photon\ shot}} + \sigma^2_{t_{dark\ shot}}} = \sqrt{\sigma^2_t - \sigma^2_{t_{read}}} \ \ Volts\ RMS \tag{4-54}$$

where $\sigma_{t_{read}}$ was computed in Section 4-5.2, and data for σ_t was measured for the optical sensitivity and charge transfer noise experiments. Using (2-21), (2-22), (2-23), and (2-24) the left-hand side of (4-54) can be written as:

$$\sqrt{\sigma^2_{t_{photon\ shot}} + \sigma^2_{t_{dark\ shot}}} = G\sqrt{N_{signal} + N_{dark}} \ \ Volts\ RMS \tag{4-55}$$

Squaring (4-55) and dividing by (4-53) yields:

$$G = \frac{\sigma^2_{t_{photon\ shot}} + \sigma^2_{t_{dark\ shot}}}{\mu_{signal} + \mu_{dark}} \ \ Volts/electron \tag{4-56}$$

Using data obtained in Section 4-9.1 and Section 4-6.1 as part of the charge transfer noise and optical sensitivity experiments respectively, (4-56) allowed the calculation of the conversion gain G which is shown as a function of mean signal level μ in Figure 4-30(a) and (b) respectively.

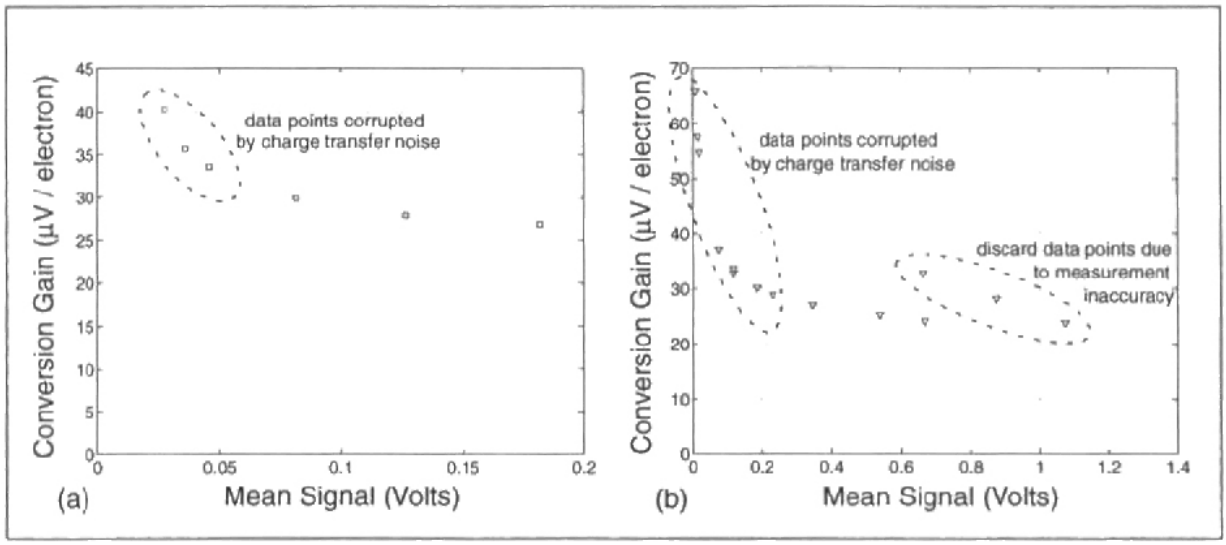


Figure 4-30. (a) The conversion gain G as a function of mean signal μ computed using (4-56) from the data of Figure 4-23(b), and (b) from the optical sensitivity data of Figure 4-18. Data points that are suspect due to corruption by charge transfer noise or known measurement inaccuracy are labelled.

To compute the conversion gain it was necessary to neglect the charge transfer noise as its precise value was not known for each of the operating points in Figure 4-23 and Figure 4-18 and so its contribution to (4-39) could not be included in the calculation. However, inspection of Figure 4-23(b) suggests that charge transfer noise does not drop below the dark current shot noise level until a PG pulse width of 1650ns is used corresponding to an integration time of 90ms for the modified photogate timing (Table 4-11). It is therefore likely that the first three data points in Figure 4-30(a) are corrupted by charge transfer noise and have been labelled as such.

The data for Figure 4-18 was obtained using an integration time of 30ms and it can therefore be expected from Figure 4-23(b) that the value of charge transfer noise will be greater than the dark current shot noise and comparable to the photon shot noise at low signal levels. The mean signal level for 30ms integration in Figure 4-23(b) is approximately 0.03V (Figure 4-21) and the photon shot noise and charge transfer noise at this operating point are about 0.9mV and 0.7mV respectively. This means that by neglecting the charge transfer noise an error of 60% is introduced into the numerator of (4-56) at this operating point. As the photon shot noise is proportional to the square root of the mean signal, increasing the mean signal by a factor of 9 increases the magnitude of the photon shot noise by 3. For the same value of integration time and PG pulse width and assuming that the charge transfer noise is independent of the mean signal level, this reduces the relative error of the numerator of (4-56) to 7%. If it is assumed that this provides sufficient accuracy for the computation of the conversion gain then data points in

Figure 4-30(b) corresponding to a mean signal less than 0.27V should be discarded and have been labelled as such.

The last three data points of Figure 4-30(b) should also be discarded due to inaccuracy in the corresponding σ_t data points in Figure 4-18. To obtain these data points in Figure 4-18 the gains and offsets of the acquisition system described in Section A-1 were changed and despite taking the appropriate calibration steps a modest discontinuity in the RMS sensor temporal noise σ_t resulted.

4-10.2.3 Combining the Conversion Gain Data

While Figure 4-29 and Figure 4-30 demonstrate that computing the conversion gain indirectly from noise measurements is imprecise, it is still necessary to estimate a characteristic value for the conversion gain to allow the calculation of many sensor performance parameters such as the dark current density (Section 4-4.3). To this end the combined conversion gain data from Figure 4-29 and Figure 4-30 that were not corrupted by charge transfer noise or measurement inaccuracy have been graphed together in Figure 4-31.

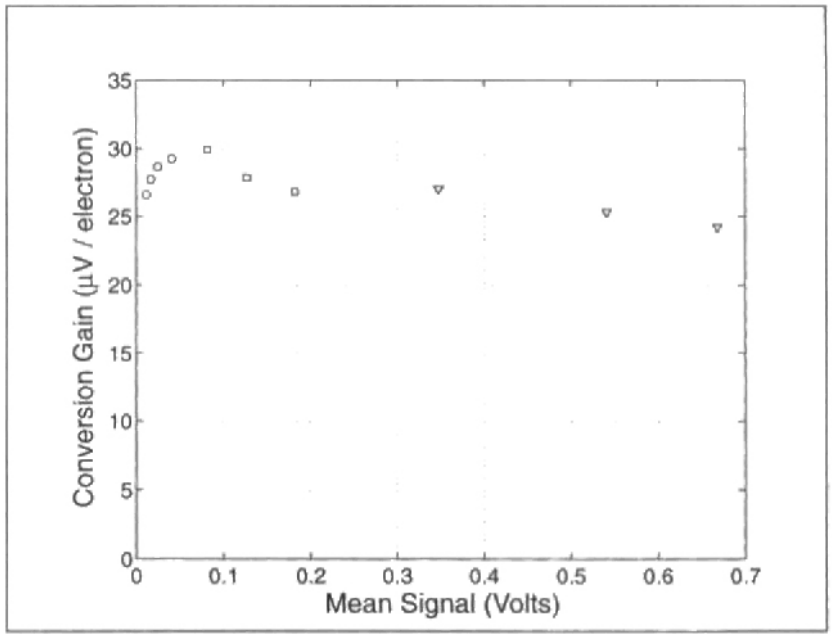


Figure 4-31. The conversion gain G as a function of mean signal μ. The open circles, squares, and triangles correspond to data from the dark experiment, charge transfer noise experiment, and optical sensitivity experiments respectively.

It can be seen from Figure 4-31 that the sensor conversion gain is not a constant but has a dependence on the mean signal level. This is not unexpected as the floating diffusion capacitance C_{FD} is formed by the parasitic capacitances of the reset device source/transfer device drain (*M1* and *M2*), and the gate of the pixel source follower device *M3*. Such capacitances are voltage dependent [Streetman 1990]. Despite the dependence on the mean signal level, it is

customary to quote a single value for the sensor conversion gain and from Figure 4-31 the author chose a nominal value of $28\mu V/electron$ referred to the sensor output.

Sensor Conversion Gain G	$28\mu V/electron$

Circuit simulations gave the combined gain of the sensor pixel and column source followers $A_{SF} \approx 0.4$ under the same bias conditions used to obtain the experimental data. Therefore (2-18) gives the conversion gain referred to the pixel floating diffusion node as $G_{FD} = 70\mu V/electron$ corresponding to a capacitance for the pixel floating diffusion node of $C_{FD} = 2.3fF$.

4-10.3 Conversion Gain Comparison

The conversion gain of the photogate sensor is compared to values reported for other CMOS and CCD sensors in Table 4-12.

Sensor	Architecture	Process	Pixel Size (μm × μm)	G (μV/electron)	Vdd (Volts)
[Wong et al. 1998]	Photogate APS	0.25μm CMOS	7.0 × 7.0	45.6	1.8
[Mendis et al. 1997b]	Photogate APS	0.35μm CMOS	8.0 × 8.0	42	3.3
This sensor	**Photogate APS**	**0.8μm CMOS**	**16.0 × 16.0**	**28**	**5.0**
[Itakura et al. 1995]	Frame-Interline-Transfer	0.7μm CCD	6.7 × 11.05	20	Not given
[Akimoto et al. 1991]	Interline-Transfer	1.0μm CCD	6.4 × 7.5	16.2*	5.0
[Bosiers et al. 1995]	Frame-Transfer	0.8μm CCD	6.9 × 12.6	12	10.0
[Nixon et al. 1996b]	Photogate APS	1.2μm CMOS	20.4 × 20.4	10.6	5.0
[Hurwitz et al. 1997]	Photodiode APS	0.8μm CMOS	10.8 × 10.8	10	5.0
[Mendis et al. 1997b]	Photodiode APS	0.35μm CMOS	8.0 × 8.0	9.5	3.3
[Schaeffer et al. 1994]	Frame-Transfer	Not given	7.5 × 7.5	8	10.0
[Smith et al. 1997]	Frame-Interline-Transfer	1.5μm CCD	11.5 × 13.5	3	Not given
[Kamasz et al. 1994]	Frame-Transfer	Not given	12.0 × 12.0	2.6	13.5

Table 4-12. Conversion gain of CMOS and CCD image sensors. All values of conversion gain are referred to the sensor output. The CCD sensor marked * employed a feedback plate amplifier in the output stage to achieve this value of conversion gain.

The conversion gain of CMOS photogate sensors and CCD sensors increases as the feature dimensions of the fabrication process are reduced. This is due to a corresponding decrease in the capacitance of the floating-diffusion node as its area is reduced. The floating diffusion capacitance of the CMOS photogate pixel (Figure 2-14) is composed of the parasitic capacitance of the shared drain/source region of the transfer and reset devices (*M1* and *M2*), together with the gate capacitance of the source follower device *M3*. All of these devices can be of minimum size as the required bandwidth of the pixel is only a function of the line rate. This allows for very high values of conversion gain for the CMOS photogate architecture as illustrated in the first two entries of Table 4-12. In comparison, the bandwidth of the output stage of a CCD sensor is a function of the pixel frequency and so the source follower device cannot be of min-

imum size. As a consequence the value of conversion gain achievable in a CCD output stage is limited unless feedback is employed [Akimoto et al. 1991]. The conversion gain of CMOS photodiode architecture is limited by the capacitance of the photodiode which also acts as the floating diffusion node. While it is possible to increase the conversion gain of the photodiode pixel by introducing a separate read-out node with a transfer gate, such sensors suffer from significant image lag [Mendis et al. 1997b].

The high conversion gain of the photogate sensor is advantageous from a SNR perspective as it minimizes the contribution of read noise and noise from the subsequent stages of signal processing such as CDS and A/D conversion to the sensor SNR (see (2-27)). Consequently, the temporal noise performance of the photogate sensor is completely determined at the pixel level by photon shot noise and dark current shot noise. However, it was shown in (4-38) that the signal saturation level of the photogate sensor is limited by read-out circuit considerations, and that high conversion gain can reduce the sensor dynamic range. As the feature dimensions of the CMOS fabrication process are reduced, together with the supply voltage Vdd, it will become increasingly important to design the floating diffusion node capacitance such that the value of conversion gain yields an acceptable trade-off between SNR and dynamic range.

4-11. Fixed-Pattern Noise

4-11.1 Measuring The Fixed-Pattern Noise

The fixed-pattern noise performance of the photogate sensor was determined by measuring the pixel fixed-pattern noise σ_p and column fixed-pattern noise σ_c as a function of illumination during the optical sensitivity experiment described in Section 4-6. The definitions used to compute σ_p and σ_c are given in Section A-2. The effectiveness of correlated-double sampling (CDS) as a technique for managing fixed-pattern noise was assessed by measuring the pixel and column fixed-pattern noise without CDS, then using one level of CDS, and finally two levels of CDS. The second level of CDS is also known as crowbar (CB) [Mendis et al. 1997a].The combined fixed-pattern noise data from the experiment is shown in Figure 4-32 plotted as a function of mean signal level μ.

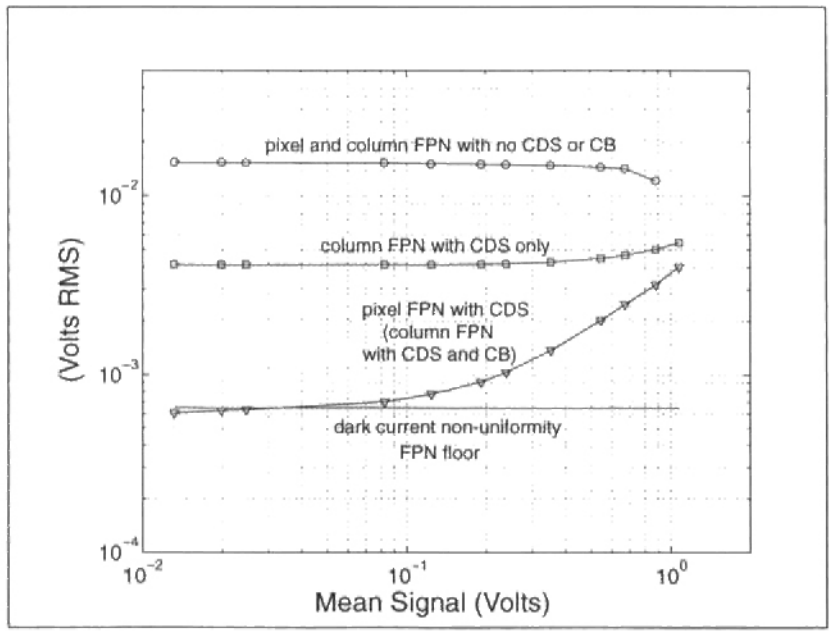


Figure 4-32. Sensor pixel FPN σ_p and column FPN σ_c as a function of mean signal level μ with and without the application of correlated-double sampling (CDS) and crowbar (CB) for an integration time of 30ms. The FPN floor imposed by dark current non-uniformity is also shown.

4-11.1.1 FPN with No CDS

Without the use of CDS the sensor FPN is dominated by pixel offset mismatch due to threshold variations in the pixel reset and source follower devices, *M2*, *M3*, and *M4* shown in Figure 4-1. Under these conditions the pixel and column FPN level is $15.4mV\ RMS$ or $6.7\%\ p\text{-}p\ sat.$ As the sensor saturates the FPN necessarily decreases.

4-11.1.2 One Level of CDS

With the application of the first level of CDS column FPN due to offset mismatch between the column source followers formed by devices *M11-M16* becomes the dominant source of FPN at $4.1mV\ RMS$ or $1.8\%\ p\text{-}p\ sat.$

At low to moderate signal levels with one level of CDS the pixel FPN is suppressed to the noise floor imposed by dark current non-uniformity at $0.67mV\ RMS$ or $0.29\%\ p\text{-}p\ sat.$ for a 30ms integration period. The FPN floor due to dark current non-uniformity is dependent on integration time and was quantified in Figure 4-9.

At moderate to high signal levels with one level of CDS the pixel FPN σ_p increases as a function of the mean signal level μ. This data is re-plotted in Figure 4-33 on a linear scale and a straight line has been fitted to the last five data points in a least squares sense.

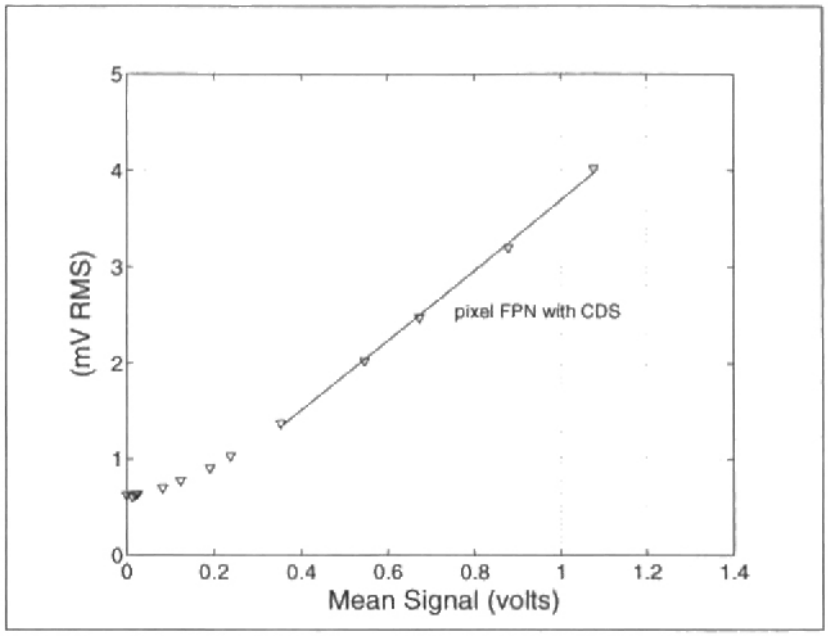


Figure 4-33. Sensor pixel fixed-pattern noise σ_p as a function of mean signal level μ with the application of one level of correlated-double sampling (CDS) for an integration time of 30ms. A straight line has been fitted to the last five data points in a least squares sense.

The good fit obtained in Figure 4-33 indicates that at high signal levels pixel FPN increases as a linear function of the mean signal due to gain mismatch between pixels. The slope of the line at $3.63mV\,RMS/V$ corresponds to an RMS pixel gain mismatch of 0.36%. This compares favourably with previously reported values for pixel gain mismatch of 1% [Nixon et al. 1996a].

Pixel gain mismatch may be due to photoresponse non-uniformity and/or conversion gain non-uniformity. Photoresponse non-uniformity is caused by differences in the optical sensitivity of pixels across the sensor array due to variations in the photogate structure. Conversion gain non-uniformity is caused by differences in the capacitance of the pixel floating diffusion node C_{FD}. Variations in the manufacturing process across the die are responsible for both of these phenomena. As the physical dimensions of the photogate are much greater than that of the structures forming the floating diffusion node it is reasonable to conclude that the dominant cause of pixel gain mismatch is conversion gain non-uniformity.

The capacitance of the floating diffusion node C_{FD} was computed in Section 4-10.2 to be $2.3fF$. Based on (2-18) an RMS variation of 0.36% in G corresponds to an RMS variation of $0.008fF$ in C_{FD} to account for the gain mismatch trend. While pixel gain mismatch is undesirable it may not be problematic for many imaging applications. This is because the human

visual system is not as sensitive to spatial or temporal noise in images at high signal levels as it is at low signal levels.

At high signal levels and with one level of CDS the column FPN also begins to increase. This is due to the magnitude of the pixel FPN becoming comparable to the column FPN. Under such conditions the column FPN as defined in Section A-2 begins to be influenced by the pixel FPN.

4-11.1.3 Two Levels of Correlated Double Sampling

With the application of the second level of CDS, or crowbar (CB), the column FPN is suppressed to the same level as the pixel FPN with one level of CDS, 0.29% *p-p sat.* at low to moderate signal levels. The use of CB does not alter the pixel FPN level.

4-11.2 Fixed-Pattern Noise Performance Comparison

The pixel fixed-pattern noise performance of the photogate sensor at low to moderate signal levels is compared to values reported for other CMOS and CCD image sensors in Table 4-13. All the CMOS APS image sensors listed used two levels of correlated-double sampling to deliver the fixed-pattern noise performance reported. From the results obtained with the photogate sensor whose FPN performance is the subject of this investigation it can be surmised that the FPN performance of any CMOS photogate or photodiode APS image sensor using two levels of CDS will be determined by the level of dark current non-uniformity. As a direct relationship between dark current density and dark current non-uniformity is assumed, the reported values for the dark current density J_{dark} of the image sensors are also given in Table 4-13.

The fixed-pattern noise performance of the photogate sensor being discussed in this chapter is at the low end of values reported for CMOS active pixel sensors, but almost 4 times larger than a frame-transfer CCD without the use of advanced dark current management techniques such as surface pinning. Due to the connection between dark current and fixed-pattern noise the trend in Table 4-13 is similar to that found in Table 4-1; as the feature dimensions of the fabrication process is reduced the fixed-pattern noise performance of CMOS sensors is substantially degraded.

Sensor	Architecture	Process	Pixel Size (μm × μm)	σ_p (% p-p sat.)	J_{dark} (pA/cm²)	Temp. (°C)
[Mendis et al. 1997b]	Photogate APS	0.35μm CMOS	8.0 × 8.0	6.0	11000	Not given.
	Photodiode APS	0.35μm CMOS	8.0 × 8.0	1.5	2600	Not given.
[Mansoorian et al. 1997]	Photogate APS	0.55μm CMOS	11.0 × 11.0	0.6	3530	23
	Photodiode APS	0.55μm CMOS	11.0 × 11.0	0.6	938	22
This sensor	**Photogate APS**	**0.8μm CMOS**	**16.0 × 16.0**	**0.29**	**183**	**25**
[Nixon et al. 1996b]	Photogate APS	1.2μm CMOS	20.4 × 20.4	0.2	105	Not given.
[Nixon et al. 1995]	Photodiode APS	1.2μm CMOS	19.2 × 19.2	< 0.15	< 200	25
[Bosiers et al. 1995]	Frame-Transfer	0.8μm CCD	6.9 × 12.6	0.08*	79*	28
	Frame-Transfer with Surface Pinning	0.8μm CCD	6.9 × 12.6	0.01*	3*	25

Table 4-13. Pixel fixed-pattern noise performance and dark current density of CMOS and CCD image sensors. All the CMOS image sensors used two levels of correlated-double sampling. The values marked with * have been computed from their value at 60°C assuming that dark current doubles every 8°C [Theuwissen 1995].

4-11.3 Managing Fixed-Pattern Noise in CMOS APS Image Sensors

It has been demonstrated that correlated-double sampling is an extremely effective technique for cancelling offset differences between pixel and column circuits in a CMOS APS image sensor. This was shown by the ability of one level of CDS to cancel pixel offset mismatch and the second level of CDS to cancel column offset mismatch. However, CDS cannot suppress gain differences between circuits such as those due to photoresponse non-uniformity and conversion gain non-uniformity in the photogate pixel. Such sources of fixed-pattern noise can only be managed by achieving greater device uniformity at the fabrication process level.

The FPN noise floor of a CMOS APS sensor using two levels of CDS is set by dark current non-uniformity as CDS does not cancel this non-ideality. Alternative FPN management techniques have been developed for use in digital still cameras that employ a frame memory to measure and subtract the contribution due to dark current non-uniformity for each pixel [Hurwitz et al. 1997]. For applications where such an approach is unsuitable dark current non-uniformity can only be addressed at the fabrication process level by reducing the dark current density and/or introducing pixel structures that support surface pinning [Guidash et al. 1997]. To compete with the fixed-pattern noise performance of high-end CCD sensors intervention at the fabrication process level will be required.

4-12. Quantum Efficiency

4-12.1 The Quantum Efficiency Measurement

The quantum efficiency of the monochrome and colour photogate sensors were determined using the experimental setup shown in Figure 4-34. A Jobin Yvon H-10 monochromator provided a monochromatic source with variable wavelength in the range 400nm to 1100nm. An optical fibre and beam splitter was used to equally share the source between the photogate sensor and a Newport 840-C optical power meter with a 818-UV photodetector.

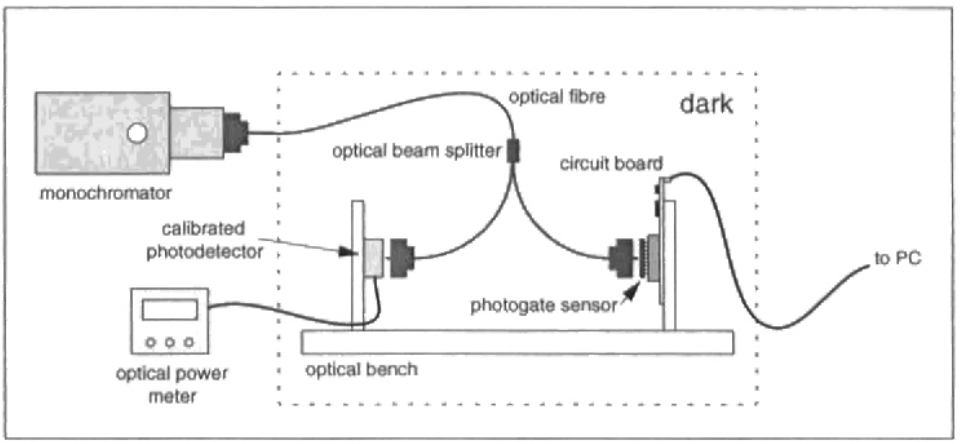


Figure 4-34. Experimental setup for the quantum efficiency measurement.

The quantum efficiency of the photogate sensor was determined using the following procedure. At each wavelength λ the beam produced by the monochromator was completely enclosed by the imaging array. The exposure of the sensor was set to ensure that none of the pixels were saturated. 100 frames were acquired and the mean signal level μ_{ij} for each pixel was computed using (A-6) and a black reference level subtracted.

The total number of signal electrons collected was computed using:

$$N_{signal\ total} = \frac{1}{G} \sum_{i}^{rows} \sum_{j}^{columns} \mu_{ij} \quad electrons \tag{4-57}$$

The optical power meter was used to measure the optical power $P_e(\lambda)$ output by the monochromator at each wavelength λ. The total number of photons $N_{photons\ total}(\lambda)$ incident on the photogate sensor during the integration period T_{int} was calculated using:

$$N_{photons\ total}(\lambda) = \frac{\lambda P_e(\lambda)\, T_{int}}{h\, c} \quad photons \tag{4-58}$$

which was derived from (2-2).

The sensor quantum efficiency at λ is then given by:

$$\eta(\lambda) = \frac{N_{signal\ total}(\lambda)}{N_{photons\ total}(\lambda)} \tag{4-59}$$

All the quantum efficiency data presented in Section 4-12 was obtained by Iliana Fujimori of the Massachusetts Institute of Technology.

4-12.2 Quantum Efficiency of the Monochrome Sensor

The measured quantum efficiency $\eta(\lambda)$ of the monochrome sensor is shown in Figure 4-35.

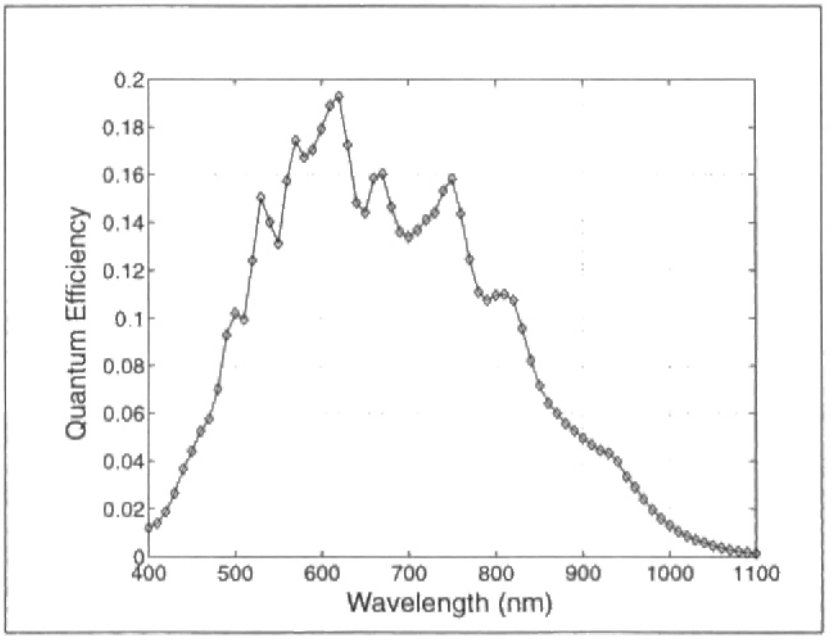


Figure 4-35. Quantum efficiency $\eta(\lambda)$ of the monochrome sensor. Note that the data has not been divided by the drawn pixel fill factor.

The sensor quantum efficiency at wavelengths 400-500nm is particularly low due to optical absorption in the polysilicon of the photogate. The oscillations in the quantum efficiency plot at wavelengths 500-800nm are caused by optical interference in the polysilicon, SiO_2, and protective layers of the photogate structure [Theuwissen 1995]. The quantum efficiency at wavelengths greater that 800nm begins to fall due to these photons penetrating the silicon substrate at depths in excess of the minority carrier diffusion length before being absorbed. Most electrons generated by such photons recombine rather than diffusing to the collection site under the photogate.

4-12.3 Quantum Efficiency Comparison

The monochrome sensor quantum efficiency is compared with values reported for other CMOS and CCD image sensors in Table 4-14.

Sensor	Architecture	Process	η_{400nm}	η_{600nm}	η_{800nm}	η_{peak}
[Levine et al. 1994]	Frame-Transfer with Backside Illumination	2.0μm CCD	57%	80%	58%	80% (600nm)
[Stevens et al. 1991]	Interline-Transfer	1.2μm CCD	73%	55%	15% (est.)	79% (440nm)
[Nixon et al. 1995]	Photodiode APS	1.2μm CMOS	6%	53%	46%	59% (610nm)
[Bosiers et al. 1995]	Frame-Transfer	0.8μm CCD	14%	20%	4%	32% (500nm)
[Nixon et al. 1996a]	Photogate APS	1.2μm CMOS	2.5%	20%	17%	24% (700nm)
This sensor	**Photogate APS**	**0.8μm CMOS**	**1.2%**	**18%**	**11%**	**19% (620nm)**

Table 4-14. Quantum efficiency of CMOS and CCD image sensors.

The quantum efficiency of the photogate sensor is comparable to data published for other CMOS photogate APS image sensors but the peak quantum efficiency is approximately 70% lower than that of a frame-transfer CCD [Nixon et al. 1996a, Bosiers et al. 1995]. The photogate sensor has a factor of 3 or 4 times lower quantum efficiency than the CMOS photodiode sensor, the interline-transfer CCD, and the frame-transfer CCD with backside illumination. The low quantum efficiency of the photogate sensor explains the poor optical sensitivity results obtained in Section 4-6. The low quantum efficiency of the photogate sensor, particularly at short wavelengths, is due to absorption in the polysilicon photogate [Wong et al. 1998]. By way of comparison, the polysilicon of a standard sub-micron CMOS process is of the order of 3 to 10 times thicker than that used in a frame-transfer CCD [Bosiers et al. 1995]. To substantially improve the quantum efficiency of the photogate sensor would require decreasing the thickness of the polysilicon photogate as a modification to the standard CMOS fabrication process. The quantum efficiency of the photogate sensor could also be enhanced by increasing the pixel fill-factor. As the feature dimensions of CMOS fabrication technology continue to decrease this will enable higher pixel fill-factors to be achieved. However, the manufacture of image sensors in sub-micron CMOS fabrication technology introduces a new issue concerning quantum efficiency to be addressed. It is normal practice in state-of-the-art CMOS processes to implant the polysilicon gate and source/drain regions of devices with metallic ions to form a compound known as *silicide*. While the use of silicide improves various electrical properties of transistors, it is almost opaque to light in the visible spectrum [Wong et al. 1998]. It is therefore critical in the manufacture of CMOS sensors in sub-micron technology to block the formation of silicide on the photogates and the photodiodes. As no measured data has been published comparing the sensitivity and quantum efficiency of sensors with and without silicide, the

exact performance penalty of the use of silicide is unknown. The photogate sensor evaluated in this chapter was manufactured in a 0.8µm CMOS process for which the formation of silicide was blocked.

4-12.4 Quantum Efficiency of the Colour Sensor

The measured quantum efficiency of the colour sensor is shown in Figure 4-36 with the quantum efficiency of the monochrome sensor superimposed. A CM-500M colour compensating filter was used with the colour sensor for this measurement.

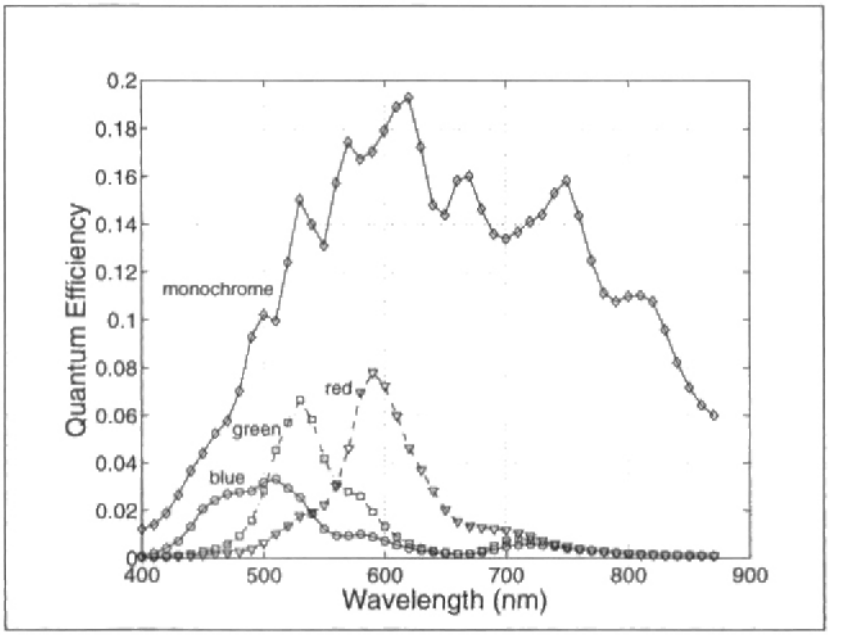


Figure 4-36. Quantum efficiency of the monochrome and colour sensors. The data has not been divided by the drawn pixel fill-factor.

The quantum efficiency of the colour pixels is approximately what might be expected by multiplying the quantum efficiency of the monochrome sensor with the transmission characteristics of the colour filters (Figure 4-6), and the CM-500M colour compensating filter characteristic (Figure 4-7) as shown in Figure 4-37. The measured quantum efficiency is not exactly as predicted due to the use of optical shields, and the presence of pixel cross talk. Overall, the quantum efficiency of the colour sensor is very low, particularly for the blue pixels.

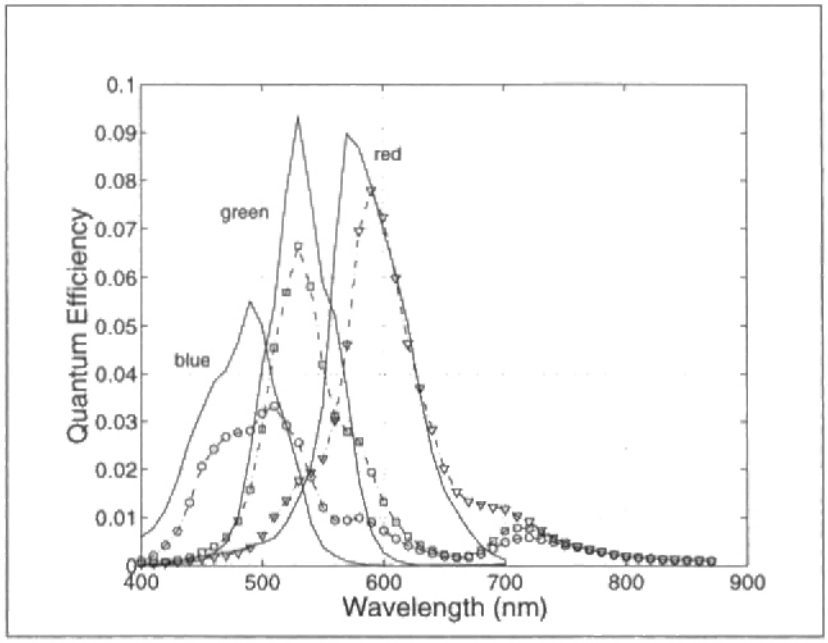


Figure 4-37. Predicted and measured quantum efficiency of the colour sensor represented by the solid and dashed traces respectively. The data has not been divided by the drawn pixel fill-factor.

4-12.4.1 Optical Light Shields

As part of the deposition of the colour filter array, opaque material was deposited over the portion of each pixel not corresponding to the photogate to form a light shield as shown in Figure 4-38. This was done to minimize the possibility of optical coupling or "light piping" between adjacent pixels that can degrade image sharpness and contribute to colour cross talk [Theuwissen 1995].

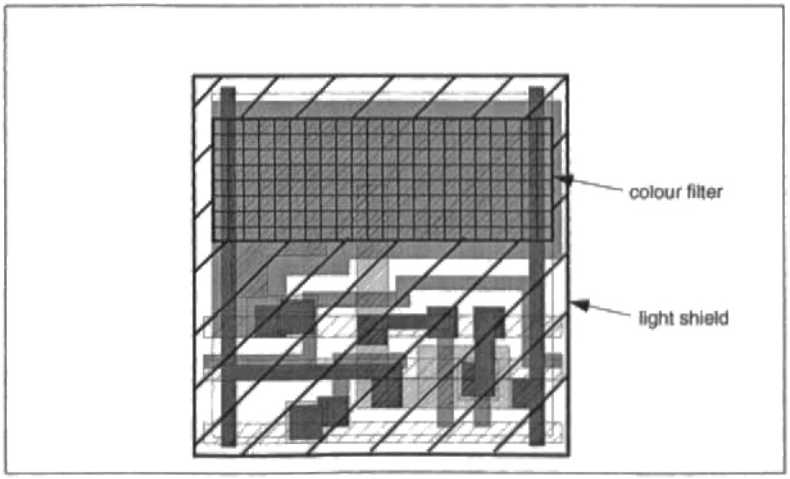


Figure 4-38. Light shield and colour filter deposited over the photogate pixel.

Inspection of Figure 4-37 suggests that in practice the pixel area responsible for the absorption of photons is substantially larger than the area of the photogate itself. This means that a significant proportion of the carriers collected in the potential well under the photogate are the result of diffusion through the substrate. This phenomenon can also degrade image sharpness and cause colour cross talk.

4-12.4.2 Colour Cross Talk

Colour cross talk occurs in solid-state image sensors that use colour filter arrays (CFA). It is due to photons being transmitted by the colour filter of one pixel, but the generated carriers being collected by a different pixel due to light piping or diffusion through the substrate [Lavine et al. 1983, Engelhardt and Seitz 1993]. Inspection of the quantum efficiency data reveals colour cross talk in the photogate sensor as highlighted in Figure 4-39. Significant cross talk from the red pixels into the green and blue pixels was identified, in addition to cross talk from green pixels into the blue pixels. This is consistent with the photon penetration depth being greater for longer wavelengths. It was also found that green pixels in the same rows as the red pixels had a slightly different quantum efficiency than the green pixels in the same rows as the blue pixels. This difference is most pronounced in terms of the level of red → green cross talk and suggests that cross talk from the red pixels occurs preferentially in the direction of the same row rather than along the same column. In Figure 4-39 the different green pixels have been denoted green1 (G1) and green2 (G2) respectively.

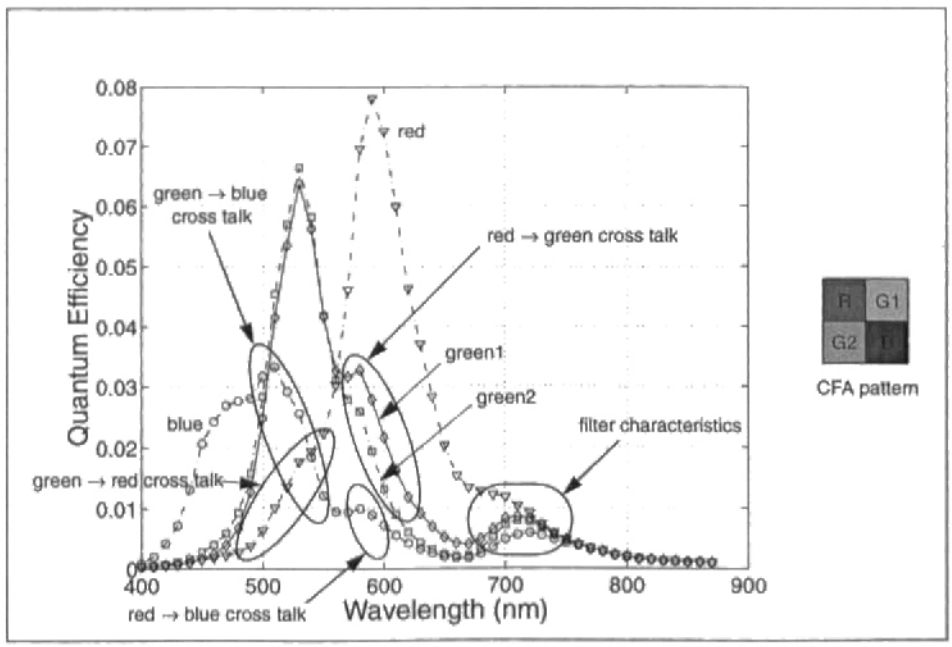


Figure 4-39. Quantum efficiency of the colour sensor demonstrating colour cross talk. The data has not been divided by the drawn pixel fill-factor.

It can also be seen in Figure 4-39 that the quantum efficiencies of the red, green, and blue pixels have a small peak near 720nm. This is because the transmission characteristic of the corresponding filters (Figure 4-6) and colour compensating filter (Figure 4-7) are not zero in this portion of the spectrum. This non-ideality also contributes to colour cross talk. The net result of colour cross talk in the photogate sensor is the mixing of colour components that degrades image sharpness and the colorimetric accuracy of the sensor. This will be discussed further in Section 4-13.6. Furthermore, the slight difference in quantum efficiency for green pixels in adjacent rows due to cross talk means that their optical sensitivities are also different. This has implications for performing colour interpolation that will be discussed in Section 5-7.6.4.

4-12.5 Quantum Efficiency of the Colour Sensor with Microlenses

Microlenses enhance sensor quantum efficiency through increasing the effective pixel fill-factor [Theuwissen 1995]. The measured quantum efficiency of the colour sensor with microlenses and light shield is shown in Figure 4-36. The quantum efficiency of the colour sensor with light shield alone has been superimposed for comparison.

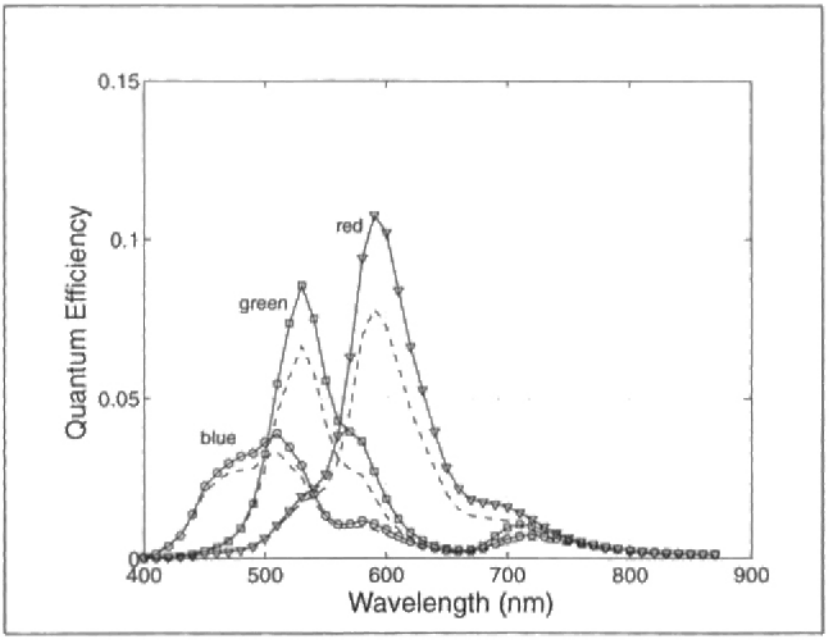


Figure 4-40. Quantum efficiency of the colour sensor with microlenses and light shield, and the colour sensor with light shield alone represented by solid and dashed traces respectively. The data has not been divided by the drawn pixel fill-factor.

The improvement in photogate sensor quantum efficiency due to the use of microlenses is quantified in Table 4-15. The percentage improvement in the peak quantum efficiency of the red, green, and blue pixels was 38%, 28%, and 18% respectively. These values are in approxi-

mate agreement with the 33%, 27%, and 15% improvement in mean optical sensitivity found using microlenses in Section 4-6.5.

Inspection of Figure 4-40 and Table 4-15 shows that the effectiveness of the microlenses in improving the sensor quantum efficiency has a clear dependence on the wavelength of the incident light. The microlenses provide greater optical gain in the red portion of the spectrum than the blue and also increase colour cross talk. As with any optical system, microlenses have a design wavelength λ_0 for which the lens design is optimal. For wavelengths significantly longer or shorter than λ_0 the microlens is less effective. The largest percentage increase in quantum efficiency for the colour photogate sensor with microlenses occurs at 620nm suggesting that λ_0 must be close to this wavelength.

η_{peak}	**red**	**green**	**blue**
without microlenses (light shield)	7.8%	6.7%	3.3%
with microlenses (light shield)	10.8%	8.6%	3.9%
% improvement due to microlenses	38%	28%	18%

Table 4-15. Peak quantum efficiency of the colour photogate sensor with and without microlenses.

4-12.6 Quantum Efficiency with Microlenses and No Light Shield

Colour photogate sensors with microlenses were also fabricated with no light shield. The measured quantum efficiency of the colour sensor with microlenses and no light shield is shown in Figure 4-41. The quantum efficiency of the colour sensor with microlenses and light shield has been superimposed for comparison.

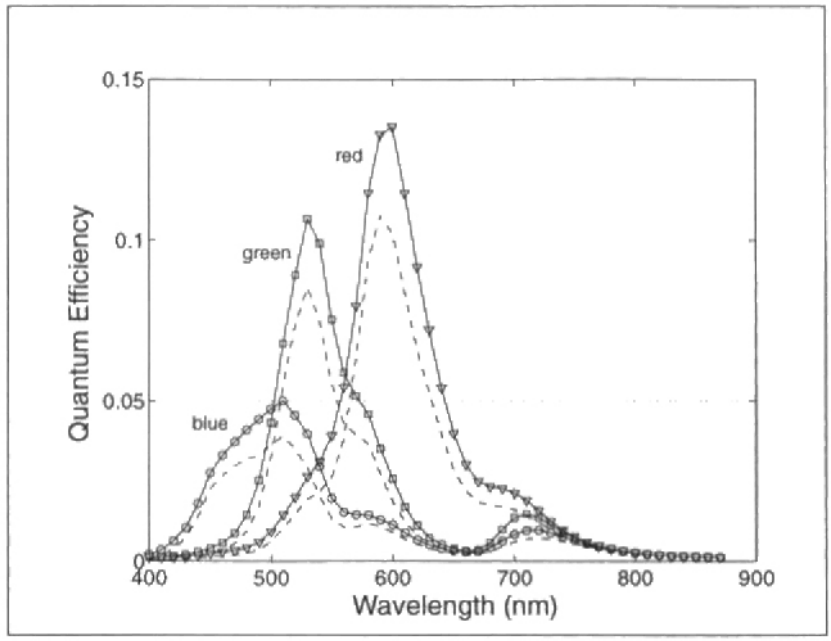


Figure 4-41. Quantum efficiency of the colour sensor with microlenses and no light shield, and the colour sensor with microlenses and light shield represented by solid and dashed traces respectively. The data has not been divided by the drawn pixel fill-factor

Inspection of Figure 4-41 suggests that the light shield uniformly reduces the quantum efficiency of the red, green, and blue pixels. The decrease in peak quantum efficiency due to the use of the light shield is quantified in Table 4-15. The percentage reduction in quantum efficiency is approximately the same for the red, green, and blue pixels. It is also apparent from Figure 4-41 that the light shield does not reduce the relative amount of colour cross talk between pixels. This implies that the dominant mechanism by which colour cross talk occurs is diffusion of carriers through the substrate and not light piping. The use of the light shield is therefore of dubious merit as it degrades the overall sensor quantum efficiency.

η_{peak}	**red**	**green**	**blue**
with microlenses and light shield	10.8%	8.6%	3.9%
with microlenses and no light shield	13.5%	10.7%	5.0%
% reduction due to light shield	25%	24%	28%

Table 4-16. Peak quantum efficiency of the colour photogate sensor with microlenses both with and without light shield.

4-13. Colorimetric Performance

As reviewed in Chapter 3 colour camera technology is largely independent of the underlying solid-state imaging technology. Colour filter arrays, microlenses, and subsequent stages of colour processing such as spatial interpolation, colour correction, and gamma correction are similar for CMOS or CCD based cameras. However, the performance of a colour camera is significantly determined by the performance of the solid-state image sensor. To establish the colorimetric accuracy and noise performance of the colour photogate sensor a digital colour camera was realized in software on a PC. As the purpose of the software implementation was to elucidate these performance parameters, only the minimum requirements for realizing a digital colour camera system were supported.

4-13.1 Colour Processing Architecture

To generate 24-bit colour images from the colour photogate sensor the digitized pixel values acquired by the PC were subject to spatial interpolation, colour correction, and gamma correction as illustrated in Figure 4-42.

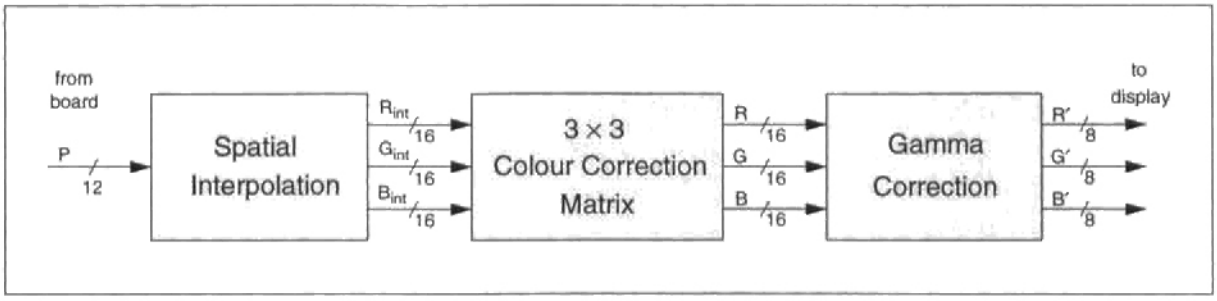


Figure 4-42. Colour processing architecture.

The colour processing was performed using 16-bit integer arithmetic to preserve accuracy and truncated to 8-bits per colour component during gamma correction. Frames of dimension 352×288 were acquired from the colour photogate sensor and processed by the PC.

4-13.1.1 Spatial Interpolation

The use of a colour filter array (CFA) to realize a single-chip colour image sensor necessitates spatial interpolation to construct three colour components for each pixel. As the interpolation scheme does not play a significant role in the colorimetric accuracy of a colour camera, an elementary interpolation procedure based on low-pass filter routines was used with the photogate sensor for ease of implementation. The interpolation algorithm used is the same as that employed by the single-chip camera and will be described fully in Section 5-7.1. It involves averaging pixel values corresponding to the same colour over a 3×3 pixel neighbourhood. While this scheme produced visible colour aliasing artifacts at luminance transitions in the

image, these could be reduced with a more advanced interpolation technique and are not indicative of the colour photogate sensor itself [Parulski et al. 1989, Hibbard 1995]. To simplify the spatial interpolation routine no interpolation was performed for the pixels along the image perimeter and so the interpolated component images R_{int}, G_{int}, and B_{int} had dimensions 350 × 286.

4-13.1.2 Colour Correction

To improve the colour rendition of the sensor and transform into a standard colour space a linear 3 × 3 matrix operation $\boldsymbol{C}$ was applied to the interpolated colour components for each pixel [Parulski 1985]. After the application of $\boldsymbol{C}$ post-offsets were added to the corrected red, green, and blue components respectively. Colour correction for the colour photogate sensor is described by:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{bmatrix} \begin{bmatrix} R_{int} \\ G_{int} \\ B_{int} \end{bmatrix} + \begin{bmatrix} offset_R \\ offset_G \\ offset_B \end{bmatrix} \tag{4-60}$$

When determining the coefficients of the colour correction matrix it is useful to consider $\boldsymbol{C}$ as the product of two 3 × 3 matrices denoted $\boldsymbol{H}$ and $\boldsymbol{P}$:

$$\boldsymbol{C} = \boldsymbol{PH} \tag{4-61}$$

The matrix $\boldsymbol{H}$ transforms the interpolated colour components from the photogate sensor into the CIE *XYZ* colour space [Wyszecki and Stiles 1982]. A procedure for determining the coefficients of $\boldsymbol{H}$ is described in Section 3-4.27. Finding the matrix $\boldsymbol{H}$ enables the colorimetric accuracy of the photogate sensor to be established.

The matrix $\boldsymbol{P}$ maps from the CIE *XYZ* colour space into the colour space of the CRT display primaries. As the necessary data concerning the primaries of the CRT display was not available it proved convenient to use the published transformation between the CIE *XYZ* colour space and the colour space of the NTSC primaries with a D_{65} white point as given by (4-62) [Sproson 1983]. While this choice may result in minor shifts for some colours it proved satisfactory for the purposes of displaying colour images from the photogate sensor.

$$\boldsymbol{P} = \begin{bmatrix} 1.9709 & -0.5494 & -0.2974 \\ -0.9538 & 1.9364 & -0.0274 \\ 0.0638 & -0.1294 & 0.9814 \end{bmatrix} \tag{4-62}$$

4-13.1.3 Gamma Correction

Gamma correction was applied to each of the colour components to correct for the characteristic non-linearity of the display cathode ray tube (CRT) according to [Poynton 1996]:

$$R' = R^{\gamma}, B' = B^{\gamma}, \text{and } G' = G^{\gamma} \tag{4-63}$$

The value of gamma, γ, was adjustable and implemented as a lookup table. As part of this process each colour component was truncated to 8-bits as required for 24-bit colour display by the PC.

4-13.2 The Colour Experiment

The matrix $\boldsymbol{H}$ defined as part of the colour correction matrix was determined empirically using 24 colour samples provided by the Macbeth ColorChecker colour rendition chart. The experimental setup is shown in Figure 4-43. A lens assembly with focus and adjustable aperture was used to focus an image of the chart onto the colour photogate sensor. A CM-500M colour compensating filter was used to suppress infra-red. D_{65} illumination was provided by a pair of Macbeth Sol-Source lamps.

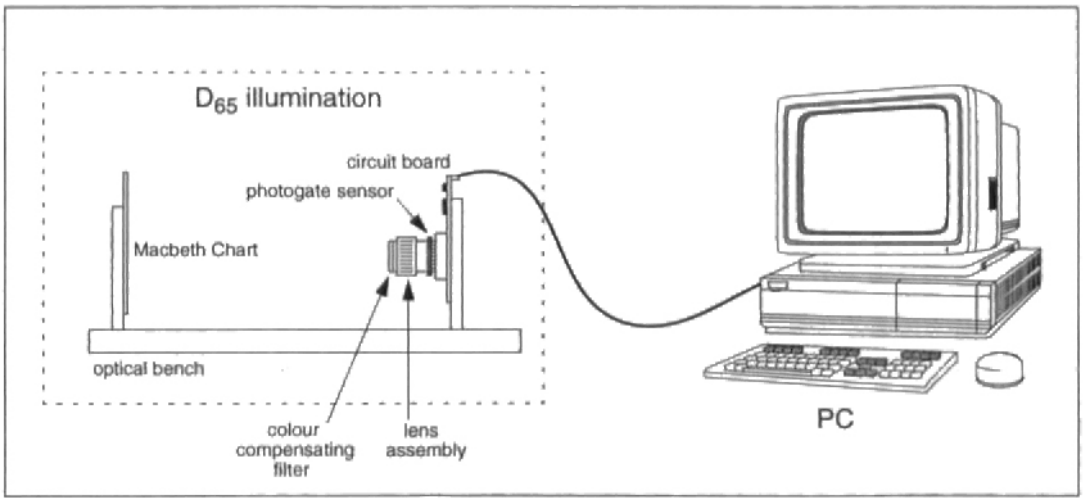


Figure 4-43. Colour photogate sensor experimental setup. A pair of Macbeth Sol-Source lamps provided the D_{65} illumination (not shown).

4-13.2.1 D_{65} Illumination

To accurately express colour information using tristimulus values such as (R, G, B) or (X, Y, Z) requires the specification of the illuminant or white point [Hunt 1995]. The CIE has provided a number of standard illuminants to support the exchange of colour information including the D6500K or D_{65} illuminant that represents daylight [Wyszecki and Stiles 1982]. The procedure employed to determine the matrix $\boldsymbol{H}$ requires that the same illuminant, prefera-

bly a CIE standard illuminant, be employed for both acquiring the colour samples with the photogate sensor, and measuring the tristimulus values of the colour samples. The availability of Macbeth Sol-Source lamps allowed the use of the D_{65} standard illuminant.

4-13.2.2 The Macbeth ColorChecker Colour Rendition Chart

The Macbeth ColorChecker chart is widely used to assess the colorimetric performance of colour acquisition and reproduction devices [Martinez et al. 1993]. It contains 24 different colour samples that include the additive primary colours (red, green, and blue), the subtractive primary colours (cyan, magenta, and yellow), a neutral series ranging from white to black, and colours representative of subjects such as human skin, foliage, and blue sky. The colour samples are numbered according to Figure 4-44 [Macbeth]. A Minolta CR-110 Chroma Meter and DP-100 Data Processor were used to measure the luminous reflectance values Y and chromaticity coordinates (x, y) for each of the colour samples with a D_{65} illuminant. For each colour sample a number of measurements were performed and the results averaged. Using (3-12) the CIE *(X, Y, Z)* tristimulus values for the colour samples were found. The matrix given in (4-62) was then applied to find the NTSC *(R, G, B)* tristimulus values for the colour samples. The mean *(X, Y, Z)* and NTSC *(R, G, B)* tristimulus values for the colour samples of the Macbeth ColorChecker are listed in Table B-1.

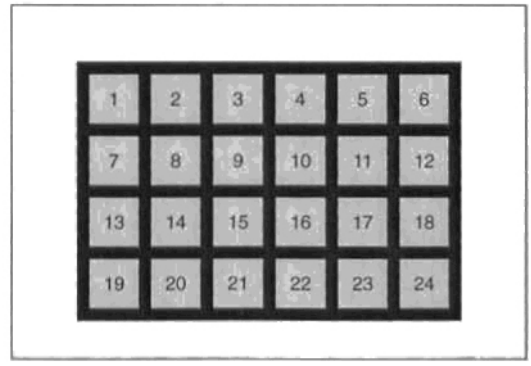


Figure 4-44. Numbering of the colour samples of the Macbeth ColorChecker colour rendition chart.

4-13.2.3 Acquiring the Colour Samples

An image of the Macbeth ColorChecker colour rendition chart was acquired by the colour photogate image sensor under D_{65} illumination using the experimental arrangement of Figure 4-43. The aperture on the lens assembly was $f/2.0$ and the integration period of the photogate sensor was 90ms. The image was interpolated and for each colour sample of the chart, regions of 30×30 pixels were averaged to yield the mean tristimulus values $(R_{int}, G_{int}, B_{int})$ for each sample. The mean $(R_{int}, G_{int}, B_{int})$ values were normalized to 255 and are listed in Table B-2.

4-13.2.4 Finding the Colour Correction Matrix

As the matrix $\boldsymbol{P}$ is given by the display primaries, finding the colour correction matrix $\boldsymbol{C}$ is the task of determining the transformation $\boldsymbol{H}$. If the post-offsets of (4-60) are required to improve colour rendition, then they must be found also. As discussed in Section 3-4.27 most methods for determining the coefficients of $\boldsymbol{H}$ are based on minimizing a colour error metric. For a given matrix $\boldsymbol{H}$, estimates of the CIE *XYZ* tristimulus values $(\hat{X}, \hat{Y}, \hat{Z})$ for the 24 samples of the Macbeth ColorChecker can be found from the interpolated tristimulus values $(R_{int}, G_{int}, B_{int})$ of Table B-2 using:

$$\begin{bmatrix} \hat{X} \\ \hat{Y} \\ \hat{Z} \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} & h_{13} \\ h_{21} & h_{22} & h_{23} \\ h_{31} & h_{32} & h_{33} \end{bmatrix} \begin{bmatrix} R_{int} \\ G_{int} \\ B_{int} \end{bmatrix} \tag{4-64}$$

The actual CIE *XYZ* tristimulus values (X, Y, Z) for the samples of the Macbeth ColorChecker are given in Table B-1. A number of different colour error metrics are available to quantify the difference between the (X, Y, Z) and $(\hat{X}, \hat{Y}, \hat{Z})$ tristimulus values. To find the optimal colour correction matrix for the colour photogate sensor the author explored two different approaches, the mean squared error in the CIE *XYZ* colour space, and the RMS colour difference in the CIE $L^*u^*v^*$ colour space.

4-13.3 The Mean Squared Error in the CIE *XYZ* Colour Space

One of the simplest colour error metrics to minimize is the mean squared error (MSE) in the CIE *XYZ* colour space:

$$MSE_{XYZ} = \frac{1}{24} \sum_{r=1}^{24} \left(\left(X_r - \hat{X}_r \right)^2 + \left(Y_r - \hat{Y}_r \right)^2 + \left(Z_r - \hat{Z}_r \right)^2 \right) \tag{4-65}$$

4-13.3.1 The Least-Squares Method

Choosing the MSE in the CIE *XYZ* colour space as the colour error metric allows an analytical solution to be found using the least-squares method which is described in Section B-3. Using MATLAB to perform the matrix calculations the MSE in the CIE *XYZ* colour space was found to be 7.296 and the optimal matrix $\boldsymbol{H}$:

$$\boldsymbol{H} = \begin{bmatrix} 0.5245 & 0.1966 & 0.1016 \\ -0.0249 & 1.2667 & -0.3419 \\ -0.2912 & -1.2649 & 2.4834 \end{bmatrix} \tag{4-66}$$

Multiplying by the matrix $\boldsymbol{P}$ given in (4-62) yields the colour correction matrix:

$$\boldsymbol{C} = \begin{bmatrix} 1.1317 & 0.0677 & -0.3498 \\ -0.5409 & 2.3017 & -0.8276 \\ -0.2493 & -1.3940 & 2.4902 \end{bmatrix} \tag{4-67}$$

4-13.3.2 Finding Post-Offsets that Minimize the MSE

The MSE can be reduced further by the use of offset terms. This can be achieved by re-writing (4-64) in the form:

$$\begin{bmatrix} \hat{X} \\ \hat{Y} \\ \hat{Z} \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} & h_{13} & offset_R \\ h_{21} & h_{22} & h_{23} & offset_G \\ h_{31} & h_{32} & h_{33} & offset_B \end{bmatrix} \begin{bmatrix} R_{int} \\ G_{int} \\ B_{int} \\ 1 \end{bmatrix} \tag{4-68}$$

and then using the least-squares algorithm to find the new optimal matrix $\boldsymbol{H}$:

$$\boldsymbol{H} = \begin{bmatrix} 0.5600 & 0.1462 & 0.1756 & -5.7940 \\ 0.0178 & 1.2059 & -0.2528 & -6.9725 \\ -0.2741 & -1.2891 & 2.5189 & -2.7804 \end{bmatrix} \tag{4-69}$$

Multiplying by $\boldsymbol{P}$ gives a 3×4 matrix, the first 3 rows and columns of which form the new colour correction matrix $\boldsymbol{C}$. This procedure yields a MSE in the CIE *XYZ* colour space of 6.136 and colour correction matrix and post-offsets of:

$$\boldsymbol{C} = \begin{bmatrix} 1.1731 & 0.0089 & -0.2637 \\ -0.4925 & 2.2328 & -0.7267 \\ -0.2358 & -1.4131 & 2.5182 \end{bmatrix}, \text{post-offsets} \begin{bmatrix} -6.7481 \\ -7.9056 \\ -2.1975 \end{bmatrix} \tag{4-70}$$

While it is convenient computationally to use the MSE in the CIE *XYZ* colour space as the colour error metric, most practical methods for finding the optimal colour correction matrix do not use this approach. This is because the CIE *XYZ* colour space is not perceptually uniform. As a direct consequence (4-65) does not yield an equal measure of colour error as seen by a human observer for *(X, Y, Z)* and $(\hat{X}, \hat{Y}, \hat{Z})$ tristimulus values in different portions of the *XYZ* colour space. This problem can be addressed by using a colour error metric in the CIE $L^*u^*v^*$ or CIE $L^*a^*b^*$ perceptually uniform colour spaces instead [Engelhardt and Seitz 1993, Lenz and Lenz 1996, Suzuki et al. 1990].

4-13.4 The RMS *L*u*v** Colour Difference

The other colour error metric used by the author to find the matrix $\boldsymbol{H}$ for the colour photogate sensor was the RMS colour difference in the CIE $L^*u^*v^*$ colour space, $(\Delta E^*_{uv})_{RMS}$. For a given matrix $\boldsymbol{H}$, estimates of the CIE XYZ tristimulus values $(\hat{X}, \hat{Y}, \hat{Z})$ for the 24 samples of the Macbeth ColorChecker can be found from the interpolated tristimulus values $(R_{int}, G_{int}, B_{int})$ of Table B-2 using:

$$\begin{bmatrix} \hat{X} \\ \hat{Y} \\ \hat{Z} \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} & h_{13} \\ h_{21} & h_{22} & h_{23} \\ h_{31} & h_{32} & h_{33} \end{bmatrix} \begin{bmatrix} R_{int} \\ G_{int} \\ B_{int} \end{bmatrix} \tag{4-71}$$

The transformation of CIE XYZ tristimulus values into the CIE $L^*u^*v^*$ colour space is described in Section 3-4.18. Using this transformation a $(\hat{L}^*, \hat{u}^*, \hat{v}^*)$ and (L^*, u^*, v^*) tristimulus value for each of the colour samples can be found from the $(\hat{X}, \hat{Y}, \hat{Z})$ estimates computed using (4-71), and the actual (X, Y, Z) tristimulus values listed in Table B-1 respectively. The RMS colour difference over the 24 colour samples is then given by:

$$(\Delta E^*_{uv})_{RMS} = \sqrt{\frac{1}{24}\sum_{r=1}^{24}\left(\left(L^*_r - \hat{L}^*_r\right)^2 + \left(u^*_r - \hat{u}^*_r\right)^2 + \left(v^*_r - \hat{v}^*_r\right)^2\right)} \tag{4-72}$$

As the transformation from the CIE XYZ to the CIE $L^*u^*v^*$ colour space is non-linear, it not possible to find an analytical solution for $\boldsymbol{H}$ and instead numerical methods must be applied.

4-13.4.1 The Conjugate Gradient Method

The numerical optimization method used to find the matrix $\boldsymbol{H}$ that minimized $(\Delta E^*_{uv})_{RMS}$ was the conjugate gradient algorithm and is described in Section B-4 [Chong and Zak 1996]. The conjugate gradient algorithm was implemented in MATLAB and successfully converged to the same solution within 300 iterations from any random initial value $\boldsymbol{H}_0$. The optimal matrix $\boldsymbol{H}$ was found to be:

$$\boldsymbol{H} = \begin{bmatrix} 0.4504 & 0.2951 & 0.0526 \\ -0.1126 & 1.4026 & -0.4154 \\ -0.3789 & -1.0966 & 2.3950 \end{bmatrix} \tag{4-73}$$

which yields a RMS colour difference $(\Delta E^*_{uv})_{RMS}$ of 8.520 *units RMS* over the 24 samples of the Macbeth ColorChecker.

Multiplying by the matrix $\boldsymbol{P}$ given in (4-62) yields the colour correction matrix:

$$C = \begin{bmatrix} 1.0601 & 0.1368 & -0.3796 \\ -0.6378 & 2.4665 & -0.9209 \\ -0.3288 & -1.2400 & 2.4097 \end{bmatrix} \tag{4-74}$$

4-13.4.2 Finding Post-Offsets that Minimize the RMS $L^*u^*v^*$ Colour Difference

The RMS colour difference was further reduced by finding the optimal offsets in a similar manner to that described in Section 4-13.3.2 The conjugate gradient algorithm was used to find the optimal matrix $\boldsymbol{H}$ of the form shown in (4-68). This procedure yielded a RMS colour difference $(\Delta E^*_{uv})_{RMS}$ of 7.678 *units RMS* and colour correction matrix and post-offsets of:

$$C = \begin{bmatrix} 1.1080 & 0.0256 & -0.1960 \\ -0.5892 & 2.3518 & -0.7164 \\ -0.3082 & -1.3188 & 2.5419 \end{bmatrix}, \text{post-offsets} \begin{bmatrix} -7.5472 \\ -8.7820 \\ -4.1656 \end{bmatrix} \tag{4-75}$$

4-13.5 Comparing the Performance of the Colour Error Metrics

4-13.5.1 Numerical Comparison of Colour Error Metrics

The results obtained using the two different colour error metrics are shown in Table 4-17. For each result the corresponding value of the alternative colour error metric has also been computed. The values for each of the colour error metrics prior to colour correction are also given. It is apparent that the application of the colour correction matrices substantially improves the colour rendition of the photogate sensor.

Optimization Method and Colour Error Metric	MSE_{XYZ}	$(\Delta E^*_{uv})_{RMS}$
no colour correction	76.53	40.59
least-squares	7.30	8.92*
least-squares with offsets	6.14	7.94*
conjugate gradient	8.45**	8.52
conjugate gradient with offsets	6.96**	7.68

Table 4-17. Comparison of colour error metrics obtained using different optimization methods. The entries labelled * were computed from the matrix found using the MSE in the *XYZ* colour space. The entries labelled ** were computed from the matrix found using the RMS $L^*u^*v^*$ colour difference.

It is held that in the CIE $L^*u^*v^*$ colour space a colour difference of 1 corresponds to a "just noticeable difference" between two colour samples. From the values listed in the last column of Table 4-17 it can be expected that the improvement in colour rendition provided by matrices found using both methods is similar, and that employing the RMS colour difference in the CIE

$L^*u^*v^*$ colour space does not yield a significantly higher level of colorimetric accuracy as is generally found [Sproson 1983]. Possible reasons for this will be presented shortly.

4-13.5.2 Visual Comparison of Colour Error Metrics

To visually assess the result of applying a given colour correction matrix a program was written to generate a 24-bit colour image to display the actual samples of the Macbeth ColorChecker together with those rendered by the photogate sensor after colour correction. By viewing the image on a 24-bit display with a D_{65} white point the accuracy of the colour match could be subjectively evaluated. Two such images representing colour correction found by minimizing the MSE in the CIE *XYZ* colour space and the RMS $L^*u^*v^*$ colour difference have been reproduced in Plate 1(a) and (b) respectively. Although the photographic process has altered the absolute colours, the relative colour differences are close to how they appear when displayed. The small squares give the measured colours while the surrounds give the acquired data from the photogate sensor after colour correction. Inspection of Plate 1(a) and (b) reveals that a fair colour match is made for most of the samples. The most notable exception is sample 17 which is "magenta". It is also apparent from Plate 1(a) and (b) that both procedures used to find the colour correction matrix yield similar colour errors for each sample. This is numerically quantified in Table B-3 where the CIE $(\Delta L^*, \Delta u^*, \Delta v^*)$ colour difference errors for each colour sample for both colour correction matrices have been computed and are shown to be comparable.

4-13.5.3 Comparison With Other Solid-State Image Sensors

To compare the colorimetric performance of the photogate sensor with other solid-state image sensors it is necessary to find studies in which the same colour error metric and colour samples were used. In an investigation by Kollarits and Gibbon they report on a model camera system based on a CCD sensor with three primary colour filters [Kollarits and Gibbon 1990]. Colour separation was achieved by placing each of the colour filters in turn between a single monochrome CCD sensor and the target. While this technique avoided the need for spatial interpolation it was only suitable for still-images. A value for $(\Delta E^*_{uv})_{RMS}$ of 4.76 *units RMS* was found by minimization over the 24 samples of the Macbeth ColorChecker using a numerical perturbation method. This result is significantly lower than those obtained for the photogate sensor listed in Table 4-17 and indicates that the colorimetric accuracy of the photogate sensor is poorer than that of the CCD-based camera of Kollarits and Gibbon.

4-13.6 Factors Limiting the Colorimetric Accuracy

4-13.6.1 The Colour Analysis Functions of the Photogate Sensor

Fundamentally the colorimetric accuracy of any solid-state image sensor is limited by the shape of the colour analysis functions. The colour analysis functions realized by the photogate

sensor before and after colour correction are shown in Figure 4-45(a) and (b) respectively. The colour analysis functions before colour correction are given by the quantum efficiencies of the red, green, and blue pixels multiplied by the gains necessary to achieve white balance for a D_{65} illuminant. The colour analysis functions after colour correction are found by application of the colour correction matrix. In principle the shape of the sensor colour analysis functions after colour correction shown in Figure 4-45(b) should be the same as the ideal NTSC colour analysis functions given in Figure 3-13. In practice substantial differences exist. The most important of these concerns the blue colour analysis function, with its peak at 480nm rather than 440nm, and its excessive negative transition. The non-ideal shape of the colour analysis functions are due to substantial colour cross talk, and the poor quantum efficiency of the photogate sensor in the blue region of the spectrum.

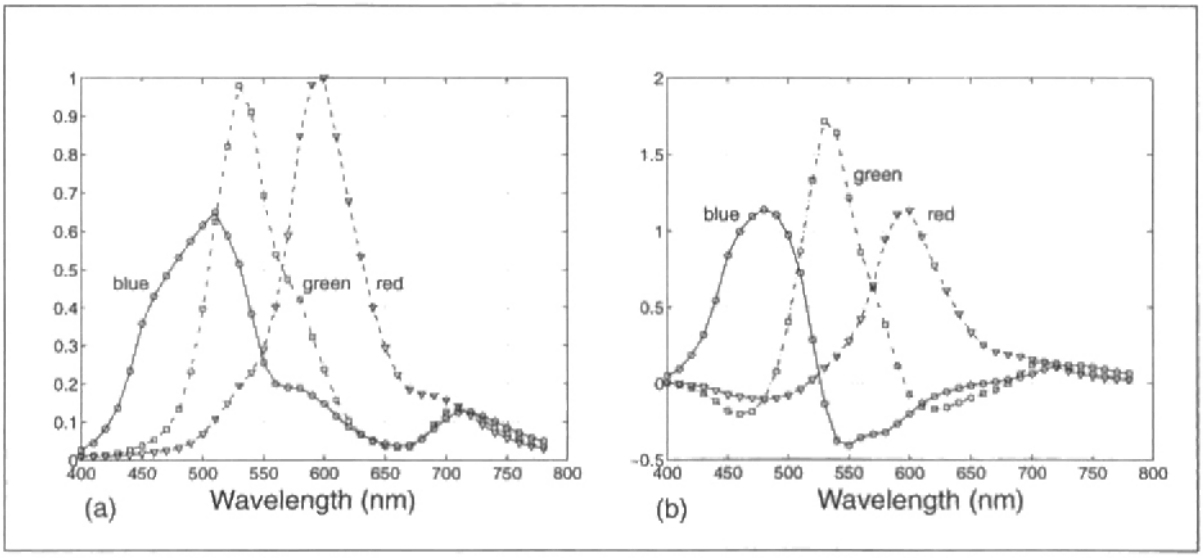


Figure 4-45. The colour analysis functions of the photogate sensor (a) before, and (b) after application of colour correction matrix (4-67). The colour analysis functions prior to colour correction have been normalized to achieve white balance for a D_{65} illuminant.

4-13.6.2 Colour Cross Talk

Colour cross talk in the photogate sensor was identified in Section 4-12.4.2. In Figure 4-45 it is clear that colour cross talk limits the ability of the photogate sensor to realize the ideal NTSC colour analysis functions. This is particularly true for the blue pixels where cross talk ensures that the blue colour analysis function shown in Figure 4-45(a) has significant response for wavelengths between 500nm and 750nm. As a consequence the colour correction matrices determined in Section 4-13.3 and Section 4-13.4 have substantial negative values for coefficients c_{21}, c_{23}, and c_{32} of the colour correction matrix to try and cancel cross talk from the red and green pixels.

4-13.6.3 Poor Sensor Quantum Efficiency

The presence of significant colour cross talk in the photogate sensor is exacerbated by the poor quantum efficiency of the monochrome photogate sensor in the blue region of the spectrum. This allows a substantial percentage of the blue response of the sensor to be contributed by cross talk rather than the collection of carriers generated by short wavelength photons. Furthermore, the poor quantum efficiency of the sensor at short wavelengths shifts the peak of the blue response. In Figure 4-6 the peak of the blue colour filter characteristic is at 450nm, as required by the ideal blue NTSC colour analysis function. However the shape of the quantum efficiency of the monochrome photogate sensor given in Figure 4-35 shifts this peak to 510nm. The colour correction matrix is only able to move this peak back to 480nm, with a corresponding loss in colorimetric accuracy.

4-13.6.4 Comparisons with Other Solid-State Image Sensors

It is now possible to account for the difference in colorimetric accuracy between the photogate sensor and the camera system of Kollarits and Gibbon discussed in Section 4-13.5.3 [Kollarits and Gibbon 1990]. Colour separation in the camera system of Kollarits and Gibbon was not achieved using a colour filter array but by mechanically changing a global colour filter and combining the different frames. It was therefore not subject to colour cross talk that might reduce its colorimetric accuracy in the manner found for the photogate sensor. However, inspection of the colour analysis functions reported for CCD sensors with colour filter arrays suggests that colour cross talk in the photogate sensor is still significantly larger than that found in CCD sensors that use CFAs [Naito et al. 1995, Nishima et al. 1995]. This is not unexpected as the CCD pixel structure and doping concentrations of the substrate are optimized to control the diffusion length of minority carriers [Stevens and Lavine 1994]. In comparison the photogate sensor was fabricated in a standard digital CMOS process were no special measures were taken to minimize cross talk within the substrate.

4-13.7 Degradation of Signal-to-Noise Performance

While the application of the colour correction matrix $\boldsymbol{C}$ provides substantial improvement in colour rendition it has an unwelcome impact on the noise performance of a colour sensor [Sproson 1983, Parulski 1985, Poynton 1996]. As the noise in the R_{int}, G_{int}, and B_{int} components are independent, their noise variances add and are weighted by the coefficients of $\boldsymbol{C}$ to give the noise in the colour corrected components R, G, and B which can be computed using:

$$\sigma_{t_R} = \sqrt{(c_{11}\sigma_{t_{Rint}})^2 + (c_{12}\sigma_{t_{Gint}})^2 + (c_{13}\sigma_{t_{Bint}})^2} \quad Volts\ RMS \tag{4-76}$$

$$\sigma_{t_G} = \sqrt{(c_{21}\sigma_{t_{Rint}})^2 + (c_{22}\sigma_{t_{Gint}})^2 + (c_{23}\sigma_{t_{Bint}})^2} \quad Volts\ RMS \tag{4-77}$$

$$\sigma_{t_B} = \sqrt{(c_{31}\sigma_{t_{Rint}})^2 + (c_{32}\sigma_{t_{Gint}})^2 + (c_{33}\sigma_{t_{Bint}})^2} \quad Volts\ RMS \tag{4-78}$$

where $\sigma_{t_{Rint}}$, $\sigma_{t_{Gint}}$, and $\sigma_{t_{Bint}}$ are the RMS temporal noise components in R_{int}, G_{int}, and B_{int} respectively, and σ_{t_R}, σ_{t_G}, and σ_{t_B} are the RMS temporal noise components in R, G, and B. As many of the off-diagonal elements of C are comparable to the diagonal elements the signal-to-noise ratio of the sensor after colour correction is significantly degraded.

The degradation of the signal-to-noise ratio of the photogate sensor with the application of the colour correction matrix can be illustrated with a numerical example for 1-lux faceplate illumination and a 30ms integration time. Under this exposure the sensor is photon shot noise limited and using the optical sensitivity data of Table 4-7 together with (2-12), (2-23), and (4-22) the number of signal electrons N_{signal}, the number of RMS electrons representing the photon shot noise $n_{photons\ shot}$, and the SNR for each colour can be calculated. Based on the ratio of N_{signal} between the colour channels, the relative gains necessary to achieve white balance can be found. This data corresponding to the performance of the sensor prior to colour correction is given in the first half of Table 4-18. While (4-60) and (4-76)-(4-78) relate voltage quantities, they can be used in an equivalent sense for the purposes of this calculation with sensor signal and noise components represented using electrons and RMS electrons respectively. If the colour correction matrix given by (4-74) is applied, then the equivalent number of signal electrons N_{signal} and RMS electrons representing the photon shot noise $n_{photons\ shot}$ are given in the second half of Table 4-18 together with the SNR for each colour.

Colour	Before Colour Correction				After Colour Correction		
	N_{signal} (electrons)	$n_{photon\ shot}$ (RMS electrons)	White Balance Gains	SNR (dB)	N_{signal} (electrons)	$n_{photon\ shot}$ (RMS electrons)	SNR (dB)
red	1851	43	1.000	32.7	1513	52	29.2
green	1521	39	1.217	31.8	1680	134	22.0
blue	816	29	2.268	29.1	1556	167	19.4

Table 4-18. The signal-to-noise performance of the colour photogate sensor at 1-lux faceplate illumination both before and after application of the colour correction matrix (4-74). The data corresponds to an illuminant consisting of a 3200K tungsten halogen lamp with BG0.40 colour compensating filter.

For this example the SNR of the green and blue channels of the photogate sensor are degraded by 10dB with the application of the colour correction matrix. This is due to the low sensitivity of the blue pixels, and substantial colour cross talk which results in large absolute values for the coefficients c_{21}, c_{23}, and c_{32}.

4-13.8 Example Images

The colour correction matrix was applied to an interpolated image acquired using the photogate sensor under D_{65} illumination at an ambient level of 4.3-lux. The image before and after colour correction are reproduced in Plate 2(a) and (b) respectively. The improvement in colour rendition is striking. While it is difficult to see the degradation in SNR due to colour correction in the images provided, the colour aliasing artifacts are more noticeable. The use of more sophisticated interpolation schemes could be used to reduce their visibility [Parulski et al. 1989, Hibbard 1995].

4-13.9 Subjective Comparison

In the bulk of this chapter various performance parameters of the photogate sensor have been determined and compared with reported values for other CMOS and CCD sensors. However, it should be noted that by virtue of their publication most of these sensors are or were state-of-the-art in some aspect of their design or performance. Therefore to gain greater perspective on the performance of the photogate sensor was subjectively compared with a low-end colour CCD-based multi-media camera under normal fluorescent room lighting [Connectix]. It was found that the colour photogate provided a cleaner imaging with superior colour rendition. However, the performance of both sensors was substantially degraded at low-light levels. This suggests that while many performance parameters of the photogate sensor are not competitive with that of state-of-the-art CCD sensors, the performance of the photogate sensor is comparable or better than that of low-end CCD sensors.

4-14. Conclusion

It is now possible to summarize the performance of the photogate sensor, to form conclusions regarding the performance limitations of CMOS image sensors in general, and to suggest how each of these limitations might be addressed.

4-14.1 Performance Summary of the Photogate Sensor

The performance of the CMOS photogate sensor evaluated in this chapter is summarized in Table 4-19.

Pixel Design	Single-poly photogate
Technology	Lucent Technologies 0.8μm CMOS
Resolution	352 × 288
Pixel Dimensions	16.0μm × 16.0μm
Pixel Fill-Factor	35% (drawn active area)
Dark Current Density	183pA/cm^2 at 25°C
Saturation	1.38V (49 K electrons)
Read Noise	121.5μV RMS 455.0μV RMS including CDS
Dynamic Range	73.6 dB (30ms integration, 25°C) 68.4 dB including CDS
Monochrome Sensitivity	4.25V/lux.s
Colour Sensitivity	Red 1.73V/lux.s Green 1.42V/lux.s Blue 0.76V/lux.s
Conversion Gain	28μV/electron (70μV/electron pixel referred)
Fixed-pattern Noise	0.29% peak-to-peak of saturation
Peak Quantum Efficiency	19%
Supply Voltage	5.0V
Power Dissipation	50mW

Table 4-19. Summary of photogate sensor performance. The optical sensitivity values were obtained using a 3200K tungsten halogen lamp and colour compensating filter.

4-14.2 Performance Limitations of CMOS Image Sensors

4-14.2.1 Fixed-Pattern Noise

It has been widely assumed that mismatch of pixel and column read-out circuits is the factor limiting the FPN performance of CMOS image sensors, and that this gives rise to the FPN advantage that CCD sensors enjoy over CMOS sensors. The author has been able to demonstrate that with the use of two levels of correlated-double sampling all FPN due to circuit mismatch is cancelled, and instead the sensor FPN performance is limited by dark current non-uniformity at low signal levels, and pixel conversion gain non-uniformity at high signal levels (Figure 4-32). For the CMOS photogate evaluated in this chapter, the level of FPN due to dark current non-uniformity is approximately 3 times greater than that of a FT-CCD sensor without surface pinning or charge pumping, and a factor of 20 larger than a FT-CCD with surface pinning (Table 4-13). The difference in dark current performance between CMOS and CCD sensors becomes more pronounced as the feature dimensions of CMOS fabrication tech-

nology are reduced. It is therefore clear that CMOS sensors manufactured in a standard CMOS process cannot compete with the FPN performance achieved by their CCD counterparts. However, it is significant that the FPN performance of CMOS active pixel sensors using two levels of CDS is not read-out circuit limited. Fundamentally, this means that the read-out architectures of CCD sensors do not possess any inherent FPN advantage over the architectures of CMOS imagers. Furthermore, many of the dark current management techniques employed with CCD sensors, such as surface pinning, can be introduced as modifications to a standard CMOS process to improve FPN performance [Guidash et al. 1997]. Dark current levels in CMOS sensors can also be minimized by greater attention to process cleanliness as is required for the manufacture of DRAMs. Any advances in fabrication process control will also yield corresponding increases in conversion gain uniformity. Application of such methods should lead to a substantial improvement in the FPN performance of CMOS sensors.

4-14.2.2 Optical Sensitivity and Quantum Efficiency

The optical sensitivity of the CMOS photogate evaluated in this chapter is about a factor of 3 or 4 lower than that of values reported for CMOS photodiode and CCD sensors (Table 4-5). This is due to correspondingly poor quantum efficiency, particularly at short wavelengths (Table 4-14). As the SNR of the sensor is almost completely determined by the number of signal electrons collected, this results in poor SNR performance, particularly for the blue channel of the colour photogate sensor. To attain any substantial improvement in optical sensitivity would require addressing the sensor quantum efficiency at the fabrication process level by reducing the thickness of the polysilicon photogate. While the CMOS photogate is characterized by poor optical performance, the CMOS photodiode achieves optical performance that is competitive with that of CCD sensors. This is because the photodiode pixel is not covered by a thick polysilicon layer and achieves a higher fill-factor than the photogate for given pixel dimensions. However, the disadvantages of the photodiode architecture are lower conversion gain, and the inability to implement "true" CDS to cancel pixel reset noise on-chip.

4-14.2.3 Colorimetric Accuracy

While subjectively pleasing colour rendition has been obtained from the CMOS photogate sensor evaluated in this chapter, the author has been able to show that the colorimetric accuracy of the sensor is limited by poor blue response and significant colour cross talk (Section 4-13.6). To achieve higher colour fidelity would require addressing each of these issues at the fabrication process level. To improve the blue response, greater quantum efficiency is needed at short wavelengths, while cross talk could be reduced by reducing the diffusion length of minority carriers in the substrate through control of the doping concentration and/or introducing channel stops between pixels. As well as increasing the colorimetric accuracy of the sensor, any improvements in each of these areas would enhance the SNR perform-

ance by reducing the magnitude of the off-diagonal coefficients of the colour correction matrix.

4-14.2.4 Charge Transfer Noise and Image Lag

The fundamental problem with the single-poly photogate pixel is the inability to ensure complete charge transfer from the photogate to the floating diffusion node. The author has been able to show that incomplete charge transfer introduces charge transfer noise and image lag that degrade sensor performance (Section 4-9.3). While charge transfer noise can be minimized by suitable timing, it cannot be eliminated from the single-poly photogate pixel. Complete charge transfer can only be guaranteed by using alternative pixel designs such as the double-poly photogate pixel, or developing new pixel architectures.

4-14.3 The Future of CMOS Imaging Technology

The results obtained in this chapter demonstrate that while a sensor suitable for low-end imaging applications can be manufactured in a standard CMOS process, it is not possible to attain performance competitive with that of state-of-the-art CCD sensors. Furthermore, as the feature dimension of CMOS fabrication technology are reduced, the performance of sensors fabricated in standard CMOS is degraded rather than enhanced. This is in agreement with predictions made by others [Wong 1996]. As CMOS technology progresses to deep sub-micron it can be expected that the performance of CMOS sensors will be severely restricted by dark current. It is therefore inevitable that changes must be introduced to a standard CMOS fabrication process to enable the manufacture of competitive image sensors. In addition to greater attention to process cleanliness to minimize leakage, it can be anticipated that alternative pixel designs will be developed. At the circuit level it will be desirable to improve the gain and swing of the read-out architecture.

4-14.3.1 Alternative Pixel Designs

At present two main active pixel designs have been adopted that are compatible with fabrication in standard CMOS, the photogate (Figure 2-14) and the photodiode (Figure 2-18(a)). Each of these pixels has advantages and disadvantages. The photogate pixel provides high conversion gain and supports "true" CDS to cancel reset noise. Both of these features are a result of the separation of the collection site from the floating diffusion node. However, the photogate pixel suffers from poor optical sensitivity and low quantum efficiency due to absorption of photons in the polysilicon photogate. The single-poly photogate pixel is also subject to charge transfer noise and image lag as a consequence of incomplete charge transfer. In comparison the photodiode pixel is characterized by high quantum efficiency but low conversion gain. Furthermore, it does not support "true" CDS to cancel reset noise as the floating diffusion node is also used as the collection site. The active photodiode pixel with transfer gate (Figure 2-18(b))

combines the advantages of both the photogate and photodiode pixels by using a photodiode as the collection site, separated from a small floating diffusion node by a transfer gate. Unfortunately when such pixels are fabricated in a standard CMOS process they are subject to lag and noise due to incomplete charge transfer [Mendis et al. 1997b]. However, with the introduction of a thin $p+$ implant to the fabrication process it is possible to solve this problem by employing a pinned photodiode [Teranishi et al. 1982]. Pinned photodiodes are widely used with interline-transfer CCDs and not only ensure complete charge transfer but also reduce dark current. The introduction of a pinned photodiode is a relatively minor modification to a standard CMOS process and at least one research group is actively pursing this approach [Guidash et al. 1997]. Their pixel design is reproduced in Figure 4-46.

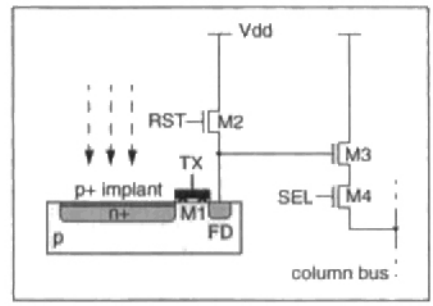


Figure 4-46. Pinned photodiode active pixel with transfer gate [Guidash et al. 1997].

In addition to the pinned photodiode it may be possible to produce other enhanced active pixel designs with minor modifications to a standard CMOS process. One possibility is a double-poly photogate pixel that employs thin polysilicon for increased quantum efficiency, and an additional buried channel implant similar to that used with some frame-transfer CCDs to realize surface pinning for dark current reduction [Bosiers et al. 1995]. With all future pixel designs it will be essential to block the formation of silicide to maximize sensor quantum efficiency. It will also be necessary to carefully design the capacitance of the floating diffusion node to ensure that the sensor conversion gain provides a satisfactory trade-off between good SNR performance (see Eq. (2-27)) and high dynamic range (see Eq. (4-38)).

4-14.3.2 Alternative Read-Out Architectures

At present the dynamic range of CMOS photogate and photodiode sensors is competitive with those of CCD sensors (Table 4-9). However, Eq. (4-38) suggests that this may be difficult to maintain as the supply voltage Vdd is decreased with each new generation of CMOS fabrication technology. Consequently, it will become important to develop alternative sensor read-out architectures that achieve higher gain and signal swing, and have lower read noise. A read-out architecture that achieves a gain much closer to unity than the source follower architecture of Figure 4-1 has already been proposed and will be described in Section 5-4.2 [Loinaz et al. 1998a]. The available signal swing could also be increased by being able to completely

reset the floating diffusion node to Vdd. One simple way to achieve this is to apply a voltage to the gate of the reset device one threshold voltage greater than Vdd, i.e. $Vdd + V_{tn}$ [Wong et al. 1998]. Sensor read noise could be reduced by using a number of parallel output stages as are typically employed with high resolution CCD sensors.

4-14.3.3 Why Pursue CMOS Imaging in Non-Standard Technology?

While it is not possible to manufacture a high performance image sensor in standard CMOS, a strong case can be made for pursing CMOS imaging through the introduction of modifications to a standard CMOS fabrication process. The reasons for developing specialized CMOS imaging technology are based on the fact that the CMOS APS architecture is fundamentally low power and compatible with camera system integration [Wong 1996]. Furthermore, many of the process changes required to increase the performance of CMOS sensors are relatively minor, for example the introduction of a pinned photodiode [Guidash et al. 1997]. This should mean that CMOS sensors with competitive imaging performance can be developed at a modest cost. Once comparable imaging performance has been obtained, the low power dissipation and system integration capability of CMOS imaging technology will challenge the dominance of CCD sensors in many applications, particular portable consumer imaging products. The demonstration of complete camera system integration and related issues form the subject of the next chapter.

CHAPTER 5 An Integrated CMOS Digital Colour Camera

5-1. Introduction

CMOS active pixel sensor technology (APS) has been promoted as an alternative solid-state imaging technology to CCD that is compatible with camera system integration [Fossum 1993]. Increasing the level of integration can provide a substantial reduction in power dissipation, and decrease the physical size and cost of a system. Driving digital signals off-chip rather than analog signals is also advantageous from a noise perspective. However, despite the possibility of realizing a complete camera system on a single chip using a CMOS APS approach, only modest levels of camera system integration have been demonstrated to date, typically the inclusion of an on-chip analog-to-digital converter [Mendis et al. 1993a]. In this chapter an entirely integrated CMOS digital colour camera is described, together with an investigation into camera performance degradation due to the coupling of digital switching noise into analog circuits. As far as the author can ascertain it is one of only two reported true single-chip colour cameras, and the first producing digital video output [Loinaz et al. 1998a, Smith et al. 1998].

A number of significant ideas are incorporated into the architecture of the integrated CMOS digital colour camera, herein known as the single-chip camera, at both the circuit and system level. In the analog portion of the camera these include a new column circuit design, a hierarchical column multiplexer, and a digitally programmable gain amplifier. In the digital portion of the camera programmable architectures for spatial interpolation, colour correction, and the computation of image statistics have been developed. At the system level a sophisticated switching noise management scheme was introduced to quantify sensor performance degradation due to the coupling of digital switching noise into analog circuits through the substrate. The chip architecture was designed to share camera system functionality with software running on a host computer. Camera operations that must be performed at the pixel rate, such as spatial interpolation and colour correction, are supported by on-chip hardware, while

high-level algorithms such as automatic exposure control and white balance are managed by software on the host computer.

In this chapter the architecture and performance of the single-chip camera are described, with emphasis on the camera digital system. Firstly the target application is discussed followed by the specifications and high-level architecture of the camera. The analog modules of the camera are then briefly described before a detailed exposition of the camera digital system. The architecture of the camera digital system is presented and the main issues determining the timing of the camera are discussed, namely the switching noise management strategy, the digital video timing, and the timing of the photogate sensor. The architecture and operation of each of the major digital subsystems are then described, namely the control block, the spatial interpolation subsystem, the colour correction subsystem, and the image statistics subsystem. The host interface is then explained followed by the details of the camera implementation. This chapter concludes with an evaluation of the single-chip camera in terms of the impact of digital switching noise on camera performance, the characteristics of the on-chip photogate sensor, and a discussion of the power dissipation of the various camera subsystems. Finally, conclusions are drawn regarding the future development of CMOS integrated cameras.

5-2. Camera Application

An application that is particularly well suited to CMOS APS technology is that of a low-cost tethered digital multi-media camera.

5-2.1 Digital Multi-Media Cameras

Tethered digital multi-media cameras can be used for desktop video telephony and still-image capture (Section 3-2.3.3). At present digital multi-media cameras based on CCD technology can be purchased as a peripheral for desktop computers as illustrated in Figure 5-1(a) [Connectix]. In the future such cameras may be incorporated into the computer display or chassis as shown in Figure 5-1(b). Present digital multi-media cameras are priced in excess of US $100. However, it has been predicted that if their cost could be reduced below US $50 they would be bundled with the majority of PCs as a standard peripheral [Ackland and Dickinson 1996]. This would create a sizeable new solid-state camera market.

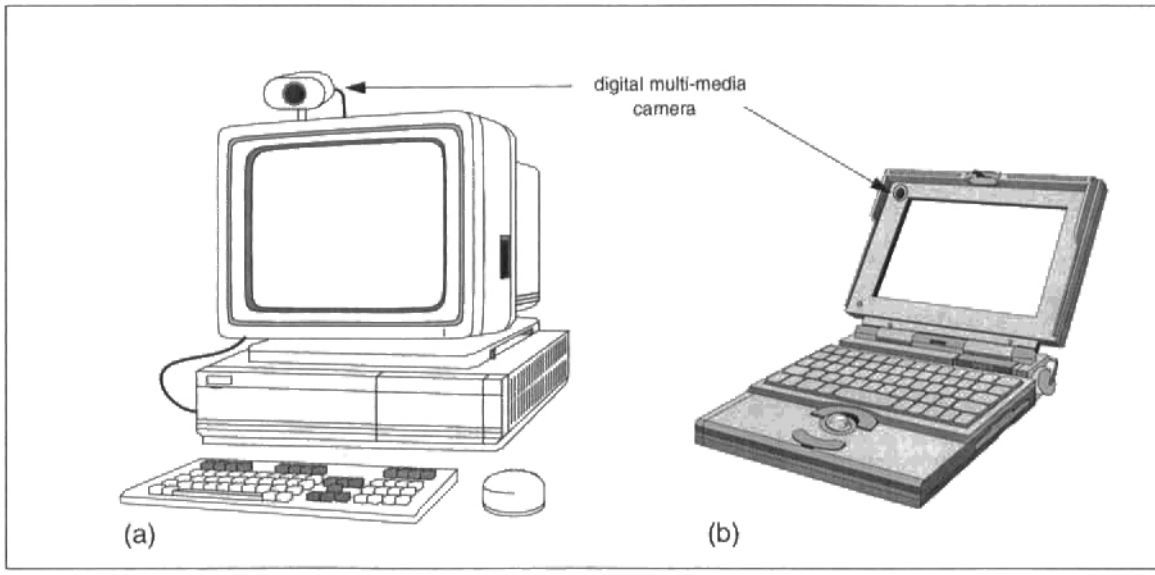


Figure 5-1. Tethered digital cameras for multi-media applications (a) as a peripheral for desktop use or (b) built into the laptop chassis.

The architecture of a digital multi-media camera is shown in Figure 5-2. It consists of an image sensor and associated timing circuits, an analog-to-digital converter (A/D), digital signal processing to perform operations such as spatial interpolation and colour correction, and a bi-directional digital interface to transfer image data to a host computer and receive configuration instructions concerning functions such as image size, exposure level, and white balance.

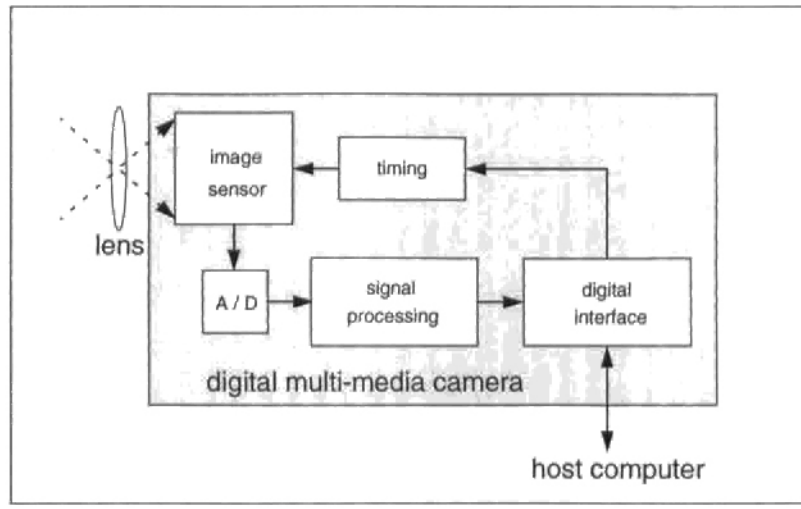


Figure 5-2. Architecture of a digital multi-media camera [Ackland and Dickinson 1996].

5-2.2 The Advantages Of Using CMOS APS Technology

CCD technology is not well suited to the digital multi-media camera application for a number of reasons. CCD sensors typically require high-voltage, high-current clocks and consequently dissipate considerable electrical power, typically between 2W to 25W depending on the sensor resolution and frame rate [Takizawa et al. 1983, Itakura et al. 1995] This is a significant amount of power for a peripheral to draw directly from a host computer. Furthermore, CCD technology does not support camera system integration, and consequently the architecture shown in Figure 5-2 must be realized at the board level using a number of CMOS integrated circuits in addition to a CCD image sensor. This makes it difficult to reduce the parts count and hence the cost and physical dimensions of the camera. CMOS APS technology addresses these issues with the ability to integrate the camera onto a single chip [Ackland and Dickinson 1996]. In addition to the power saving achieved by complete system integration, a CMOS image sensor itself is an inherently low power module when compared to a CCD sensor [Fossum 1994b].

5-2.3 Project Goal - Concept Demonstrator

The purpose of developing the single-chip camera was to demonstrate the integration of a complete digital colour camera system onto a single-chip using CMOS APS technology, and secondly to investigate if this goal can be achieved without loss of image quality due to the coupling of digital switching noise into the analog circuits. As such the focus of the project was on the technical issues involved rather than developing a specific product. This is reflected in the architecture of the camera which was designed with greater emphasis on managing switching noise and supporting a high level of testability, rather that providing advanced functionality that would probably be included in a product. For example, basic functions such as spatial interpolation and colour correction are implemented in the camera, but advanced features such as aperture correction, defect concealment, and electronic zoom are not.

5-3. Camera Specifications and System Architecture

The camera specifications were established from the desired resolution and frame rate. Together with the colour filter array pattern and the core functionality this enabled the camera architecture to be developed. However, the architecture was also determined by the interfacing requirements of the chosen host, a desktop PC. Each of these factors will be discussed in turn before the system level architecture of the single-chip camera is presented.

5-3.1 Camera Resolution and Frame Rate

It was proposed that the single-chip camera produce digital images of CIF resolution at up to 30 frames/second. CIF is a recognized standard for video telephony and has a resolution of 352×288 pixels [ITU 1995].

5-3.2 Colour Filter Array

The primary Bayer checkerboard colour filter array (CFA) pattern shown in Figure 5-3 was selected for the single-chip camera [Bayer 1976]. The checkerboard pattern provides superior horizontal resolution than stripe CFA patterns at the expense of diagonal resolution where the acuity of the eye is poor [Parulski 1985]. A primary CFA was used in preference to a complementary CFA to simplify the subsequent stages of colour processing.

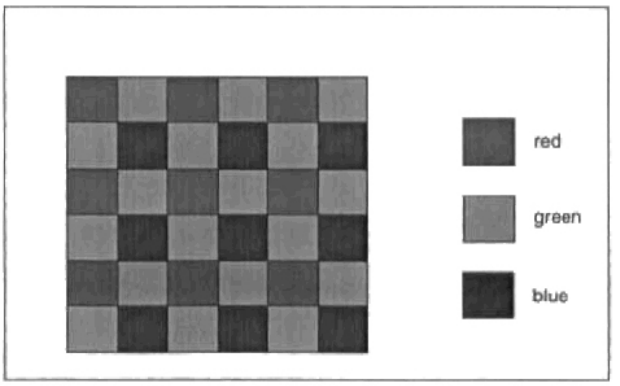


Figure 5-3. Primary Bayer checkerboard colour filter array.

The design of optimal colour filter transmission characteristics for solid-state image sensors is a complex procedure [Engelhardt and Seitz 1993, Vrhel and Trussell 1995]. For low-cost consumer applications such as the digital multi-media camera it is not practical to manufacture a colour filter array with custom designed transmission characteristics. For this reason a set of colour filters was selected from a range supplied by a manufacturer, similar to those used with the photogate sensor in Chapter 4 (Section 4-2.5). A global colour compensating filter was employed to suppress infrared. The optical transmission characteristics of the colour filter array and colour compensating filter are shown in Figure 5-4.

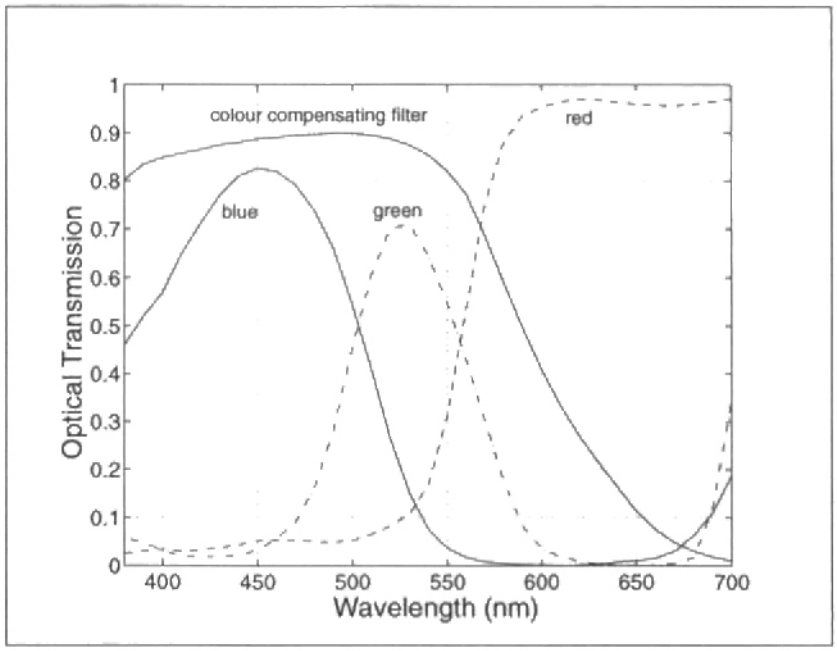


Figure 5-4. Optical transmission characteristics of the colour filter array and global CM-500M colour compensating filter.

5-3.3 The Host Architecture

5-3.3.1 Acquiring, Displaying, and Encoding Digital Image Data

At present standard desktop computers do not contain hardware support for digital video or video telephony. This presents a number of problems for a host computer in terms of acquiring the image data from the single-chip camera, displaying it, and compressing and encoding it for transmission across the public switched telephone network (PSTN). Furthermore, differences in the colour spaces required for image display and compression also introduce difficulties. To display high quality colour images computers represent image data in display memory using a 24-bit *RGB* format where 8-bits are used to represent the red, green, and blue tristimulus value of each pixel [Hall 1989]. However, image compression techniques that deliver substantial compression gain, such as JPEG or MPEG, require a $Y'C_BC_R$ colour difference format [Netravali and Haskell 1988]. Currently the only standard PC interfaces available for data acquisition are the serial and parallel ports. If the camera is assumed to produce 24-bit *RGB* image data, then at CIF resolution and 30 frames/second this yields a data rate greater than 72-Mbits/second. This is far in excess of either the serial or parallel port bandwidth. While several new interface standards such as the Universal Serial Bus (USB) and IEEE Standard 1394 (Firewire) have been proposed they are not yet established [USB, Firewire]. If the camera was to perform image compression to significantly reduce the data rate, it would need to be based on $Y'C_BC_R$ colour difference encoded pixel values. To display the images from the camera the host would

then need to transform the data from $Y'C_BC_R$ to 24-bit *RGB*. At CIF resolution and 30 frames/second this requires dedicated hardware. It was therefore inevitable that the host would require additional non-standard hardware to acquire and display image data from the camera. To support video telephony the host would also need dedicated hardware. This is because compressing and encoding video of CIF resolution at any significant frame rate requires a substantial hardware commitment as the bandwidth of PSTN is relatively low [AVP 1995]. As the focus of the project was on demonstrating camera system integration and investigating digital switching noise, the application of the single-chip camera to video telephony was not actively pursued.

5-3.3.2 The Host Interface

It is clear from this discussion that at present it is not possible to interface a digital camera of CIF resolution to a PC at 30 frames/second through a standard I/O port. Therefore it was decided to employ a specialized PC interface in the form of a digital framegrabber, and use a 24-bit *RGB* format for the image data produced by the single-chip camera. A Matrox digital framegrabber was installed in the host PC to support the acquisition of image data in 24-bit *RGB* format at up to 30 frames/second. The framegrabber also contained video memory to enable the display of the image data at the acquisition rate with full 24-bit colour. Using a 24-bit *RGB* image data format simplified the architecture of the single-chip camera as no conversion to $Y'C_BC_R$ was needed. Furthermore, as the framegrabber could meet the resolution and frame rate requirements, no on-chip compression was necessary. It is likely that both of these benefits will not be available to future generations of digital multi-media cameras that will need to target new standard I/O interfaces as they are established. However, for the purposes of demonstrating camera system integration and investigating digital switching noise, opting for the simplest I/O requirements for the single-chip camera was convenient, and did not affect the general validity of the camera performance results obtained.

5-3.3.3 Realizing Camera Functionality on the Host

In addition to the host acquiring and displaying image data from the camera, it was proposed that a number of high-level, low-speed tasks required by the camera be performed in software on the host. Algorithms for automatic exposure control and white balance typically change camera parameters at much less than the frame rate, but the algorithms themselves are often quite complex [Morimura et al. 1990, Liu et al. 1995]. Therefore it would be advantageous to realize the automatic exposure control and white balance algorithms in software on the host to simplify the architecture of the single-chip camera. However, both exposure control and white balance algorithms are usually based on metrics determined from image statistics in each frame whose calculation requires significant arithmetic at the pixel rate. Consequently, to enable the exposure control and white balance algorithms to be realized in software on the

host, it was decided to include dedicated hardware on the single-chip camera to compute the necessary image statistics for each frame. A low-speed interface could then be used to upload these statistics to the host where the exposure control and white balance software could determine new parameters to be downloaded to the single-chip camera to adjust the sensor exposure and white balance. Furthermore, to provide the greatest flexibility in testing and operating the camera it was decided to allow the host to modify the coefficients and configuration registers of all on-chip systems, not just those associated with exposure control and white balance. For this reason a separate low-bandwidth digital I/O board was installed in the host to support bi-directional parameter exchange.

5-3.4 Camera Architecture

The architecture of the single-chip camera contains both analog and digital modules and a top-level block diagram is shown in Figure 5-5. The target fabrication process for the single-chip camera was a non-silicided, single-poly, double-metal Lucent Technologies 0.8μm CMOS process, the same process used to produce the photogate sensor of Chapter 4.

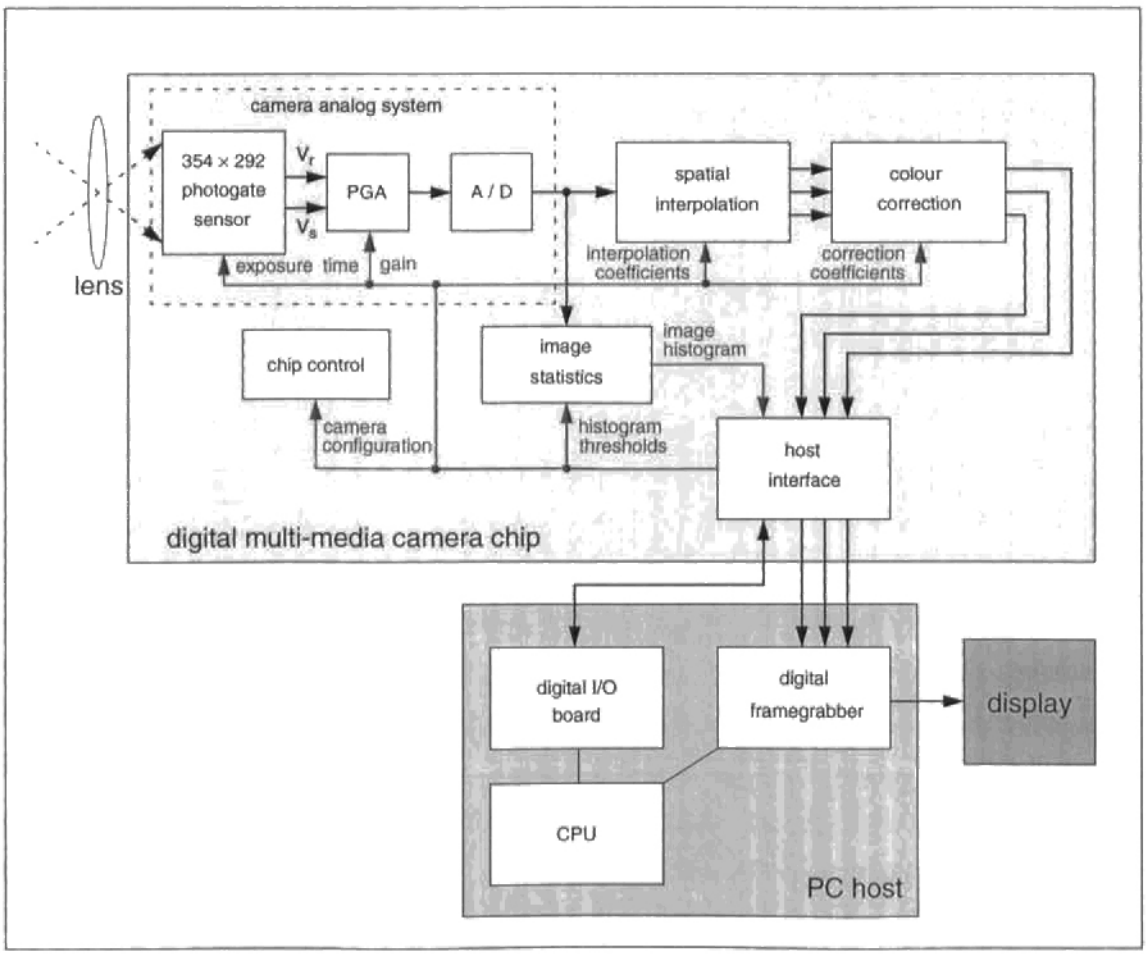


Figure 5-5. Camera system architecture.

5-3.4.1 Camera Analog System

The camera analog system consists of a photogate image sensor, a programmable gain amplifier (PGA), and an analog-to-digital converter (A/D). The PGA performs two levels of correlated-double sampling (CDS) to suppress pixel and column fixed-pattern noise (FPN). Furthermore, it provides a gain to the corrected pixel values that can be varied to control sensor exposure and white balance. The A/D digitizes the pixel values output from the PGA. The camera analog system will be described in Section 5-4.

5-3.4.2 Camera Digital System

The camera digital system performs the processing necessary to generate 24-bit *RGB* image data from the raw digitized pixel values supplied by the A/D. The minimum requirements to achieve this goal are spatial interpolation and colour correction. In principle, gamma correction should also be applied by the camera. However, to reduce the development time for the camera it was omitted, and instead implemented by the digital framegrabber in the host. The camera digital system also provides hardware to compute image statistics used by the automatic exposure control and white balance algorithms, and digital logic to control the timing and configuration of the analog and digital modules. A host interface is used to export image data from the camera and to support parameter exchange with the host. The camera digital system is described in Section 5-5.

5-4. Camera Analog System

The camera analog system consists of the photogate sensor, the PGA, and the A/D. The design and full-custom layout of the photogate sensor and the PGA were performed by Marc Loinaz of Bell Laboratories. The A/D was designed by Kamran Azadet, also of Bell Laboratories. While the architecture of the camera analog system does not contain any contributions from the author, a brief description of the camera analog system is included as it necessarily influenced the design of the camera digital system.

5-4.1 Active Pixel Sensor Photogate Array

The image sensor used in the single-chip camera was a CMOS APS photogate array of dimensions 354×292. While CIF resolution is 352×288 pixels, two extra rows and columns were included to simplify the spatial interpolation hardware. Furthermore, additional rows were placed at the top and bottom of the array and covered with an opaque material during the deposition of the colour filter array. These 'black rows' can be used to determine the dark level of the sensor array so that it can be subtracted from the image data by the programmable gain

amplifier. The format of the sensor array is shown in Figure 5-6. The addresses of the black rows were chosen to simplify the control hardware.

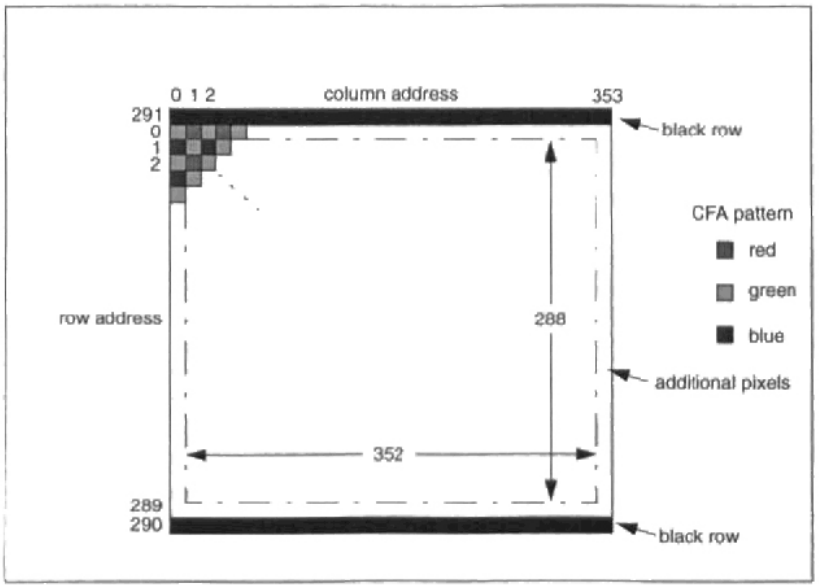


Figure 5-6. Sensor array format.

The photogate pixel design used in the single-chip camera was a scaled version of the pixel employed by the photogate sensor of Chapter 4 (Figure 4-4). For the single-chip camera the pixel dimensions were 18.0μm × 18.0μm, and a drawn pixel fill factor of 35% was realized.

5-4.2 Column Circuit Design

To improve the gain of sensor read-out, a new column circuit design was developed by Loinaz and is shown in Figure 5-7. This column circuit design has several improved features when compared to the column architectures previously employed with photogate and photodiode active pixel sensors as given in Figure 2-15 and Figure 2-19 respectively. Rather than forming part of a distributed source follower, the pixel devices *M3* and *M4* comprise part of a distributed unity-gain amplifier with devices *M5-M8*. Transistors *M3* and *M7* form a differential pair with triode devices *M4* and *M6*. These four devices, together with the current sources *M5* and *M8*, realize an operational transconductance amplifier (OTA) that is connected in unity-gain feedback so that the voltage at *pout* is a buffered version of the voltage at the pixel floating diffusion node *FD*.

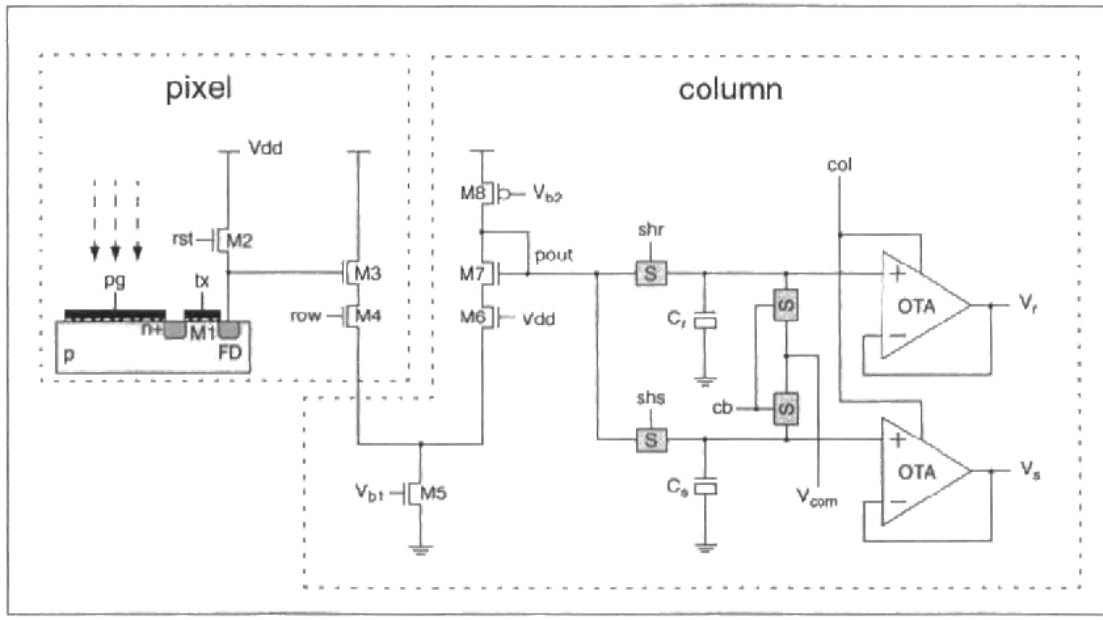


Figure 5-7. Pixel and column architecture of the photogate sensor. The components labelled 'S' are CMOS switches.The components labelled OTA are amplifiers whose schematic is given in Figure 5-8.

The *p*-type source followers used in Figure 2-15 and Figure 2-19 have also been replaced by OTA circuits connected in unity-gain feedback. The schematic for this OTA design is given in Figure 5-8.

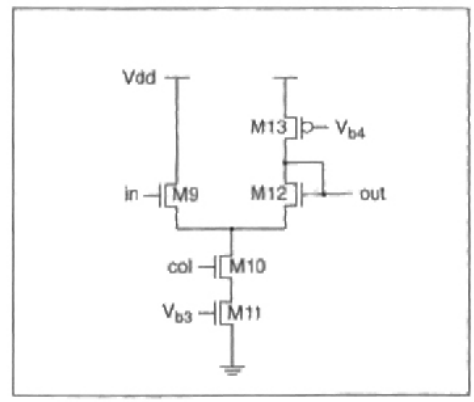


Figure 5-8. Schematic for the operational transconductance amplifier (OTA) used in the column circuit shown in Figure 5-7.

5-4.2.1 Advantages and Disadvantages of the New Column Circuit Architecture

The advantage of using unity-gain amplifiers instead of the established source follower architecture is that a combined gain very close to 1 can be achieved. Improving the gain of the read-out architecture increases the conversion gain referred to the sensor output (see (2-9)), and minimizes the contribution of the read noise to the sensor noise floor (see (4-38)). Simula-

tions of the source follower architecture yield a maximum combined gain through the read-out path of about 0.7, the corresponding simulation for the unity-gain amplifier column read-out architecture yields a gain greater than 0.9. However, the read noise of the unity-gain circuit will be slightly higher than that of the source follower architecture as there are more transistors in the signal path.

5-4.2.2 Column Circuit Timing

The timing of the new column architecture is virtually the same as that used with the source follower architecture. During integration the polysilicon photogate *pg* is held at *Vdd* and photon generated electrons are collected in the potential well beneath the gate. The transfer device *M1* is DC biased at $0.6V$ to isolate the collected charge under the photogate from the floating diffusion node *FD*. For sensor read-out each row is addressed in turn with the row decoding logic (not shown in Figure 5-7) driving the appropriate line *row* to *Vdd*. The *FD* nodes of the pixels in the row are reset to a voltage approximately one threshold voltage drop below *Vdd* by pulsing *rst*. The reset operation introduces uncertainty into the *FD* reset level due to thermal noise and the threshold voltage drop across *M2*. The reset level is buffered by the unity-gain feedback amplifier formed by devices *M3-M8* and is sampled on the gate capacitance C_r by pulsing *shr*. Electrons collected under the photogate are then transferred to the *FD* node via device *M1* by pulsing *pg* to ground. The signal electrons displace the *FD* voltage and this level is sampled on the gate capacitance C_s by pulsing *shs*. The sampling of the pixel reset and signal levels by the column circuits is carried out in parallel for each pixel in the selected row. This occurs in the line blanking period of the video signal. To generate the image signal each column of the sensor is then addressed in turn by the column decoding logic (not shown in Figure 5-7) by driving the *col* signal to *Vdd*. The column OTA circuits buffer the sampled reset and signal levels onto buses denoted V_r and V_s respectively. Two levels of correlated-double sampling (CDS) are then performed in conjunction with the PGA in a manner similar to that described in Section 2-4.1.3. During read-out the voltage levels on V_r and V_s are subtracted by the first stage of the PGA to remove reset noise and pixel offset mismatch. This signal level is sampled and held internally by the PGA. The *cb* signal is driven high as part of the second level of CDS to short the inputs of the column OTA circuits to a common DC voltage V_{com}. The first stage of the PGA forms the offset difference of the column OTA circuits which is then subtracted from the sampled signal level. This enables a final signal to be delivered to the A/D that has pixel and column offset variations cancelled.

5-4.3 Hierarchical Column Multiplexer

In the APS column read-out architectures of Figure 2-15 and Figure 2-19, the buses V_r and V_s are common to the entire array [Mendis et al. 1994a]. The capacitance seen by the column source followers is the combined output capacitance of all the other column source followers

in the sensor, and the capacitance of the interconnect running the full width of the array. While this results in a uniform capacitance seen by each column circuit, the total capacitance can be quite significant for a large array and must be driven at twice the pixel rate for sensor operation with two levels of CDS. It is possible to reduce the capacitance seen by each column circuit using hierarchical multiplexing techniques, such as those employed with column decoders for SRAMs [Weste and Eshraghian 1985]. A hierarchical column multiplexer was developed by Loinaz and is shown in Figure 5-9. In this scheme the final unity-gain amplifier in the column circuit has to drive only the output capacitance of seven other such amplifiers, plus the parasitic capacitances associated with two "on" CMOS switches and twelve "off" switches, and a smaller interconnect capacitance. While the hierarchical multiplexer may result in capacitive load variations for different column circuits, the column buffers were designed for 0.1% settling to minimize fixed-pattern noise. The hierarchical multiplexer reduces the load capacitance of the column circuit by more than an order of magnitude. This improves the power/read-out speed trade-off, and facilitates the power efficient design of larger image sensors.

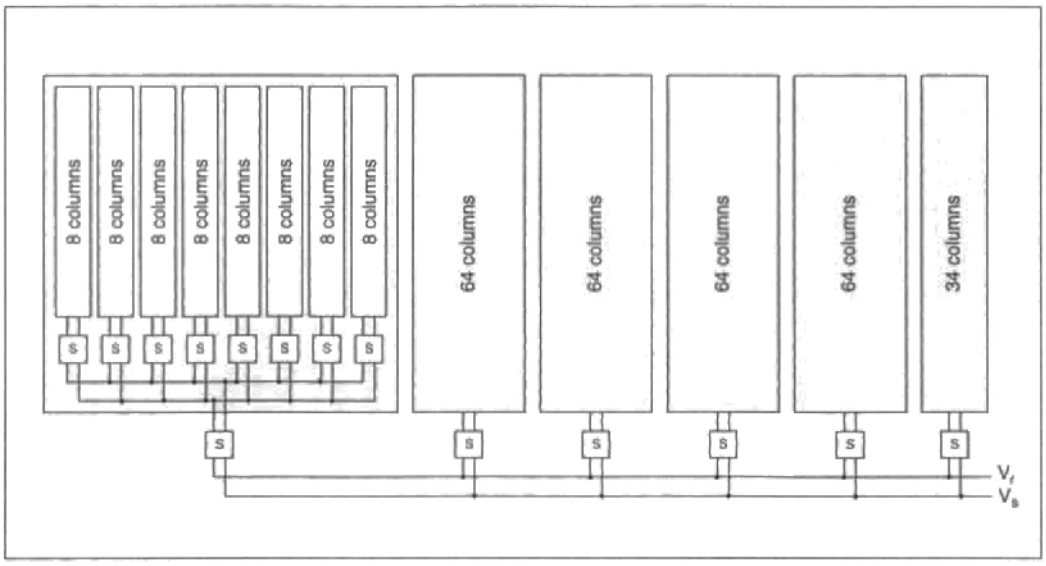


Figure 5-9. Hierarchical column multiplexer. The components labelled 'S' are pairs of CMOS switches.

5-4.4 Programmable Gain Amplifier

The programmable gain amplifier (PGA) used in the single-chip camera was designed by Loinaz and performs two levels of correlated-double sampling to suppress pixel and column FPN. The PGA also features a feedback circuit to subtract the sensor black offset determined from the two black rows of the array. The PGA was implemented using a two stage switched capacitor architecture. A fully differential design was employed to reject supply noise. A simplified schematic of the PGA is shown in Figure 5-10.

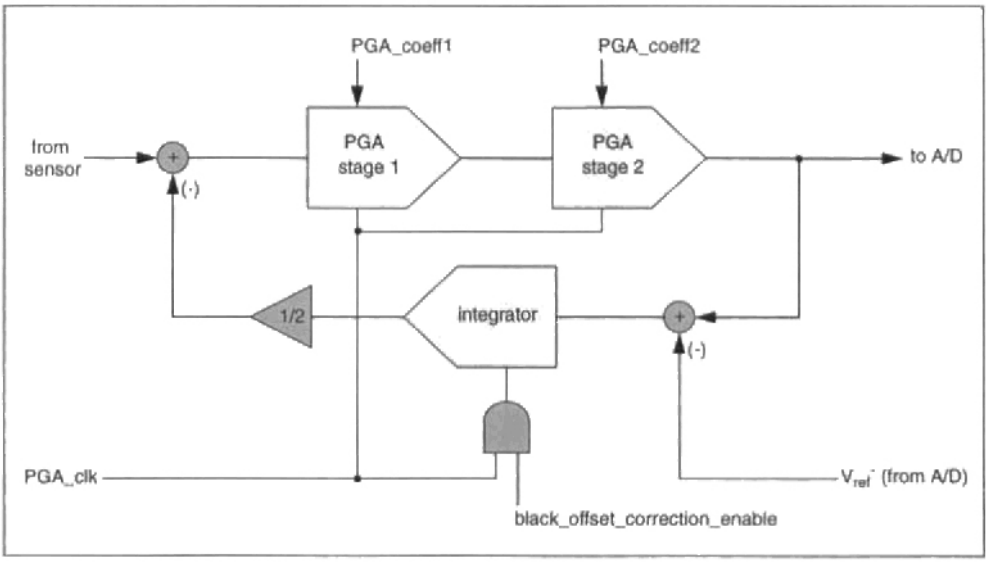


Figure 5-10. Architecture of the programmable gain amplifier (PGA). For a complete schematic that describes the differential nature of the PGA see [Loinaz et al. 1998a].

The PGA gain is digitally programmable to control sensor exposure and white balance. The gain of each stage of the PGA can be programmed to take on one of the values listed in Table 5-1 and the total gain that can be provided by the PGA ranges between 1 and 64.

PGA coefficient	Gain
000	1
001	8/7
010	8/6
011	8/5
100	2
101	8/3
110	4
111	8

Table 5-1. Values of gain provided by each PGA stage.

To achieve sensor white balance it is necessary to be able to apply different values of gain to the red, green, and blue pixel values. To support this objective the camera digital system provides a programmable coefficient store to hold gain control words for both stages of the PGA for each of the colours red, green, and blue. A state machine in the camera system control selects the appropriate gain values for the PGA based on whether the current pixel colour is red, green, or blue. The programming details of the PGA coefficients are given in Table C-3.

5-4.5 Analog-to-Digital Converter

The analog-to-digital (A/D) converter used in the single-chip camera employs an 8-bit flash architecture and can produce 3 Msamples/second. A simplified schematic of the A/D architecture is shown in Figure 5-11. Gray coding was employed to suppress errors produced by sparkles and metastability [Razavi 1995]. Furthermore, it is possible to exploit the video line blanking intervals to calibrate the comparators of the A/D prior to the read-out of each row of the image sensor. This allows comparator offset cancellation to improve A/D accuracy.

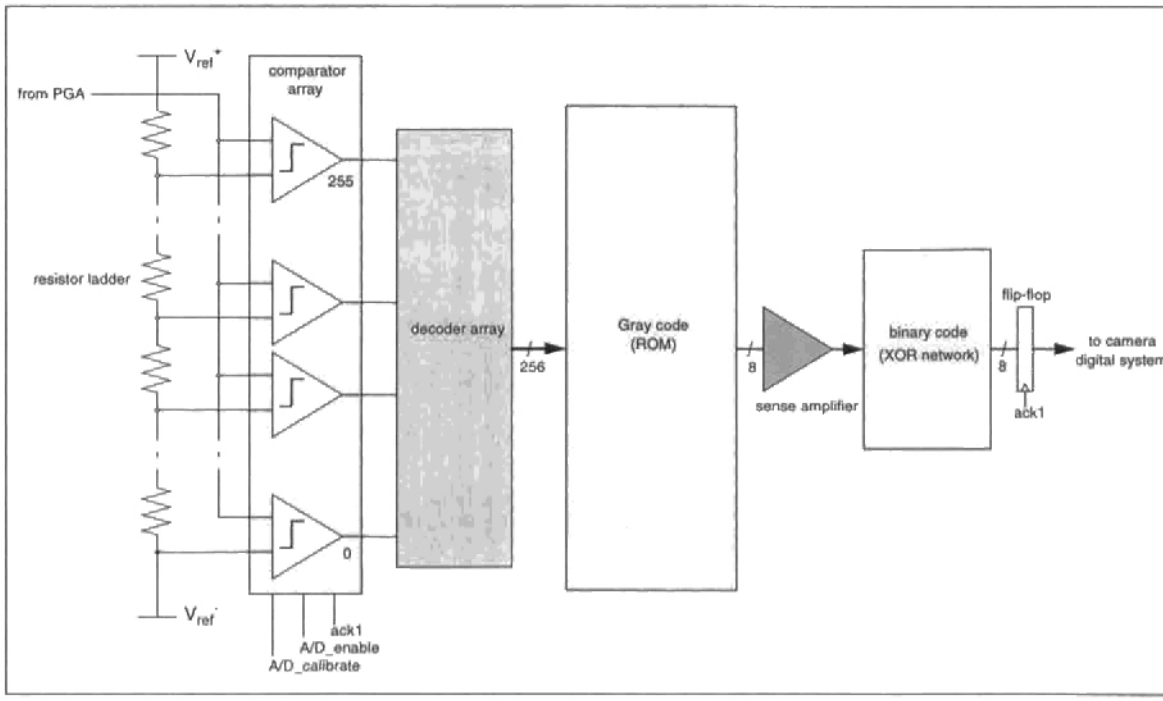


Figure 5-11. Analog-to-digital converter architecture.

This particular A/D design was used in the single-chip camera due to its ready availability in the target technology, not because it had been optimized for the single-chip camera in terms of speed, area, and power. Furthermore, the A/D input is single-ended and therefore more susceptible to noise on its input than fully differential A/D architectures. However, the most fundamental limitation of the A/D employed by the single-chip camera is that it is only 8-bit. An 8-bit A/D can be considered the minimum requirement to produce 24-bit *RGB* image data and in most digital cameras a 10 or 12-bit A/D is used instead [Wang et al. 1994, Zen et al. 1994, Chan and Youe 1995]. The reason for this is that in a given scene, the dynamic range defined as the greatest contrast ratio may be well in excess of 256. Furthermore, when applying gamma correction quantization errors are invariably introduced. If an accurate 8-bit result is desired after gamma correction then greater than 8-bit precision should be available prior to its application. The few cameras that do employ an 8-bit A/D compress the signal in a non-linear fashion prior to digitization to address this issue [Parulski and Jameson 1996].

5-5. Camera Digital System

The architecture of the camera digital system is described in a top-down fashion, in largely the order it was developed. This section is concerned with high-level issues such as the top-level architecture, testability, the host and video interfaces, and the management of digital switching noise. The digital video timing and photogate sensor timing is also presented. All the digital systems of the single-chip camera were designed by the author, with the exception of the colour correction and image statistics subsystems which were developed jointly with K. J. Singh of Bell Laboratories. A complete bit-accurate, clock-accurate description of the camera digital system was produced at the register transfer level using the Very high speed integrated circuit Hardware Description Language (VHDL). A synthesizable VHDL coding style was employed. The exception to this was the full-custom SRAM used as part of the interpolation subsystem which was designed by Jay O'Neil of Bell Laboratories. The synthesis of the VHDL model of the camera digital system to a gate level description was performed by K. J. Singh. M. Zalonis, J. Bauman, and M. Hrubik, all of Bell Laboratories, provided assistance with chip assembly. As the camera digital system was synthesized from VHDL, all the schematics and block diagrams that will be presented must be considered functional only, they do not provide information regarding physical implementation.

5-5.1 Camera Digital System Architecture

A block diagram of the camera digital system architecture is shown in Figure 5-12 and will be used to discuss a number of interfacing and testing issues. A detailed description of the camera control, interpolation, colour correction, and image statistics subsystems are deferred until Section 5-6, Section 5-7, Section 5-8, and Section 5-9 respectively.

5-5.1.1 Digital Video Interface

The camera digital system was required to produce 24-bit *RGB* colour images at up to 30 frames/second. A parallel interface for the digital video data was employed consisting of three 8-bit buses denoted *r_ch*, *g_ch*, and *b_ch* for the red, green, and blue components respectively. A pixel clock *pck* (not shown in Figure 5-12) generated by the camera was defined to synchronize the image data for the framegrabber in the host. To delimit each frame and line of digital video data it was also necessary to provide vertical and horizontal synchronization pulses [Poynton 1996]. For this purpose the *frame_enable* and *line_enable* signals were specified. As an additional feature, the *frame_active* and *line_active* signals were created to define a programmable region-of-interest in the output image. The digital video timing will be discussed in more detail in Section 5-5.3.

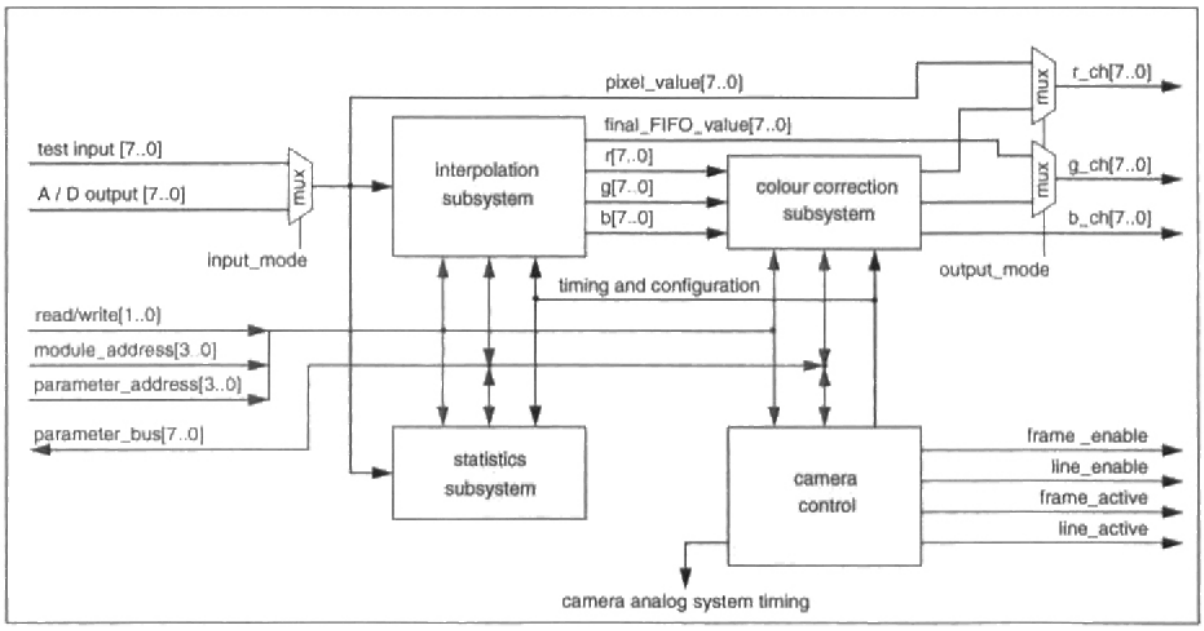


Figure 5-12. Camera digital system architecture.

5-5.1.2 Host Interface Model

A host interface was required by the camera to support parameter exchange with the host computer. A simple RAM-style model was employed with camera parameters stored in a series of registers, and an 8-bit bi-directional data bus known as the *parameter_bus* provided for parameter exchange. To simplify the host interface parameters are stored locally in each of the camera modules, and can be addressed using the *module_address* and *parameter_address* lines. In this sense the host interface does not exist as a distinct entity like the interpolation or colour correction subsystems, and is instead distributed throughout the camera digital system. A *read/write* line was provided to enable the host to select a parameter read, write, or no I/O operation. To prevent "glitches" all parameters are double-buffered. The host interface will be discussed in more detail in Section 5-10.

5-5.1.3 Design for Testability

With any large complex system it is desirable to be able to test the functionality of each module individually. While this goal was not fully realized for the single-chip camera, a significant number of test features were incorporated into the architecture. To test the camera digital system a multiplexer was provided to select the input to the digital system from either the pixel values generated by the on-chip A/D, or test vectors provided externally. A number of multiplexers were also provided at the system level, and internal to the colour correction system (see Figure 5-37), to allow intermediate results to be output from the camera for testing purposes. Output modes supported include pixel data from the A/D, pixel data after spatial interpolation, and pixel data after colour correction. The interpolation subsystem includes a FIFO imple-

mented as an SRAM (see Figure 5-31 and Figure 5-32). To enable the data flow in the interpolation subsystem and the functionality of the SRAM to be verified, the A/D test mode is also configured to place the last value of the FIFO into one of the output channels. The camera input and output modes are determined by the contents of the *camera_configuration_word* register. The camera configuration word can be programmed by the host and is described in Table C-2.

5-5.2 Switching Noise Management

The single-chip camera comprises both analog and digital subsystems. It has been shown that for mixed-signal integrated circuits, fast switching transients produced by digital logic can couple into analog components, thereby limiting the precision that can be achieved [Su et al. 1993]. An important part of the design of the single-chip camera was to develop a strategy for minimizing camera performance degradation due to the coupling of digital switching noise into analog circuits such as the sensor pixel and column circuits, the A/D, and the PGA. Furthermore, it was desirable to be able to quantify the effectiveness of the switching noise management scheme.

5-5.2.1 Direct Coupling of Switching Noise

Digital transients can produce switching noise in other circuits on the same die through both direct capacitive coupling, and interaction via the substrate. Direct capacitive coupling can be minimized by suitable physical separation of the analog and digital components and associated interconnects and supplies. However, coupling through the substrate is more difficult to manage.

5-5.2.2 Coupling of Switching Noise via the Substrate

Present standard CMOS technologies employ a substrate comprised of a lightly doped epitaxial layer grown on a heavily doped bulk substrate in order to minimize latch-up. This is illustrated in Figure 5-13(a) where a cross section of the CMOS structures are given. By design the heavily doped bulk is effectively a single electrical node, as shown by the circuit representation of Figure 5-13(b). While a heavily doped bulk substrate is advantageous for minimizing latch-up, it has important implications for the coupling of switching noise. Experimental investigation and device simulations indicate that switching noise reaching the heavily doped bulk substrate spreads throughout the entire chip [Su et al. 1993]. If analog and digital circuits are separated by four times the effective thickness of the epitaxial layer, direct capacitive coupling is minimal and crosstalk between digital and analog circuit blocks occurs primarily by way of the heavily doped bulk. Any further increase in the physical separation will not reduce crosstalk. This represents the limit of switching noise reduction that can be achieved at the circuit or layout level.

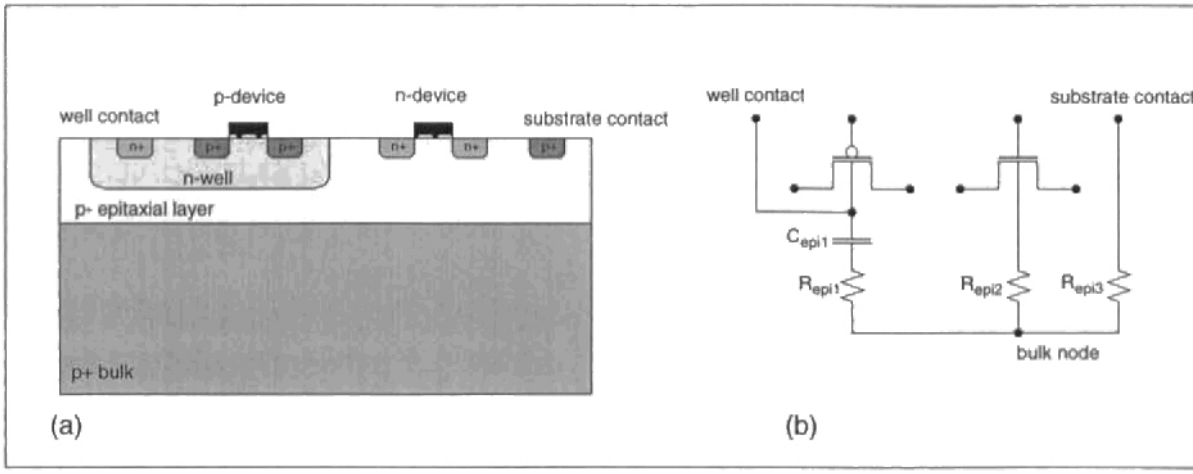


Figure 5-13. (a) Cross section and (b) circuit representation of CMOS structures on a heavily doped substrate.

5-5.2.3 Temporal Sequencing to Reduce Switching Noise

In mixed-signal projects it has been shown that the influence of switching noise can be reduced at the system timing level [Blalack and Wooley 1995, Mayes and Chin 1996]. It has been demonstrated that sampling operations in analog circuits are most sensitive to switching transients in the time period surrounding the sampling operation, the most critical time being immediately prior to sampling. This suggests a strategy to reduce analog performance degradation due to the coupling of digital transients through the substrate is to temporally separate analog and digital operations as illustrated in Figure 5-14. The introduction of "quiet" periods allows digital transients in the substrate sufficient time to decay, and hence minimizes their impact on analog sampling operations. For the example cited, a 10 dB improvement in the signal-to-noise ratio was achieved using such a switching noise management scheme [Blalack and Wooley 1995].

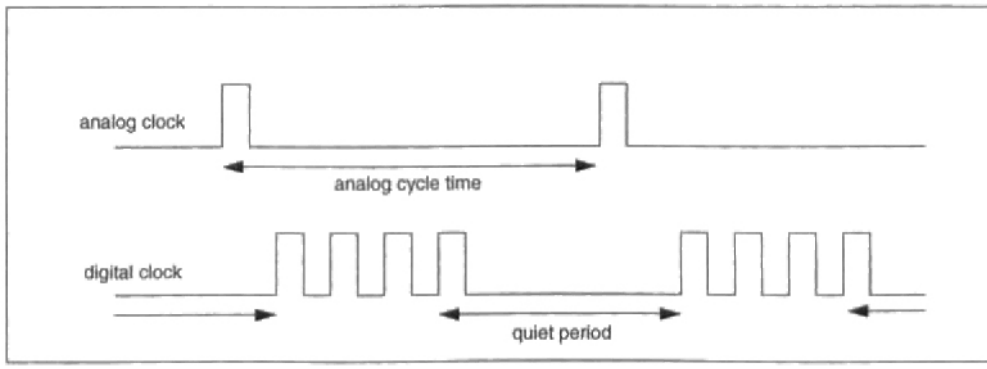


Figure 5-14. Temporal sequencing with "quiet periods" to reduce the coupling of digital switching transients into analog sampling operations.

However, the introduction of quiet periods does have a number of implications for system design. For a given analog cycle time the effective speed of the digital clock must be increased. Furthermore, the implementation of the digital clock involves what is known as "gating the clock". This is a non-standard practice in digital logic design and can pose difficulties with circuit synthesis, simulation, and verification tools. Despite these potential problems the author decided to define quiet periods in the single-chip camera timing, the first time such a switching noise management scheme has been used with an image sensor.

5-5.2.4 Camera System Clocks

A number of different clocks are required by various camera subsystems in addition to the pixel clock *pck*. Many of the digital processing steps, such as spatial interpolation and colour correction, require a significant number of operations to be performed for each pixel value. As the *pck* rate is only $3.39MHz$, a faster clock is possible for the digital system. The most complex operation performed by the single-chip camera is that of spatial interpolation. It will be shown in Section 5-7 that an efficient implementation of the interpolation algorithm chosen is possible using 6 digital or *dck* clock cycles for every *pck* cycle. The camera analog modules also have specific clocking requirements. The A/D must be clocked every pixel cycle and the PGA needs two non-overlapping clock pulses each pixel cycle. In terms of sensitivity to digital switching noise it was predicted that the A/D might be the more vulnerable of the two modules, as it was single-ended and not fully differential. For this reason camera clock definitions were developed so as to ensure that the A/D clock signals occurred in quiet periods relative to *dck* and *pck*. Two clocks *ack1* and *ack2* were generated for the A/D. In the present implementation of the single-chip camera, the 8-bit flash A/D only required a single pulse, *ack1*. The second A/D clock pulse *ack2* was supplied to allow a higher resolution pipeline A/D to be used with the camera, either at the board level with the current camera for testing purposes, or on-chip in future camera designs. As the PGA required two non-overlapping clock pulses it would have introduced substantial timing complexity to introduce quiet periods for PGA operation. For this reason no quiet periods were provided for the PGA. The camera system clock definitions are shown in Figure 5-15. A master or fast clock *fck* is used by a clock generator to produce the other system clocks. Each *pck* cycle consists of nine *fck* cycles. For a *pck* rate of $3.39MHz$ the corresponding *fck* rate is $30.5MHz$.

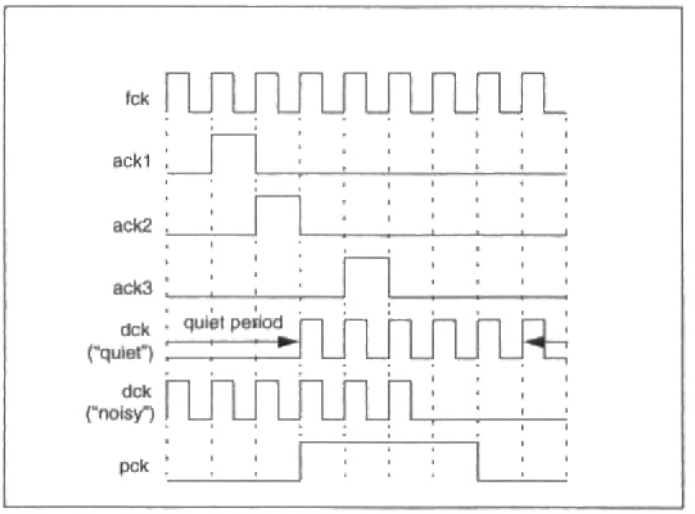


Figure 5-15. Camera system clock definitions.

5-5.2.5 "Quiet" and "Noisy" Operation

To enable the effectiveness of the switching noise management strategy to be quantified, the camera supports both a "quiet" and "noisy" mode of operation. This is achieved by altering the phase relationship of the 6 cycle *dck* with respect to the other system clocks as shown in Figure 5-15. A bit can be set in the *camera_configuration_word* to select either noisy or quiet operation (Table C-2). All the digital logic on the camera chip is positive edge triggered and clocked by either *dck* or *pck*. In quiet mode, two complete *fck* cycles are available from the final positive edge in the *dck* pulse train until the positive edge of *ack1* for switching transients in the substrate produced by *dck* to decay. From the positive edge of *pck* seven *fck* cycles are available for transients associated with *pck* to decay. However, in noisy mode the positive edge of *ack1* is coincident with a positive edge of *dck*. For correct camera system operation it is necessary to be able to transfer a number of data values from modules clocked by *pck* to subsystems clocked by *dck*, independent of whether the camera is in quiet or noisy mode. An additional signal *ack3* is provided to clock the registers used for this purpose.

To minimize the impact of digital switching noise on the sampling operations performed by the sensor column circuits during the video line blanking interval, a quiet period was defined in this interval. During the line blanking interval all clocks except for *pck* and *fck* are suppressed. A signal called *quiet/noisy_I/O* is also taken low during this interval to inform the host that it should temporarily suspend parameter I/O transfers on *pck* for quiet operation. By supporting both quiet and noisy modes of operation at the line and pixel clock level, the architecture of the single-chip camera enabled the effectiveness of this switching noise management strategy to be quantified.

5-5.2.6 Supply Bounce Sensors

In order to monitor the effects of digital switching noise a pair of supply bounce sensors was included in the camera architecture. As is customary for mixed-signal integrated circuits, separate supplies were used for the analog and digital subsystems. However, the negative supplies were shorted together through the substrate and could not be separated. This was because the standard cells employed in the digital subsystem incorporate substrate contacts connected to the negative supply. To enable the "bounce" of the on-chip analog supply $AVdd$ to be measured, a p-type transistor was connected between $AVdd$ and the chip ground Vss as shown in Figure 5-16. A similar circuit was provided to measure the bounce of the on-chip digital supply $DVdd$. When the output of each supply bounce sensor is connected to the 50Ω input of an oscilloscope a common source amplifier is formed. By varying the supply voltage the gain of the amplifier can be determined. During camera operation the supply bounce can be measured by dividing amplitude of the trace on the oscilloscope by the gain of the supply bounce sensor. As the substrate is electrically connected to the chip ground Vss, each supply bounce sensor measures the total voltage fluctuation between the corresponding supply and the substrate. Therefore, the supply bounce waveforms produced by such sensors will monitor switching noise injected into the chip substrate in addition to noise introduced to the supply voltages.

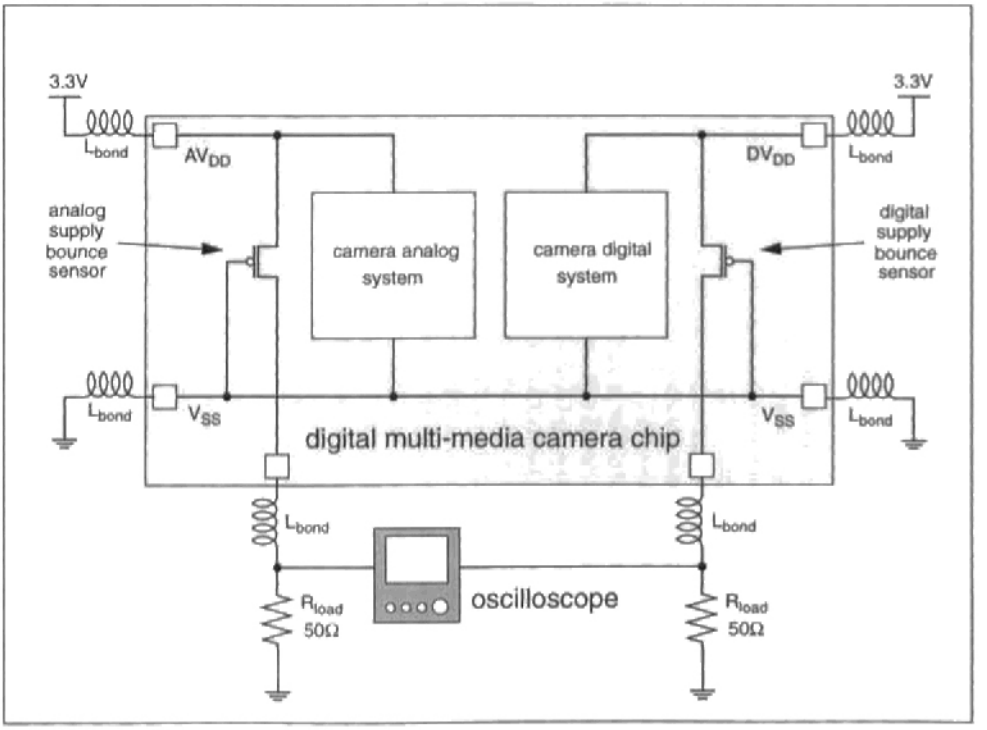


Figure 5-16. Analog and digital supply bounce sensors.

5-5.3 Digital Video Timing

A video format was defined by the author consistent with the timing requirements of the host framegrabber and read-out of the photogate sensor. To enable pixel values from the entire image sensor to be acquired for testing purposes, the digital video format was based on the full sensor dimensions of 354 × 292, rather that the CIF resolution of 352 × 288.

5-5.3.1 Video Frame Timing

Each line of video was defined as 382 *pck* cycles as will be described in the next subsection. The *frame_enable* signal is generated by the camera to delimit each frame of digital video data. Three line periods after the negative transition of *frame_enable,* 292 lines of video data are output from the camera. The duration of the "front porch" of the *frame_enable* signal is programmable and set by a 16-bit parameter to a value between 1 and 65536 video line periods. This allows the frame rate and sensor array integration period to be varied without changing the camera clock frequency or the sensor array read-out rate. This is useful for testing purposes. The default value is 1 giving a total of 296 video line periods per frame. The programming details of the *frame_enable_front_porch* are given in Table C-1. The digital video frame timing is shown in Figure 5-17.

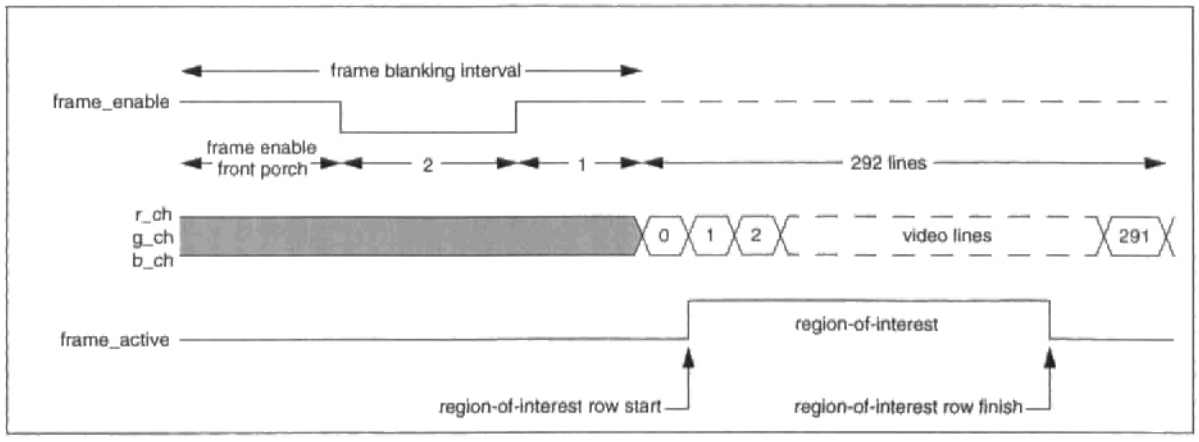


Figure 5-17. Digital video frame timing. The frame enable front porch and the rows forming the region-of-interest are programmable.

5-5.3.2 Video Line Timing

The *line_enable* signal is generated by the camera to delimit each line of video data. The line blanking interval is fixed at 28 *pck* cycles. It will be shown in Section 5-5.4 that this allows sufficient time to perform electronic shutter, sample the signal and reset levels in the current sensor read-out row, and provide a number of additional *pck* cycles to absorb the latency of the interpolation and colour correction subsystems. The digital video line timing is given in Figure 5-18.

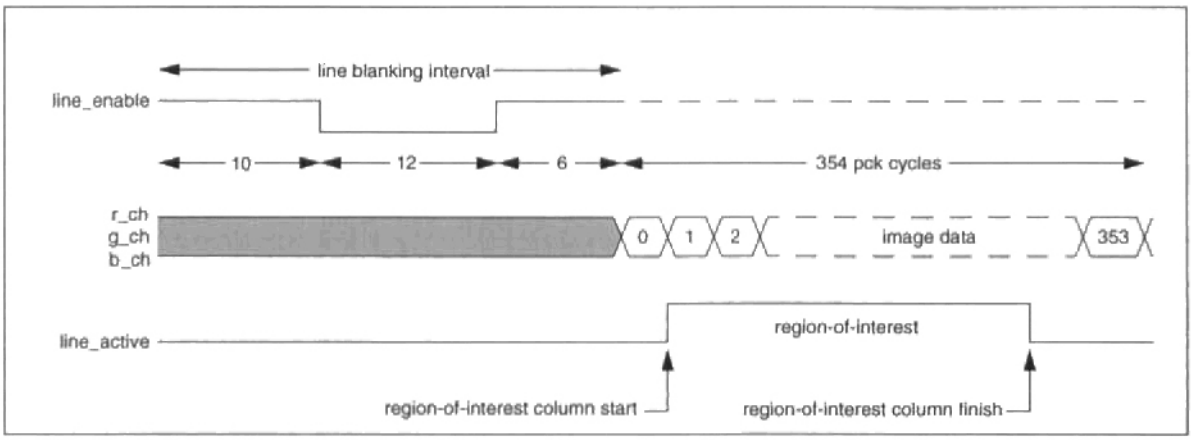


Figure 5-18. Digital video line timing. The columns forming the region-of-interest are programmable.

5-5.3.3 Region-of-Interest

The *frame_active* and *line_active* signals were defined to delimit a programmable region-of-interest in the output video stream. The region of interest is defined by the four parameters shown in Figure 5-19. The valid range of the row start and finish parameters is 0 to 289 while for the column start and finish parameters it is 0 to 353. The row and column finish parameters must be greater than the row and column start parameters respectively. The region-of-interest provides a mechanism to selectively identify pixel values in the video stream generated by the camera. The default region-of-interest delimits a window of CIF resolution (352×288 pixels). The programming details of the region-of-interest are given in Table C-1.

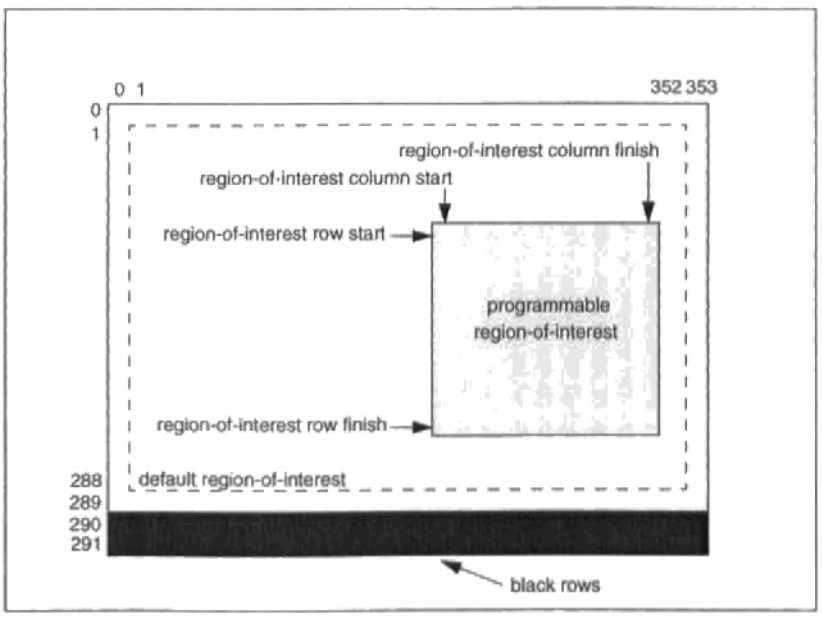


Figure 5-19. Region-of-interest and the output image. Note that the black rows physically occupy the sensor locations shown in Figure 5-6.

5-5.3.4 Pixel Clock Frequency

To achieve a frame rate of 30 frames/second with the default video timing *pck* must have a period $T_{pck} = 295ns$ computed using:

$$T_{pck} = \frac{1}{30\ frames/second \times 296\ line\ periods \times 382\ pck\ cycles}\ seconds \qquad (5\text{-}1)$$

This corresponds to a *pck* frequency of $3.39MHz$.

5-5.4 Photogate Sensor Timing

The video line timing and sensor read-out must be performed in the same number of *pck* cycles. The line blanking interval was chosen of sufficient duration to enable an electronic shutter operation to be performed, and the reset and signal levels for the pixels in each row to be sampled by the column circuits. The buffered reset and signal levels corresponding to the 354 pixels in the read-out row are then driven in turn onto sensor output buses V_r and V_s respectively. When the second level of correlated double sampling is enabled the *zero* signal is used in conjunction with the column decoding logic to generate the crowbar signal *cb* shown in Figure 5-7. The sensor array line timing is shown in Figure 5-20.

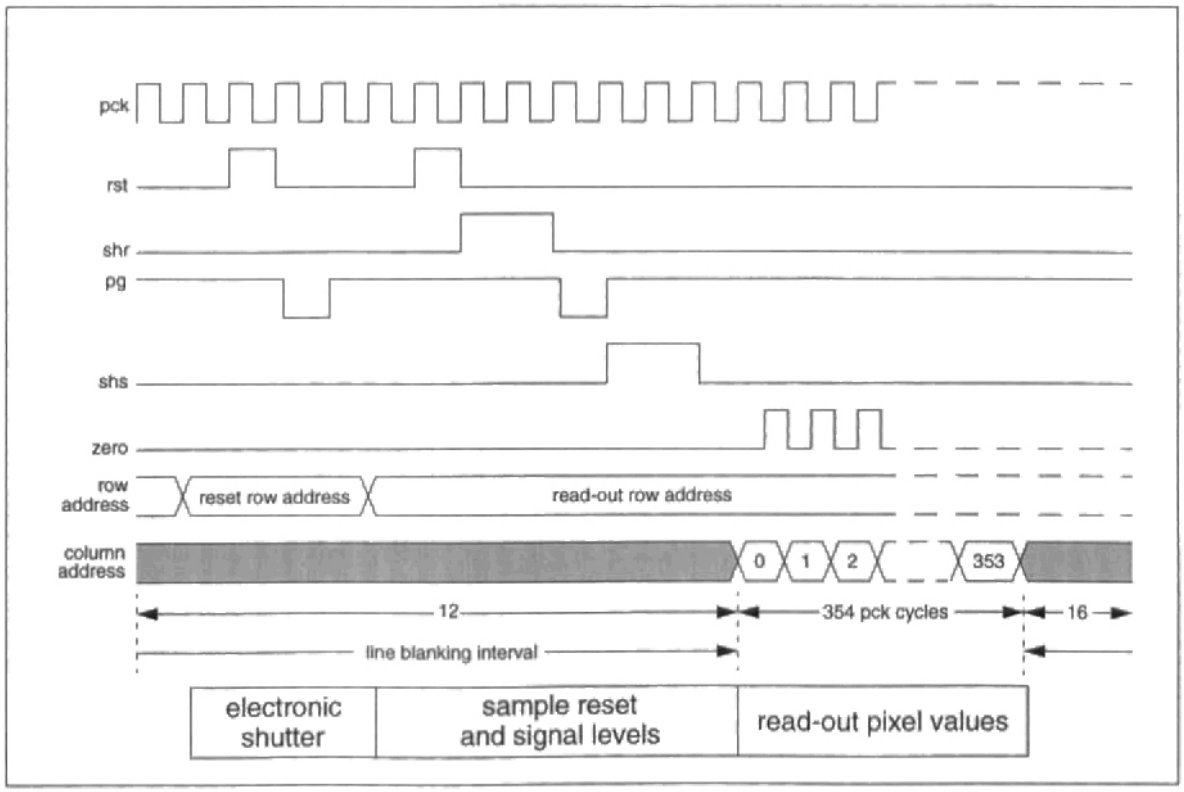


Figure 5-20. Sensor array line timing.

5-5.4.1 Electronic Shutter

Electronic shutter for a CMOS sensor normally takes the form of a "dummy read-out" or charge reset (Section 2-5.4.2). This technique as implemented in the single-chip camera involves dumping the charge collected by the pixels in each row an integer number of line periods prior to their read-out. In Figure 5-20 it is shown that the electronic shutter operation is performed in the line blanking interval by addressing the reset row and pulsing the *rst* and *pg* signals to empty the potential wells of the pixels in that row. The offset in row addresses between the reset row and the read-out row known as the *reset_row_offset* determines the effective integration time T_{int} as illustrated in Figure 5-21. For the default video timing T_{int} is given by:

$$T_{int} = 296\ line\ periods - (296 - reset\ row\ offset) \times line\ period \quad seconds \qquad (5\text{-}2)$$

where each line period is 382 *pck* cycles or $113\mu s$. The parameters for programming the *reset_row_offset* and enabling electronic shuttering are given in Table C-1 and Table C-2 respectively.

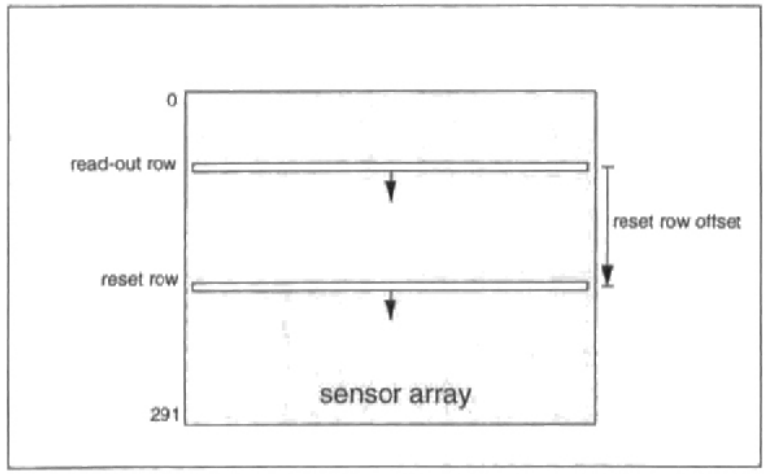


Figure 5-21. Electronic shuttering.

5-5.4.2 Managing Latency for Quiet Operation

To ensure quiet operation during the electronic shutter and column circuit sampling operations it is necessary that all digital subsystems are inactive during this period. However, the interpolation and colour correction subsystems responsible for producing the digital video stream cannot be arbitrarily stalled as the video line timing of Figure 5-18 requires that 354 pixel values be output from the camera on consecutive *pck* cycles. For this reason 16 further *pck* cycles were included in the line blanking interval in addition to the 12 required to perform the electronic shutter and column circuit sampling operations. This accounted for the latency

of the interpolation and colour correction systems per image row and allowed quiet operation during the 12 critical *pck* cycles of the line blanking interval.

5-6. Camera System Control

Having presented the high-level architecture of the single-chip camera, the switching noise management scheme, and the video and sensor timing requirements, it is now possible to describe their implementation. In this section the camera control system is presented including a number of global signals and data types. The generation of the camera system clocks is also briefly discussed.

5-6.1 The Control Finite State Machines

To generate the timing signals required by the digital video format and for sensor read-out two finite state machines (FSM) were designed, and together with a local parameter store form the camera system control module.

5-6.1.1 The Video FSM

The first FSM generates the video timing signals and is shown in block diagram form in Figure 5-22 together with the control parameter store. The video FSM is clocked by *pck* and the host places the camera in video mode by taking the *camera_mode* signal low. When the camera is running in video mode it generates the video synchronization signals *frame_enable* and *line_enable*, along with the *frame_active* and *line_active* signals used to delimit the region-of-interest. The video FSM uses the flag *start_sensor_FSM* to start the second FSM which controls the timing of the sensor array. The *start_sensor_FSM* flag is taken high when the *frame_enable* signal is taken low at the start of each video frame. When *camera_mode* is taken high the camera is placed in program mode and no video is output from the camera.

5-6.1.2 The Control Parameter Store

The control parameter store contains parameters used by both the video and sensor FSMs, as well as parameters that configure the camera architecture. The parameters resident in the control parameter store are listed in Section C-1 and are organized into two sets. The first set of parameters gives the *reset_row_offset* used with electronic shuttering, defines the region-of-interest, and specifies the *frame_enable_front_porch*. A parameter known as the *frame_offset* is provided to insert a programmable delay between the start of the sensor FSM relative to the video FSM. This will be discussed further in the following subsection. A parameter is also required to describe the realized primary Bayer checkerboard CFA pattern to the camera hardware. This information is encoded in a parameter known as the *mosaic_pattern* using one of the four values shown in Figure 5-23. The top left-hand location of the

mosaic_pattern corresponds to address *(0, 0)* of the sensor array. This allows any inconsistencies between the designed and manufactured CFA pattern to be compensated for by simply changing the value of the parameter. The *mosaic_pattern* is set by the camera configuration word (Table C-2).

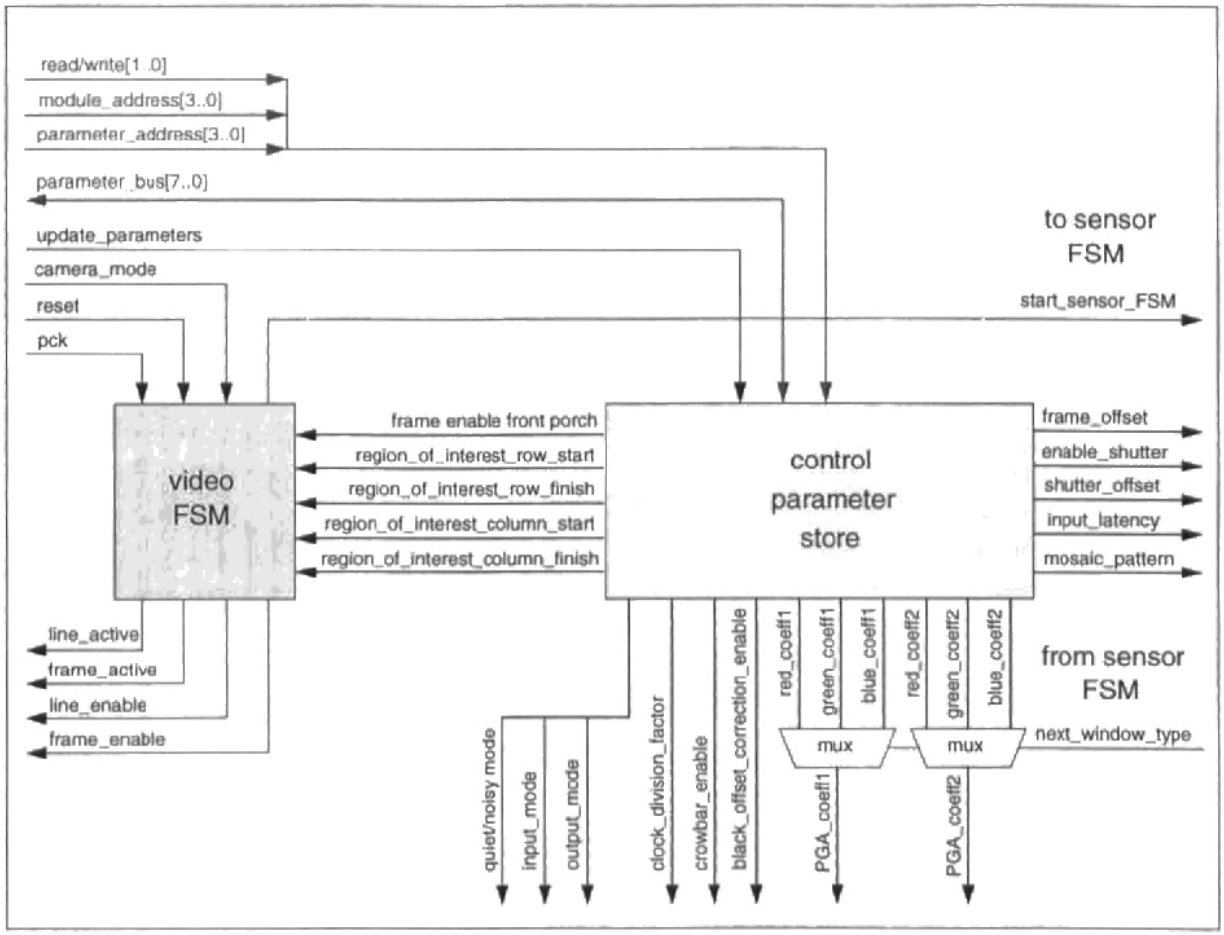


Figure 5-22. Video finite state machine and control parameter store.

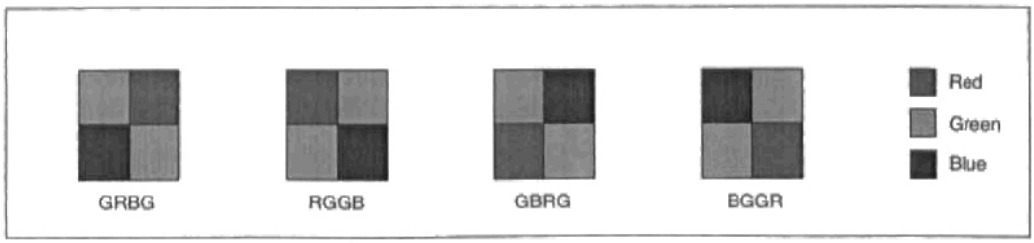


Figure 5-23. Mosaic pattern definitions.

The operation of several camera subsystems prior to spatial interpolation requires information about which colour the current pixel value corresponds to, and the spatial arrangement of the pixel colours immediately surrounding the present pixel value. To this end a data type known as the *window type* was defined. The five members of the window type are shown in

Figure 5-24. The window type is used by the control logic that selects PGA coefficients and by the interpolation subsystem. During normal camera operation the value of the window type is generated internally by the sensor FSM based on the current row and column address of the sensor read-out. This information is encoded in a signal called *next_window_type*. The centre location of the window type gives the present pixel colour. However, when testing the camera digital subsystem with external vectors it is also possible to externally provide the *next_window_type* signal. Whether the source of the window type is internal or external is set by the *camera_configuration_word* (Table C-2).

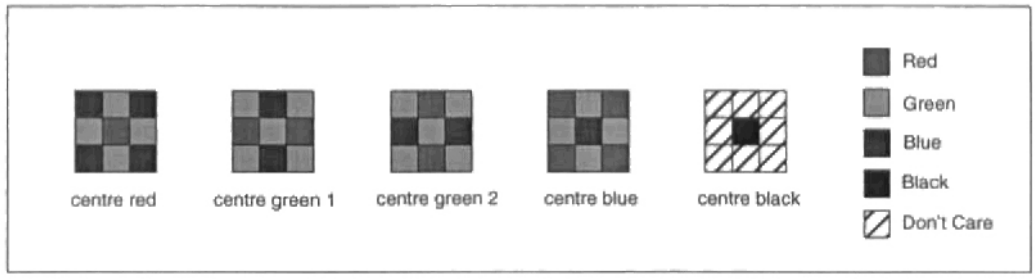


Figure 5-24. Window type definitions.

The second set of parameters in the control parameter store are used to set flags to enable or disable analog operations such as crowbar and black offset level correction, and provide the active gain values for the PGA. A further parameter is employed to describe the digital input latency, i.e. the number of *pck* cycles between changing the sensor column address and the corresponding digitized pixel value appearing at the input to the camera digital system. By default the input latency has a value of two, one cycle each for the A/D and PGA. If external vectors are applied to the camera digital system for test purposes, this can be modified accordingly. The second set of camera control parameters are described in Table C-3.

5-6.1.3 The Sensor FSM

The sensor FSM provides the timing signals required by the sensor array and is shown in block diagram form in Figure 5-25. The sensor FSM is clocked by *pck* and is enabled by the flag *start_sensor_FSM* set by the video FSM. When this flag is taken high an internal counter is loaded with the *frame_offset* parameter and the sensor FSM waits this number of *pck* cycles before commencing sensor array read-out. The *frame_offset* parameter is used to align the pixel data produced by the camera digital system, with the video synchronization signals generated by the video FSM. This is necessary because the data latency through the camera digital system is dependent on the processing stages performed. For example the interpolation subsystem has a latency in excess of two video lines, while the colour correction subsystem has a latency of only two *pck* cycles. For this reason the *frame_offset* parameter must be set by the host to a value consistent with the desired camera output mode.

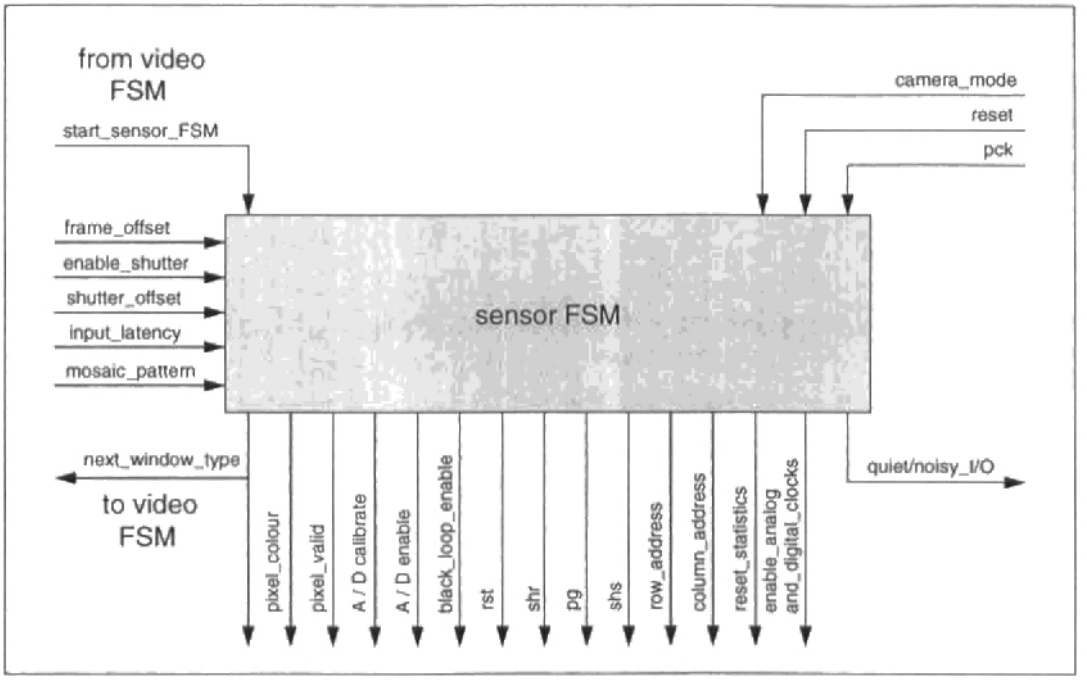


Figure 5-25. The sensor finite state machine.

The sensor FSM also generates signals needed by the PGA, the A/D converter, and the interpolation and image statistics subsystems. For example, the *pixel_valid* flag is set whenever the present pixel value corresponds to a red, green, or blue value. It is not set during the blanking intervals or when reading out a black row from the sensor. The *pixel_valid* signal is required because the interpolation and image statistics subsystems must only operate on data corresponding to pixels in the imaging part of the sensor array. The sensor FSM also produces a number of signals associated with the switching noise management scheme. The signal *enable_analog_and_digital_clocks* is supplied to the clock generation module to suppress the generation of *ack1*, *ack2*, *ack3*, and *dck* during the portion of the line blanking interval coinciding with the electronic shutter and column circuit sampling operations. The *quiet/noisy_I/O* signal is employed to inform the host that it should suspend parameter I/O operations during this interval for quiet operation.

5-6.2 Clock Generation

The camera system clocks shown in Figure 5-15 are produced by a clock generation module consisting of a clock divider and FSM, and distributed using buffers and a clock tree. The clock generation architecture is shown in Figure 5-26. A divider was employed as part of the clock generation architecture to allow the camera system to be run at a reduced rate without changing the external clock provided to the chip. The *clock_division_factor* parameter can be set by the host to divide the external clock by 1, 2, 4, or 8 as described in Table C-1. A state

machine was used to generate the different clocks required by the camera system from the output of the clock divider. If the signal *enable_analog_and_digital_clocks* is high, the analog clocks *ack1*, *ack2*, and *ack3*, are produced along with the digital clock *dck*. The *noisy/quiet_mode* flag is employed to select which of the phase relationships *dck* takes, as shown in Figure 5-15. The clocks *pck* and *fck* are always generated, independent of the state of *enable_analog_and_digital_clocks*.

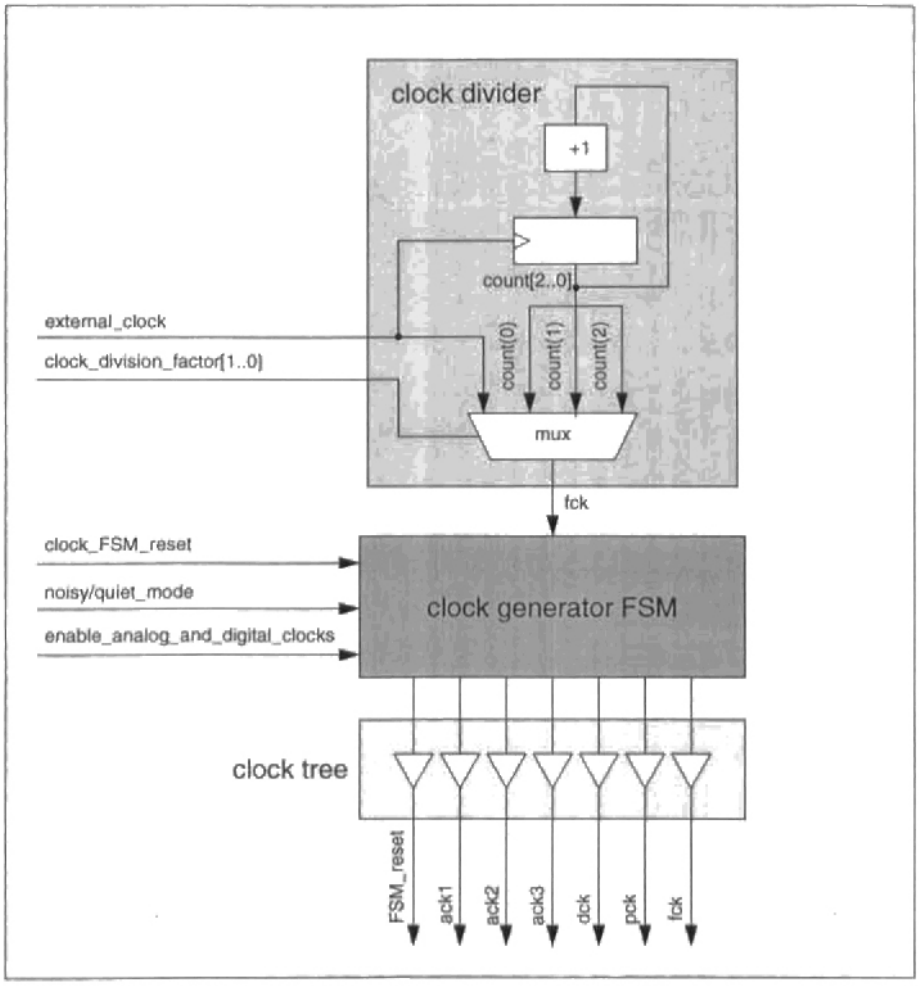


Figure 5-26. Clock generation architecture.

5-7. Spatial Interpolation Subsystem

The use of a colour filter array (CFA) to realize a single-chip colour image sensor necessitates spatial interpolation to construct three colour components for each pixel. An elementary interpolation scheme based on linear low-pass filtering over a 3×3 pixel neighbourhood was used with the single-chip camera due to its ease of implementation. While this scheme produced some visible colour aliasing artifacts at luminance transitions in the image, these could be reduced with a more advanced interpolation technique and are not indicative of APS tech-

nology itself [Parulski et al. 1989, Hibbard 1995]. In this section the interpolation algorithm employed by the single-chip camera will be described together with the requirements for mapping it to hardware. The implementation of the FIFOs needed by the algorithm are discussed before the architecture of the spatial interpolation subsystem is presented. The sequencing of the interpolation subsystem is then described followed by the architecture and operation of the multiply-accumulate units.

5-7.1 The Interpolation Algorithm

Performing linear spatial low-pass filtering over a 3×3 pixel neighbourhood for each frame of image data generated from the sensor array can be described formally as follows:

Let P be the image formed by the 354×290 pixel values $P(i,j)$ acquired from the colour photogate sensor each frame as shown in Figure 5-27.

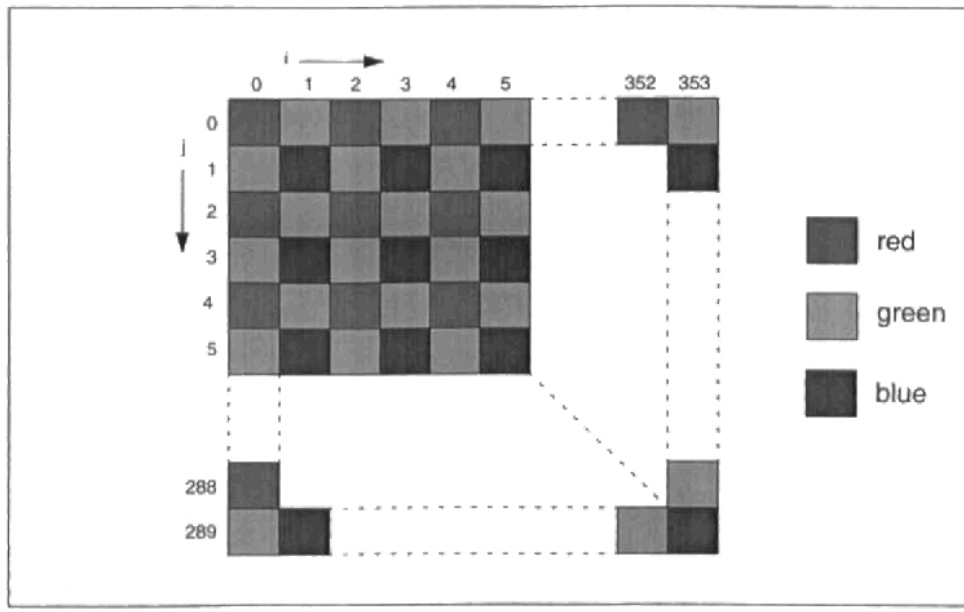


Figure 5-27. The image P formed from the 354×290 colour pixel values acquired from the sensor each frame.

From P three component images P_R, P_G, and P_B can be formed by selectively choosing the red, green, and blue pixel values respectively, and setting all other pixel values to zero. By inspection of Figure 5-27, P_R, P_G, and P_B are defined according to:

$$P_R(i,j) = P(i,j) \,\forall\, (i \bmod 2 = 0 \wedge j \bmod 2 = 0) \text{ else } P_R(i,j) = 0 \tag{5-3}$$

$$P_G(i,j) = P(i,j) \,\forall\, ((i \bmod 2 = 1 \wedge j \bmod 2 = 0) \vee (i \bmod 2 = 0 \wedge j \bmod 2 = 1)) \text{ else}$$

$$P_G(i,j) = 0 \tag{5-4}$$

$$P_B(i,j) = P(i,j) \forall (i \bmod 2 = 1 \wedge j \bmod 2 = 1) \text{ else } P_B(i,j) = 0 \tag{5-5}$$

The 3×3 linear spatial low-pass filtering operation can be described as the convolution of three 3×3 filter kernels K_R, K_G, and K_B, with the three component images P_R, P_G, and P_B. If the two dimensional spatial convolution operator is denoted by * then the interpolated red, green, and blue component images are given by:

$$R_{int} = K_R * P_R \tag{5-6}$$

$$G_{int} = K_G * P_G \tag{5-7}$$

$$B_{int} = K_B * P_B \tag{5-8}$$

As an example, the convolution of K_G with P_G at location $(1, 1)$ is given by:

$$G_{int}(1,1) = K_{G8}P_G(0,1) + K_{G6}P_G(1,0) + K_{G4}P_G(1,2) + K_{G2}P_G(2,1) \tag{5-9}$$

with reference to Figure 5-28. Note that the terms involving multiplication by zero have been omitted from (5-9).

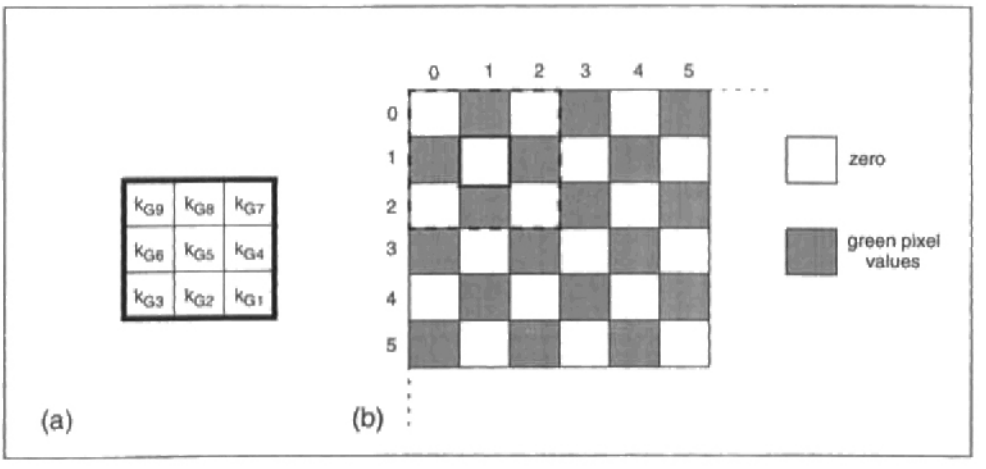


Figure 5-28. (a) The spatial interpolation filter kernel K_G. (b) Convolving the kernel K_G with the component image P_G at location (1,1).

A default set of filter kernel coefficients that were used by the spatial interpolation procedure are:

$$K_R = \begin{bmatrix} 0.25 & 0.5 & 0.25 \\ 0.5 & 1.0 & 0.5 \\ 0.25 & 0.5 & 0.25 \end{bmatrix}, K_G = \begin{bmatrix} 0.125 & 0.25 & 0.125 \\ 0.25 & 0.5 & 0.25 \\ 0.125 & 0.25 & 0.125 \end{bmatrix}, K_B = \begin{bmatrix} 0.25 & 0.5 & 0.25 \\ 0.5 & 1.0 & 0.5 \\ 0.25 & 0.5 & 0.25 \end{bmatrix} \tag{5-10}$$

To simplify the spatial interpolation procedure no interpolation is performed for the pixels along the sensor perimeter, and consequently the interpolated component images R_{int}, G_{int}, and B_{int} have the CIF resolution of 352×288.

5-7.2 Mapping the Interpolation Algorithm to Hardware

To directly implement the interpolation algorithm as defined in Section 5-7.1 results in an inefficient hardware realization. This is because the image data is not available in a memory array format, and instead is output from the sensor A/D as a serial stream of consecutive pixel values. Therefore a direct implementation would require a complete frame store so that each pixel value $P(i,j)$ can be stored for multiple reuse. For example, the pixel value $P_G(3,2) = P(3,2)$ is needed for the evaluation of 9 different 3×3 convolution operations: $G_{int}(2,1)$, $G_{int}(2,2)$, $G_{int}(2,3)$, $G_{int}(3,1)$, $G_{int}(3,2)$, $G_{int}(3,3)$, $G_{int}(4,1)$, $G_{int}(4,2)$, and $G_{int}(4,3)$.

Closer examination of the interpolation algorithm reveals that the minimum memory requirements for implementation involve storing the previous two rows of pixel data output from the A/D. A practical implementation of the interpolation algorithm was developed for the single-chip camera using a pair of FIFOs to hold the last two rows of pixel data, and a 3×3 register file to hold the current interpolation neighbourhood. The operation of this interpolation scheme can be described with reference to Figure 5-29.

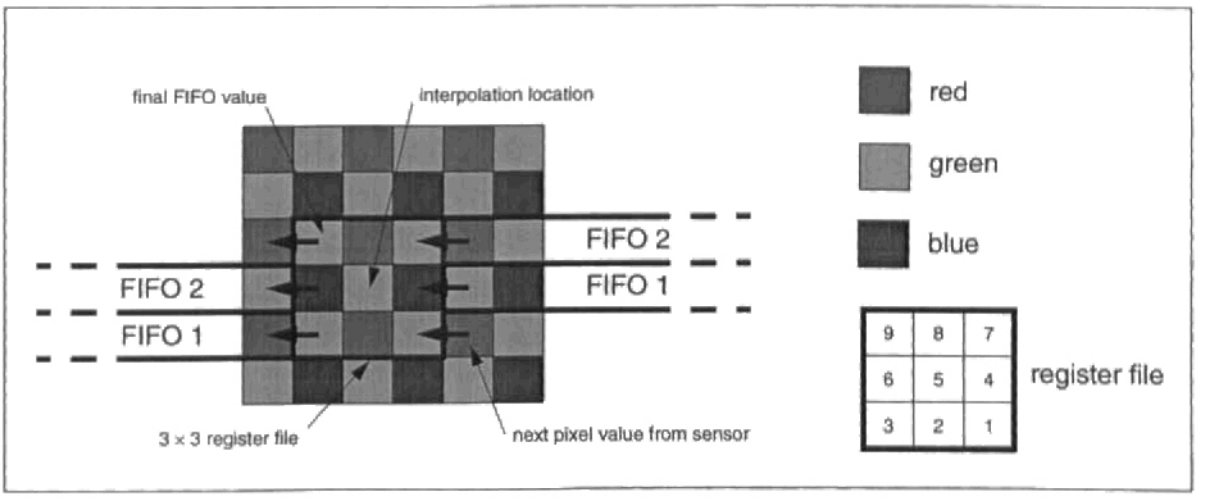


Figure 5-29. An implementation of the spatial interpolation algorithm using a FIFO pair and a 3×3 register file.

Each pixel value as it is output from the A/D is loaded into *register1* of the 3×3 register file. The pixel values from the previous two rows corresponding to the same sensor column are removed from *FIFO1* and *FIFO2* and loaded into *register4* and *register7* respectively. Once the correct pixel values have been loaded into the register file in this fashion, additional hard-

ware (not shown in Figure 5-29) can perform the necessary arithmetic operations with the filter kernel coefficients of K_R, K_G, and K_B to generate the interpolated components $(R_{int}, G_{int}, B_{int})$ for the sensor location corresponding to *register5* of the register file. The details of which registers in the register file are multiplied with which coefficients are dependent on the current window type as defined in Figure 5-24. Finally the pixel values in *register3* and *register6* of the register file are inserted into *FIFO1* and *FIFO2* respectively for later reuse, and the contents of the register file are shifted by one register to the left ready to begin the next interpolation operation.

5-7.3 FIFO Implementation

For the spatial interpolation scheme described in the previous section, the pixel values are inserted and removed from *FIFO1* and *FIFO2* in parallel. For an 8-bit pixel representation it is possible to use a single FIFO of size 352 × 16 bits to realize *FIFO1* and *FIFO2*. Power and area efficient implementations of FIFOs of this size are based on SRAM rather than registers. A full-custom single-port SRAM developed by Jay O'Neil of Bell Laboratories was available in the target CMOS technology that provided significant power and area savings over the equivalent standard-cell realization. For this reason the interpolation FIFO was implemented using a full-custom 352 × 16 bit SRAM, and suitable address generation logic synthesized to support the insertion and removal of pixel values from *FIFO1* and *FIFO2*. One important characteristic of the full-custom SRAM design employed by the interpolation subsystem is that while it supported a 1 cycle write operation, it required two cycles to perform a read operation as illustrated by the timing diagram of Figure 5-30. This had implications for the timing of the spatial interpolation subsystem that will be discussed shortly.

The architecture of the interpolation subsystem is based on three internal buses for the red, green, and blue pixel values respectively. The reasons for this will become apparent when the architecture is described in Section 5-7.4. The FIFO architecture is shown in Figure 5-31. Instructions are provided to the FIFO from the interpolation subsystem FSM. These instructions are decoded and a pair of pixel values from any two of the three internal buses are inserted or removed from *FIFO1* and *FIFO2* in parallel. Separate registers are used to store the current location of the top and bottom of the FIFO.

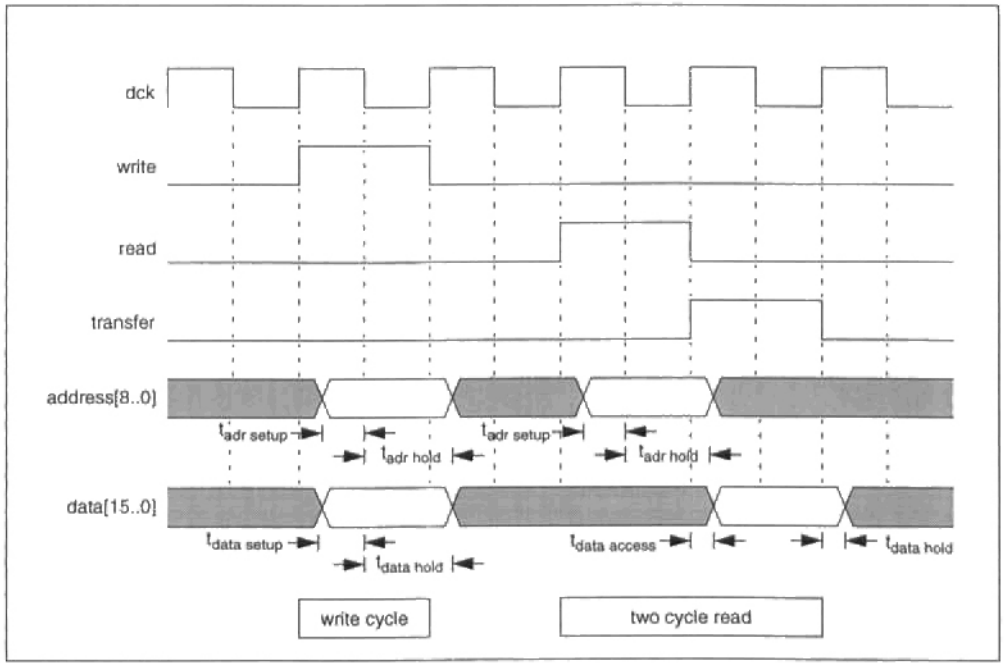


Figure 5-30. SRAM timing.

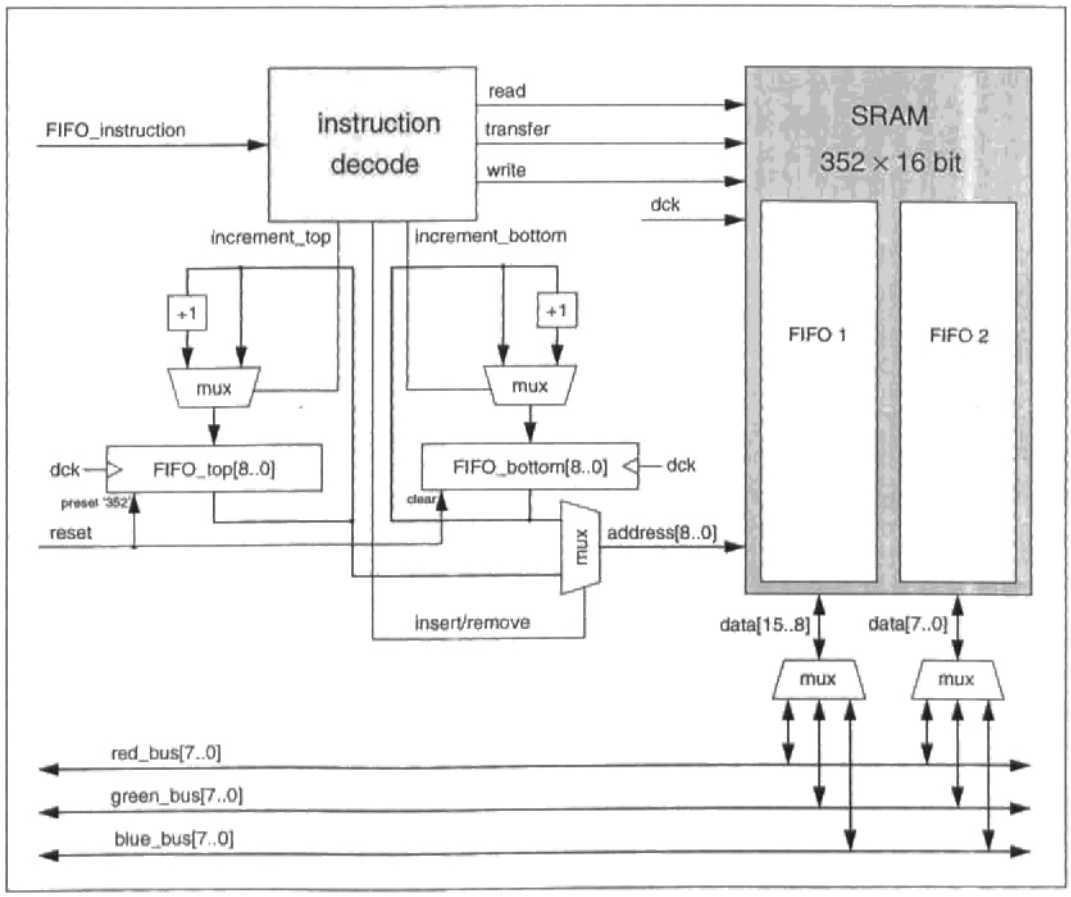


Figure 5-31. FIFO architecture.

5-7.4 Interpolation Subsystem Architecture

The interpolation scheme described in Section 5-7.2 was realized in hardware using the architecture shown in Figure 5-32. In addition to the FIFOs discussed in Section 5-7.3, the architecture is based on a 3×3 register file, and three internal buses are employed to transfer data corresponding to red, green, and blue pixels respectively. Furthermore, three parallel multiply-accumulate (MAC) units are provided to compute the R_{int}, G_{int}, and B_{int} components respectively by convolving the pixel values in the register file with the appropriate kernel coefficients. From Figure 5-29 it is clear that when inserting or removing data from *FIFO1* and *FIFO2*, the two 8-bit data values will always correspond to different colours. As the insertion or removal of 8-bit data from *FIFO1* and *FIFO2* occurs in parallel, it is necessary to have at least two buses to transfer data to and from the register file. However, when data is being transferred between the register file and the FIFOs, it can also be loaded into the appropriate two MAC units. The provision of a third bus allows the otherwise unused MAC unit to be loaded with data from the register file at the same time. The interpolation subsystem is clocked by *dck*. Using the architecture of Figure 5-32 it is possible to perform the necessary data transfer operations in 5 *dck* cycles. However, as the SRAM requires a two cycle read, 6 *dck* cycles are needed in practice.

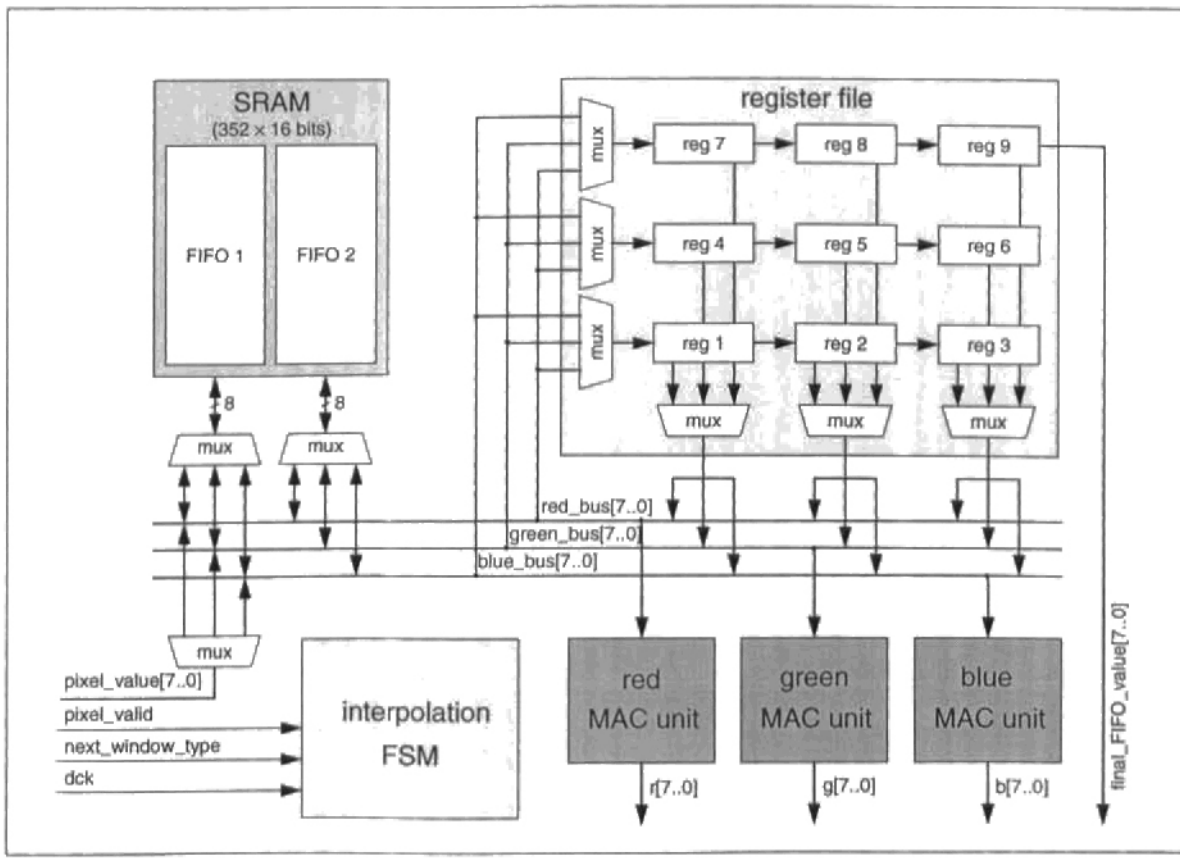


Figure 5-32. Interpolation architecture. Note that the register file is labelled in a manner consistent with Figure 5-29.

5-7.4.1 Data Flow Through The Interpolation Subsystem

The data flow through the interpolation subsystem can be described using as an example a data value output from the A/D corresponding to a red pixel. During the first *dck* cycle the contents of the 3 × 3 register file are shifted to the right by one register, i.e. *register1* → *register2*, *register2* → *register3*, *register4* → *register5*, *register5* → *register6*, *register7* → *register8*, and *register8* → *register9*. The previous contents of *register3*, *register6*, and *register9* are discarded. At the same time the current pixel value from the A/D, a red pixel value in this example, is simultaneously loaded into *register1* and the red MAC unit via the *red_bus*. During the second and third *dck* cycles, the pixel values from the previous two rows are removed from *FIFO1* and *FIFO2* in parallel, and loaded into *register4* and *register7* and the green and red MAC units, via the *green_bus* and *red_bus* respectively. During the fourth *dck* cycle the pixel values in *register3* and *register6* are inserted into *FIFO1* and *FIFO2* respectively, and the red and green MAC units. In the fifth *dck* cycle the pixel values in *register5*, *register8*, and *register9* are loaded into the blue, green, and red MAC units respectively. In the sixth *dck* cycle the contents of register2 are loaded into the green MAC. Data flow through the interpolation subsystem is similar for values output from the A/D corresponding to green, and blue pixels. The sequencing of the interpolation subsystem is described further in Table 5-2, and the architecture and operation of the MAC units will be presented in Section 5-7.6.

5-7.4.2 Testing Data Flow Through The Interpolation Subsystem

To test the flow of pixel data through the interpolation subsystem the camera *input_mode* can be set to *1* in the *camera_configuration_word* (Table C-2), and external test vectors introduced to the camera digital system via the *test_input* bus (see Figure 5-12). Consistent with Figure 5-29, *register9* corresponds to the final stage in data flow through the interpolation subsystem. By setting the camera *output_mode* to *00* the pixel value stored in *register9* is driven onto the *final_FIFO_value* bus rather than being discarded, and into the *g_ch* camera output bus (see Figure 5-12). This allows the interpolation data flow to be functionally tested.

5-7.5 The Interpolation FSM

The operation of the interpolation subsystem is controlled by a finite state machine (FSM) clocked by *dck*. Interpolation commences when the *pixel_valid* flag generated by the sensor FSM is set (Section 5-6.1.3). This signals that data corresponding to a red, green, or blue pixel is present on the *pixel_value* bus. Spatial colour information about the current pixel value is encoded in the signal *next_window_type*, also produced by the sensor FSM. The state table for the interpolation FSM is given in Table 5-2 and illustrates the dependence of the interpolation subsystem operations on the value of *next_window_type*.

dck cycle	*next_window_type*			
	centre red	centre green 1	centre green 2	centre blue
1	reg 1 → reg 2 reg 2 → reg3 reg 4 → reg 5 reg 5 → reg 6 reg 7 → reg 8 reg 8 → reg 9 pixel_value → reg 1 blue MAC (blue bus)	reg 1 → reg 2 reg 2 → reg3 reg 4 → reg 5 reg 5 → reg 6 reg 7 → reg 8 reg 8 → reg 9 pixel_value → reg 1 green MAC (green bus)	reg 1 → reg 2 reg 2 → reg3 reg 4 → reg 5 reg 5 → reg 6 reg 7 → reg 8 reg 8 → reg 9 pixel_value → reg 1 green MAC (green bus)	reg 1 → reg 2 reg 2 → reg3 reg 4 → reg 5 reg 5 → reg 6 reg 7 → reg 8 reg 8 → reg 9 pixel_value → reg 1 red MAC (red bus)
2	commence data removal from FIFOs (SRAM has two cycle read)			
3	FIFO 1 → reg 4 green MAC (green bus) FIFO 2 → reg 7 blue MAC (blue bus)	FIFO 1 → reg 4 red MAC (red bus) FIFO 2 → reg 7 green MAC (green bus) reg 8 → blue MAC (blue bus)	FIFO 1 → reg 4 blue MAC (blue bus) FIFO 2 → reg 7 green MAC (green bus) reg 8 → red MAC (red bus)	FIFO 1 → reg 4 green MAC (green bus) FIFO 2 → reg 7 red MAC (red bus)
4	reg 3 → FIFO 1 blue MAC (blue bus) reg 6 → FIFO 2 green MAC (green bus)	reg 3 → FIFO 1 green MAC (green bus) reg 6 → FIFO 2 red MAC (red bus) reg 2 → blue MAC (blue bus)	reg 3 → FIFO 1 green MAC (green bus) reg 6 → FIFO 2 blue MAC (blue bus) reg 2 → red MAC (red bus)	reg 3 → FIFO 1 red MAC (red bus) reg 6 → FIFO 2 green MAC (green bus)
5	reg 5 → red MAC (red bus) reg 8 → green MAC (green bus) reg 9 → blue MAC (blue bus)	reg 5 → green MAC (green bus)	reg 5 → green MAC (green bus)	reg 5 → blue MAC (blue bus) reg 8 → green MAC (green bus) reg 9 → red MAC (red bus)
6	reg 2 → green MAC (green bus)	reg 9 → green MAC (green bus)	reg 9 → green MAC (green bus)	reg 2 → green MAC (green bus)

Table 5-2. Interpolation FSM state table.

5-7.6 The Interpolation Multiply-Accumulate Units

The spatial interpolation algorithm described in Section 5-7.1 can support general linear spatial filtering over a 3×3 pixel neighbourhood if the coefficients of the three filter kernels K_R, K_G, and K_B are allowed to take on any values. To support the greatest possible interpolation flexibility for the single-chip camera it was decided to realize programmable kernel coefficients rather than employing a set of fixed coefficients. While this resulted in a substantial hardware overhead, it did allow an unforeseeable performance characteristic of the photogate sensor to be corrected for which will be discussed in Section 5-7.6.4

5-7.6.1 Interpolation Coefficients

Each coefficient of the 3×3 filter kernels K_R, K_G, and K_B used in the interpolation subsystem is programmable and represented using a 6-bit signed[1] mantissa and a 4-bit unsigned exponent that is always interpreted as negative.

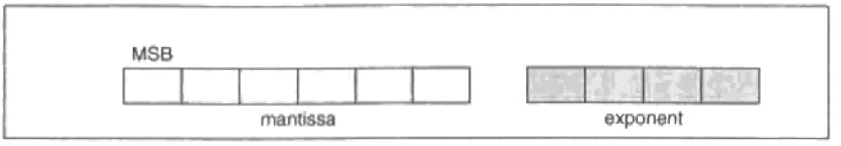


Figure 5-33. Representation of the interpolation coefficients.

The value of each filter coefficient can be computed using:

$$coefficient = (mantissa) \times 2^{-(exponent)} \tag{5-11}$$

For example, the coefficient *111101 0011* is –0.375 in decimal. Rather than each coefficient having an individual exponent, a single exponent is shared with all coefficients within each filter kernel. While this reduces the available "dynamic range" of the coefficients, it simplifies the implementation of the MAC unit by requiring only a single normalization at the MAC unit output. Coefficients that can be represented using this format fall in the range defined by:

$$\frac{-32}{2^{(exponent)}} \leq coefficient \leq \frac{31}{2^{(exponent)}} \quad \text{where } 0 \leq exponent \leq 15 \tag{5-12}$$

The interpolation coefficient parameters, their default values, and their programming details are given in Table C-4.

5-7.6.2 Interpolation MAC Unit Architecture

The architecture of the red, green, and blue MAC units are identical and shown in Figure 5-34. Each MAC unit comprises a multiplier, adder, shifter, and coefficient store. The MAC unit is pipelined using registers clocked by *dck*.

1. Two's complement representation.

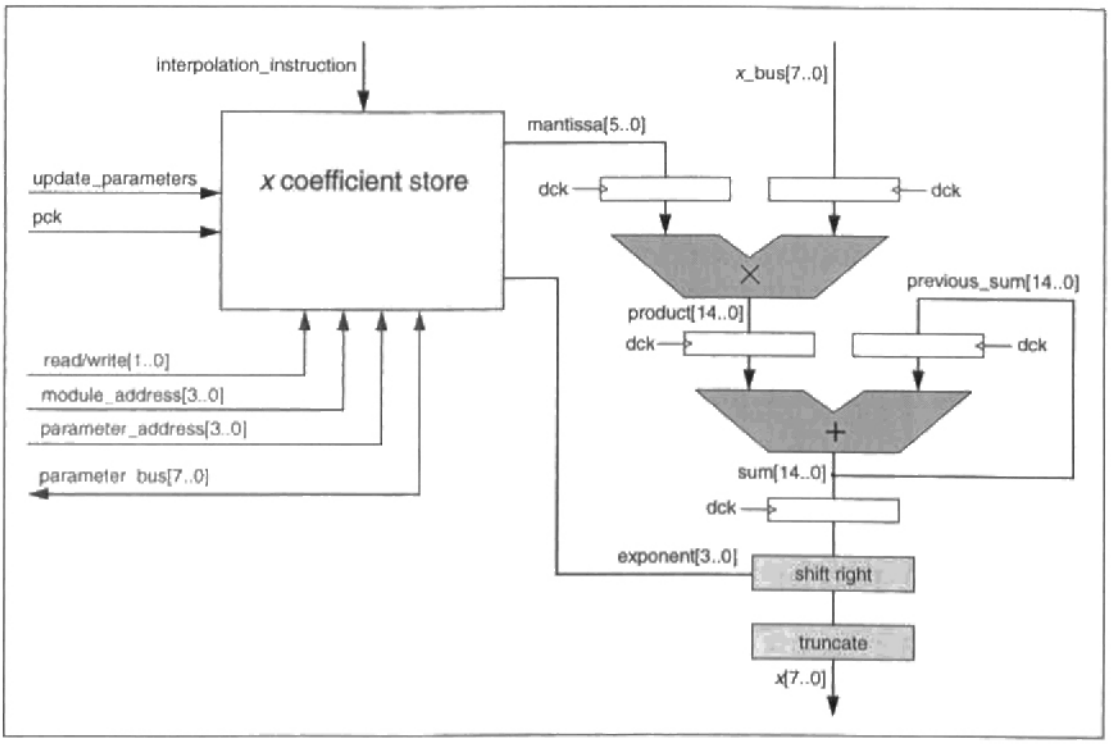


Figure 5-34. Interpolation MAC unit architecture. Note that *x* corresponds to red, green, or blue.

5-7.6.3 Interpolation MAC Unit Operation

As described in Table 5-2 pixel values are loaded into the MAC units from the *red_bus*, *green_bus*, and *blue_bus* internal to the interpolation system. As each pixel value is loaded into a MAC unit, the mantissa of the appropriate coefficient is fetched from the coefficient store based on the which register the pixel value originated from or is intended for. After multiplication the product is accumulated by the adder with the previous sum if required. After the accumulation of all the product terms in the convolution the result is normalized by shifting to the right the number of bits determined by the kernel exponent. To produce the output value the final result is truncated to 8-bits. For correct MAC unit operation a number of control signals not shown in Figure 5-34 are used to clear the previous sum at the start of each interpolation operation, and stall the MAC unit while waiting for the next pixel value. The MAC units have a latency corresponding to 2 *pck* cycles. The total latency of the interpolation subsystem is 714 *pck* cycles, 712 of which are contributed by the FIFO and register file. This means that the interpolation subsystem does not start producing valid output results until after two rows of sensor read-out.

5-7.6.4 Interpolation Coefficients And The Colour Photogate Sensor

While the decision to support fully programmable interpolation coefficients resulted in greater complexity for the MAC unit architecture, it did allow an unexpected characteristic of

the colour photogate sensor to be compensated for. After the camera was manufactured and the CFA deposited it was found that the optical sensitivity of the green pixels in adjacent rows of the sensor were slightly different. This behaviour is caused by colour cross talk which was discussed in Section 4-12.4.2. It effectively results in two types of green pixel that have been denoted green1 and green2 as shown in Figure 5-35.

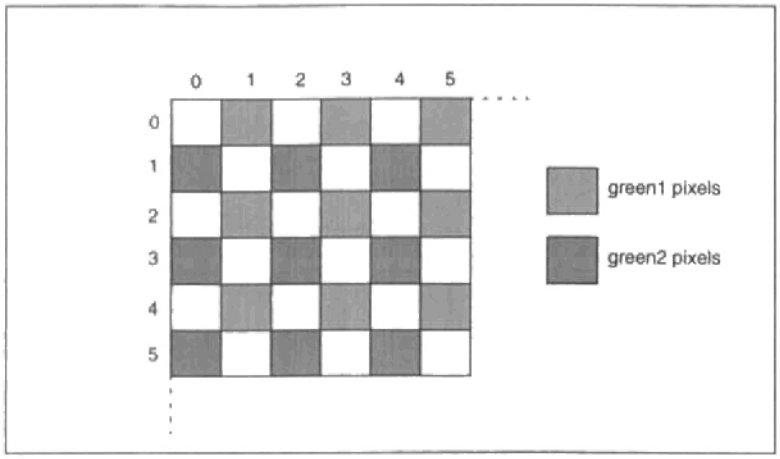


Figure 5-35. Illustrating the two types of green pixel of the colour photogate sensor.

Having two types of green pixels can result in unwanted visible artifacts in the interpolated image depending on the selection of the interpolation coefficients. In the absence of this information the most natural coefficients to use for interpolating the green pixel values are:

$$K_G = \begin{bmatrix} 0.0 & 0.25 & 0.0 \\ 0.25 & 1.0 & 0.25 \\ 0.0 & 0.25 & 0.0 \end{bmatrix} \tag{5-13}$$

This filter kernel implies that when interpolating 3×3 pixel neighbourhood with a green pixel in the centre, just use that pixel value for G_{int}. However, it was found that if this set of coefficients was employed, a checkerboard pattern was visible in the image data generated by the interpolation subsystem due to the differences in optical sensitivity of the green1 and green2 pixels. Fortunately, as the kernel coefficients are programmable it was possible to select an alternative set of coefficients to suppress this phenomena. By ensuring that all green pixel values within each 3×3 neighbourhood are used in the computation of the convolution, the effect of the green1 and green2 pixels can be averaged. The coefficients employed to interpolate the green pixels and suppress this effect are:

$$K_G = \begin{bmatrix} 0.125 & 0.25 & 0.125 \\ 0.25 & 0.5 & 0.25 \\ 0.125 & 0.25 & 0.125 \end{bmatrix} \tag{5-14}$$

5-7.7 Discussion Of The Interpolation Architecture

While the ability to program the interpolation coefficients was found to be valuable, the precision with which the interpolation coefficients are represented is excessive, particularly the exponent range. A substantially simpler scheme in terms of hardware could be developed by restricting coefficients to powers of 2, for example 2, 1, 0.5, 0.25, 0.125 etc. This still supports the default coefficients given in (5-10) and would allow the multiplier of Figure 5-34 to be replaced by a shift register, and the final normalization stage would be redundant. Simplifying the interpolation MAC unit architecture in this way could result in significant area and power savings. However, it is more likely that future interpolation schemes will use advanced non-linear algorithms rather than linear low-pass filtering to provide greater suppression of colour aliasing artifacts [Parulski et al. 1989, Hibbard 1995]. To implement these techniques would require a complete redesign of the interpolation MAC unit architecture. If the chosen interpolation scheme operated over a 3 × 3 pixel neighbourhood, the remainder of the interpolation architecture in terms of the register file, FIFO, and internal buses could be reused.

5-8. Colour Correction Subsystem

To improve the colour rendition of a solid-state camera and transform into a standard colour space, it is necessary to apply a linear 3 × 3 matrix to the interpolated colour components $(R_{int}, G_{int}, B_{int})$ for each pixel (Section 3-4.27.2). If the colour correction matrix is denoted C, then the basic colour correction operation is given by:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{bmatrix} \begin{bmatrix} R_{int} \\ G_{int} \\ B_{int} \end{bmatrix} \tag{5-15}$$

However, in practice it is useful to be able to add offsets to the pixel colour components to improve colour rendition by correcting for offsets introduced by the PGA or A/D. It was decided to implement both pre- and post-offsets in the colour correction subsystem according to:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{bmatrix} \begin{bmatrix} R_{int} + pre\ offset_R \\ G_{int} + pre\ offset_G \\ B_{int} + pre\ offset_B \end{bmatrix} + \begin{bmatrix} post\ offset_R \\ post\ offset_G \\ post\ offset_B \end{bmatrix} \tag{5-16}$$

As the coefficients of C and the pre and post offsets are not known apriori, they must be programmable. Using an off-line calibration scheme similar to that described in

Section 4-13.2, the optimal coefficients and offsets can be found for a given illuminant and downloaded to the single-chip camera by the host.

5-8.1 Colour Correction Coefficients

Each coefficient of the matrix C used in the colour correction system is programmable and represented using a 6-bit signed[1] mantissa and a 2-bit unsigned exponent that is always interpreted as negative with an offset of 2. Unlike the interpolation coefficients, each colour correction coefficient has an individual exponent.

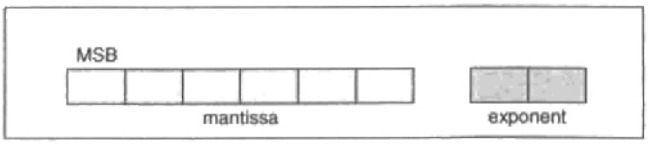


Figure 5-36. Representation of colour correction coefficients.

The value of each colour correction coefficient can be computed using:

$$coefficient = (mantissa) \times 2^{-(exponent+2)} \tag{5-17}$$

As an example the coefficient *110111 11* is –0.28125. Coefficients that can be represented using this format fall in the range defined by:

$$\frac{-32}{2^{(exponent+2)}} \leq coefficient \leq \frac{31}{2^{(exponent+2)}} \quad \text{where } 0 \leq exponent \leq 3 \tag{5-18}$$

As the coefficients are not known apriori the default matrix for C is the identity matrix I. The pre-offsets and post-offsets are represented by 8-bit signed integers giving a range of -128 to 127. The default value for the pre-offsets and post-offsets is 0. The programming details for the colour correction parameters are given in Table C-5.

5-8.2 Colour Correction Architecture

The colour correction operation described by (5-16) was implemented using the architecture shown in Figure 5-37. It comprises an adder, a coefficient store, and three parallel multiply-accumulate (MAC) units. The timing of the colour correction system and MAC units is controlled by a state machine clocked with *dck*. The architecture of the colour correction subsystem was developed jointly with K. J. Singh, however the verification of the colour correction subsystem precision (Section 5-8.3) and the subsequent discussion (Section 5-8.4) are entirely the work of the author.

1. Two's complement representation.

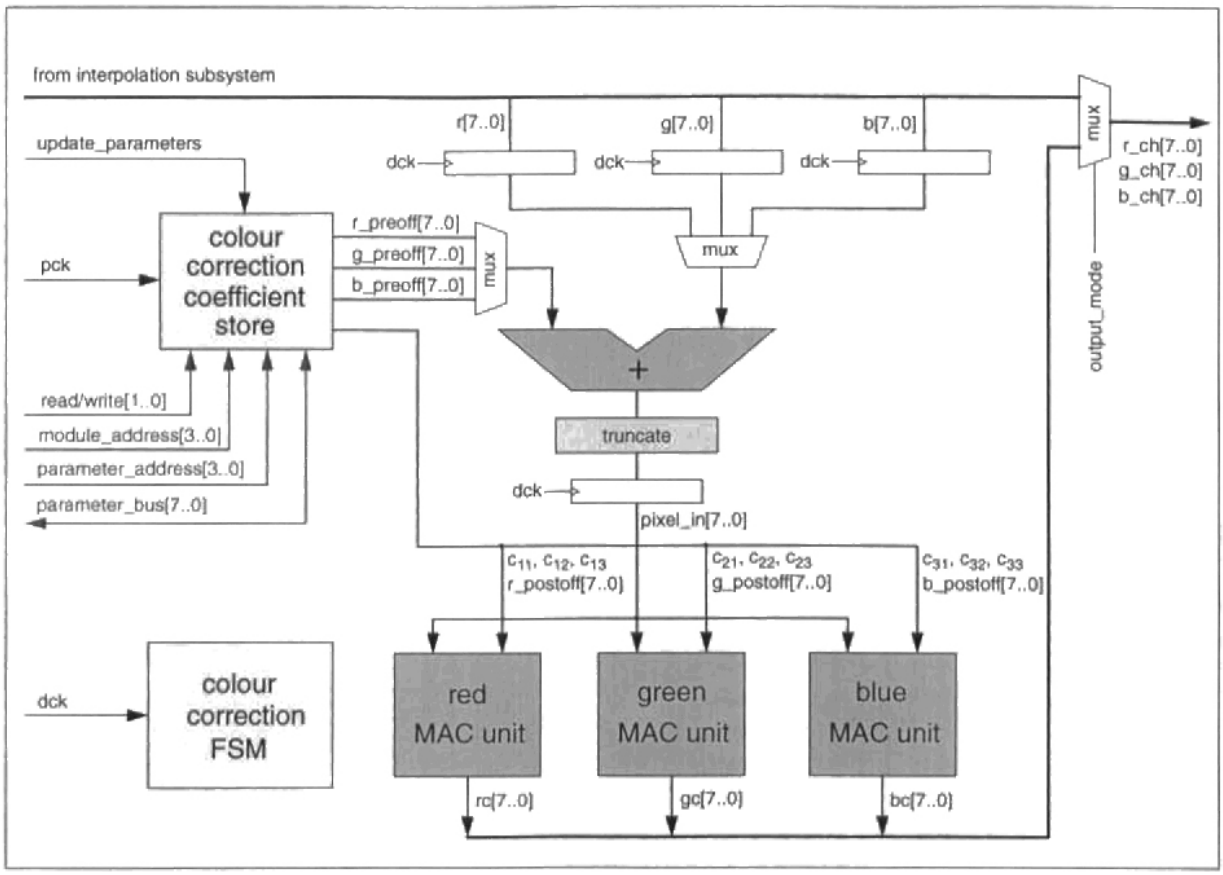


Figure 5-37. Colour correction architecture.

5-8.2.1 Colour Correction MAC Unit Architecture

The architecture of the red, green, and blue colour correction MAC units are identical and shown in Figure 5-38. Each MAC unit comprises a multiplier, adder, and shifter. The MAC unit is pipelined using a number of registers clocked by *dck*.

5-8.2.2 Operation of the Colour Correction Subsystem

The interpolated colour components $(R_{int}, G_{int}, B_{int})$ for each pixel are fed serially into the colour correction subsystem. In the first *dck* cycle the red component R_{int} is added with the red pre-offset, truncated to 8-bits, and then loaded into the thee MAC units in parallel. In subsequent *dck* cycles the appropriate offsets are added to G_{int} and B_{int} in turn, and these results loaded into the MAC units also. As each pre-offset corrected component is loaded into the MAC units, they are multiplied by the mantissa of the appropriate matrix coefficient, and the result normalized by the exponent. For example, when the pre-offset corrected R_{int} is loaded into the MAC units it is simultaneously multiplied by c_{11} in the red MAC unit, c_{12} in the green MAC unit, and c_{13} in the blue MAC unit. In the following cycle these results are accumulated with the product of the pre-offset corrected G_{int} with c_{21} in the red MAC unit, c_{22} in

the green MAC unit, and c_{23} in the blue MAC unit respectively. In the next cycle the pre-offset corrected B_{int} is multiplied by c_{31} in the red MAC unit, c_{32} in the green MAC unit, and c_{33} in the blue MAC unit. Each of these products is accumulated in the MAC unit by an adder with the corresponding post-offset. To produce the output value the final result for each MAC unit is truncated to 8-bits.

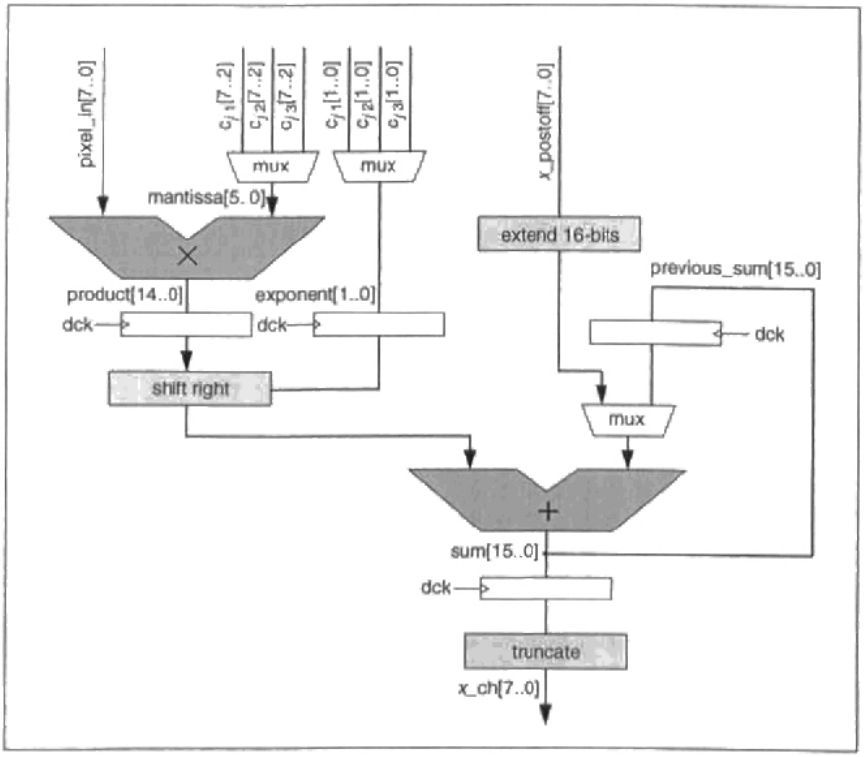


Figure 5-38. Colour correction MAC unit architecture. Note that *j* corresponds to 1, 2, or 3 for *x* taking on the values red, green, or blue respectively.

5-8.3 Precision Of The Colour Correction Subsystem

To verify that the precision of the colour correction subsystem is adequate, it is possible to simulate its application on a set of standard colour samples, for example the samples of the Macbeth ColorChecker, and compare the colorimetric accuracy obtained with that achieved using floating point arithmetic. To perform this simulation the optimal colour correction matrix for the single-chip camera must first be determined. In principle, the procedure employed with the photogate sensor in Section 4-13.2 to find the optimal colour correction matrix can be used to determine the colour correction matrix for the single-chip camera. However, it is clearly not possible to perform this procedure before the camera has been manufactured. Therefore, the colour correction matrix C and tristimulus data $(R_{int}, G_{int}, B_{int})$ acquired from the photogate sensor of Chapter 4 were used in the simulation instead. It can be expected that the colour correction matrix and tristimulus values found for the samples of the Macbeth ColorChecker using the photogate sensor might be similar to those obtained with the single-chip camera. This

is because the target fabrication technology for the single-chip camera was the same as that used for the photogate sensor, a scaled version of the same pixel design was employed, and similar filter characteristics were used for the CFA.

5-8.3.1 Representing the Colour Correction Matrix Coefficients

In Section 4-13.3 the optimal colour correction matrix found for the photogate sensor of Chapter 4 was given by (4-70)[1]. The matrix coefficients and post-offsets have been reproduced in Table 5-3 together with their binary representation in the format of the colour correction subsystem of the single-chip camera (Section 5-8.1). The algorithm used to map from their optimal value in a floating point representation to the closest value in the binary representation of the colour correction subsystem is described in Section C-3.2. The floating point equivalent of the binary representation and the corresponding coefficient error are also tabulated in Table 5-3. The average coefficient error is approximately 2%, neglecting the 100% error for c_{12}. The average post-offset error is about 5%.

Coefficient	Optimal Value (floating point)	Binary Representation	Equivalent Value (floating point)	Error (floating point)	% Error (floating point)
c_{11}	1.1731	010011 10	1.1875	-0.0144	1.23
c_{12}	0.0089	000000 00	0	0.0089	100.0
c_{13}	-0.2637	111000 11	-0.25	-0.0137	5.19
c_{21}	-0.4925	110000 11	-0.5	0.0075	1.53
c_{22}	2.2328	010010 01	2.25	-0.0172	0.77
c_{23}	-0.72668	101001 11	-0.71875	-0.00793	1.09
c_{31}	-0.2358	111000 11	-0.25	0.0142	6.01
c_{32}	-1.4131	101001 10	-1.4375	0.0244	1.72
c_{33}	2.5182	101100 01	2.5	0.0182	0.72
red post-offset	-6.7481	11111001	-7	0.2519	3.60
green post-offset	-7.9056	11111000	-8	0.0944	1.18
blue post-offset	-2.1975	11111110	-2	-0.1975	9.88

Table 5-3. Representing the colour correction matrix of (4-70) in the binary format of parameters of the single-chip camera colour correction subsystem. Note that the pre-offsets have been set to zero.

5-8.3.2 Colorimetric Simulation of the Colour Correction Subsystem

To determine the colorimetric error introduced by the limited precision of the colour correction subsystem, a program was written to simulate the arithmetic operations performed by the colour correction architecture. The 24 tristimulus values $(R_{int}, G_{int}, B_{int})$ obtained for the samples of the Macbeth ColorChecker by the photogate sensor of Chapter 4 (Table B-2) were used in the simulation, together with the binary representation of the matrix coefficients found in Table 5-3. In this manner the set of 24 tristimulus values (R, G, B) in the NTSC colour

1. Determined by minimizing the mean squared error over the 24 samples of the Macbeth ColorChecker in the CIE *XYZ* colour space.

space corresponding to the application of the colour correction subsystem was found. An equivalent set of tristimulus values in the CIE *XYZ* colour space was computed by applying the inverse of matrix $\boldsymbol{P}$ given in (4-62) using full floating point precision. The actual CIE *XYZ* tristimulus values for the Macbeth ColorChecker samples are listed in Table B-1. This allows the mean squared error in the CIE *XYZ* colour space MSE_{XYZ} to be computed using (4-65). Mapping both the actual and computed tristimulus values into the CIE $L^*u^*v^*$ colour space using the transformation described in Section 3-4.18 enables the RMS colour difference in the CIE $L^*u^*v^*$ colour space $(\Delta E^*_{uv})_{RMS}$ to be calculated using (4-72). Each of these results has been listed in Table 5-4 together with the values obtained using full floating point precision. As 1 unit in the CIE $L^*u^*v^*$ colour space corresponds to a "just noticeable difference", it can be concluded from Table 5-4 that the limited precision of the colour correction subsystem does not introduce any visible degradation in colorimetric accuracy. Therefore the precision of the colour correction subsystem is satisfactory and will not limit the colorimetric accuracy of the single-chip camera.

Colour Correction Implementation	MSE_{XYZ}	$(\Delta E^*_{uv})_{RMS}$
floating point representation	6.14	7.94
binary representation (colour correction subsystem)	6.77	8.45

Table 5-4. Comparison of colorimetric error obtained using both a floating point and binary representation for the colour correction matrix. The colorimetric error is given both in terms of the MSE in the *XYZ* colour space, and the RMS $L^*u^*v^*$ colour difference.

5-8.4 Discussion of the Colour Correction Architecture

While the architecture and precision of the colour correction system is sound, it is worth noting that when applying colour correction in the form of (5-16), either the post-offsets or the pre-offsets are redundant. This is because any pre-offset can be expressed as a post-offset and visa versa using the relations:

$$\begin{bmatrix} post\ offset_R \\ post\ offset_G \\ post\ offset_B \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{bmatrix} \begin{bmatrix} pre\ offset_R \\ pre\ offset_G \\ pre\ offset_B \end{bmatrix} \tag{5-19}$$

$$\begin{bmatrix} pre\ offset_R \\ pre\ offset_G \\ pre\ offset_B \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{bmatrix}^{-1} \begin{bmatrix} post\ offset_R \\ post\ offset_G \\ post\ offset_B \end{bmatrix} \tag{5-20}$$

Therefore, to simplify the colour correction hardware all offsets could be included as post-offsets in the MAC units, and the adder in Figure 5-37 used to implement the pre-offsets would no longer be required.

5-9. Image Statistics Subsystem

As the target application of the single-chip camera is a low-cost digital multimedia camera, this precludes the use of several of the exposure control and white balance techniques discussed in Section 3-5.5. For example, it is not envisaged that an automatic mechanized iris could be employed in a low-cost product. However, the exposure of the sensor in the single-chip camera can be controlled using electronic shutter (Section 5-5.4.1), and by changing the gains of the PGA (Section 5-4.4). The white balance of the camera can be managed by adjusting the relative magnitudes of the gains applied to the red, green, and blue pixel values by the PGA. While a detailed design of the exposure control and white balance algorithms had not been finalized prior to the manufacture of the single-chip camera, it was decided to incorporate hardware to compute image histograms into the camera architecture. By determining a separate histogram of the red, green, and blue pixels in each image, a measure of the relative amount of each colour component is found. This could form the basis of a metric for a white balance algorithm. The distribution of the pixel values within the 8-bit range of the A/D provides a measure of the sensor exposure and utilization of the A/D input range [Andersson and Shelby 1994]. By allowing the thresholds that define the histogram bins to be changed by the host in successive frames if desired, a detailed set of statistics can be accrued over a number of frames. Based on such metrics, exposure control and white balance algorithms running in software on the host can download new electronic shutter and/or PGA parameters respectively to the single-chip camera. The architecture of the image statistics subsystem was developed jointly with K. J. Singh.

5-9.1 Parameters of the Image Statistics Subsystem

The image statistics subsystem computes a separate histogram of the red, green, and blue colour component values for each frame. Each histogram consists of four bins defined by five programmable thresholds as shown in Figure 5-39. For the sensor CFA arrangement of Figure 5-6, the maximum possible count for a histogram bin occurs when all 51330 green pixels have the same or similar value. To handle this case the count for each histogram bin is stored in a

16-bit register. The image statistics parameters that correspond to the histogram bins and programmable thresholds are given in Table C-6.

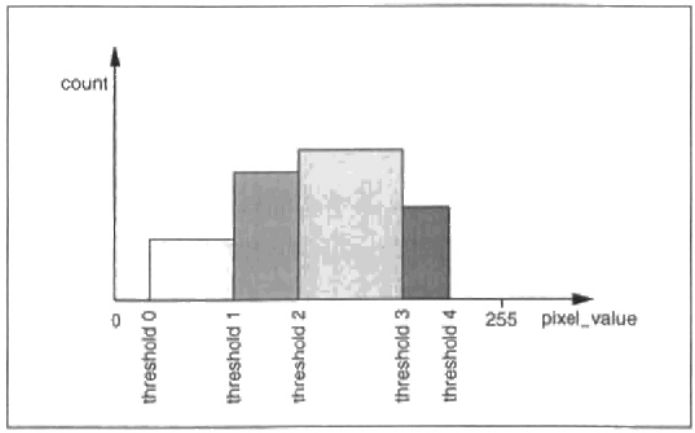


Figure 5-39. Histogram definition used by the image statistics subsystem.

5-9.2 Image Statistics Architecture

The image statistics subsystem has the architecture shown in Figure 5-40. Its operation can be described as follows. At the start of sensor read-out the histogram bins are cleared using the *reset_statistics* signal generated by the sensor FSM. During sensor read-out when the *pixel_valid* flag is set the pixel value from the A/D is compared with the five thresholds. Based on the result of this comparison and the present pixel colour, the appropriate histogram bin is addressed and incremented. At the end of each frame the host can upload the image histograms over the parameter bus.

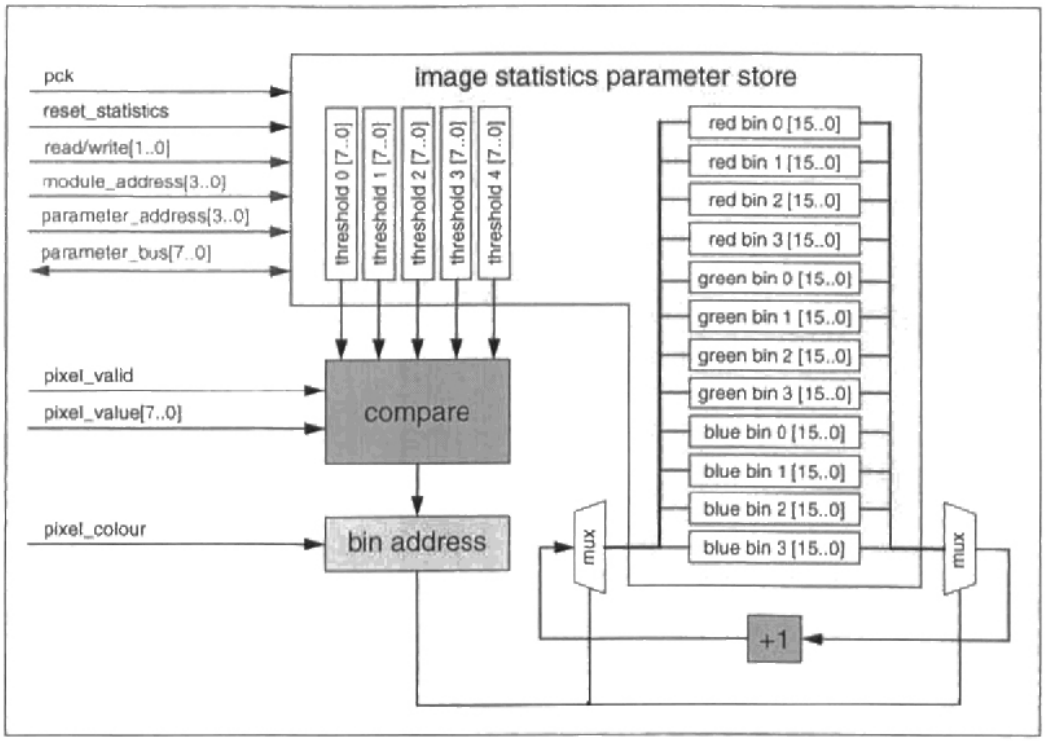


Figure 5-40. Image statistics subsystem architecture.

5-10. Host Interface

All the camera system parameters listed in tables in this chapter can programmed by the host computer through using the signals shown in Figure 5-41. The host interface was developed by the author.

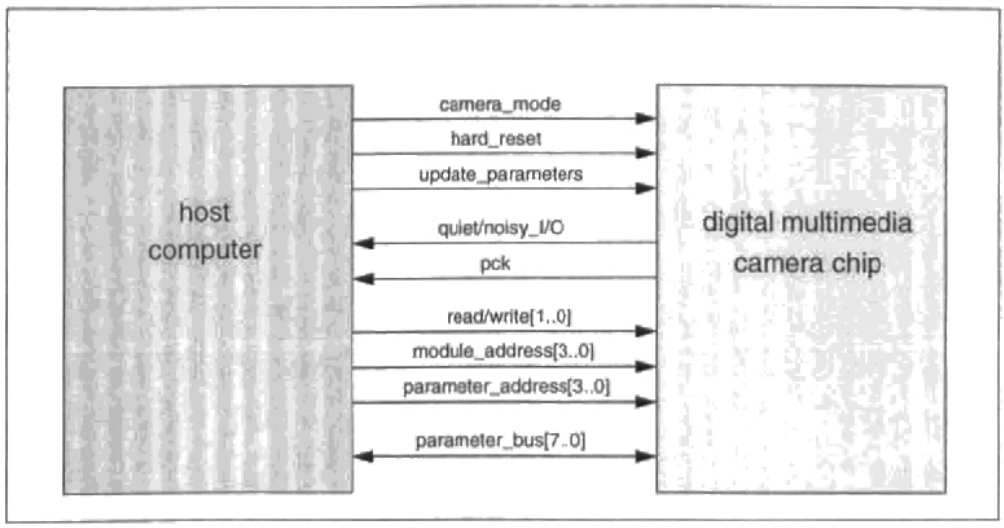


Figure 5-41. Host interface programming model.

5-10.1 Parameter Read and Write Cycles

The host synchronizes all parameter read and write operations to the pixel clock *pck*. The timing diagram for parameter read and write cycles is shown in Figure 5-42. To read a parameter from the camera, the *read/write* signal is set by the host to *10* and the *module_address* and *parameter_address* are established. Once the module and parameter addresses are decoded by the camera, the corresponding parameter value is immediately driven onto the *parameter_bus* by the camera. The host can latch the value on the *parameter_bus* on or before the next rising edge of *pck*. As the maximum rate for *pck* is only $3.39MHz$, the speed requirements of the host or camera are not excessive. To write a parameter to the camera the host sets the *read/write* signal to *11* and establishes the module and parameter addresses, and the parameter value on the *parameter_bus*. The camera latches the value on the *parameter_bus* on the next rising edge of *pck*. The host can suspend parameter I/O by setting *read/write* to the value *00* or *01*.

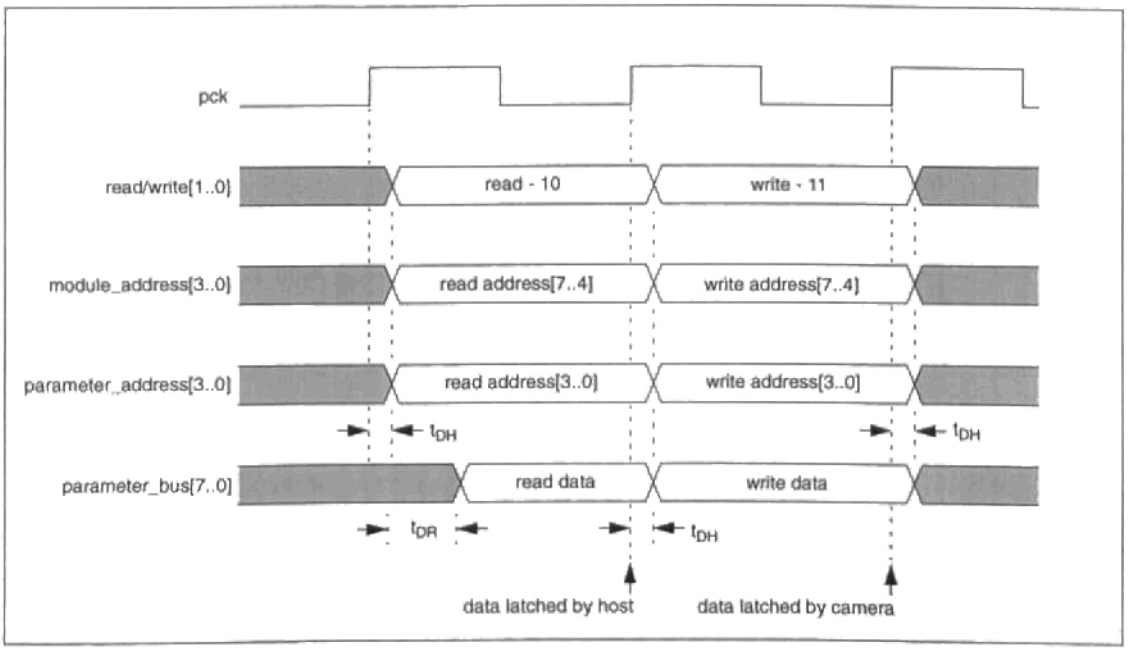


Figure 5-42. Parameter read/write timing diagram. Note that t_{DH} is the time it takes the host to establish data and addresses during read and write operations, and T_{DR} is the time it takes the camera to establish data on the parameter bus during a read operation.

5-10.2 Updating Parameters

All camera parameters are double-buffered [D'Luna and Parulski 1991, Wang et al. 1994]. This allows parameters to be changed at any time during a video frame without introducing "glitches". The parameter double-buffering scheme used with the single-chip camera is illustrated schematically in Figure 5-43. When parameters are written to the camera they are buffered in flip-flops. When the host wishes to make these parameters values active, it holds the *update_parameters* signal high for at least 1 *pck* cycle. This event is detected by the sensor

FSM on the single-chip camera and during the blanking interval at the start of the next frame the active parameters take on their new values. When a parameter is read from the camera, the active value is driven onto the *parameter_bus*. As an alternative method for changing parameters on the single-chip camera, the host can disable video output from the camera by taking the *camera_mode* signal high. This places the camera in program mode. Under these conditions, parameters written to the camera are made active when the *update_parameters* signal is pulsed by the host. To reload the default values into the active and buffered parameter locations the host can pulse the camera *hard_reset* signal. If the camera is in video mode this will also have the effect of restarting the current frame.

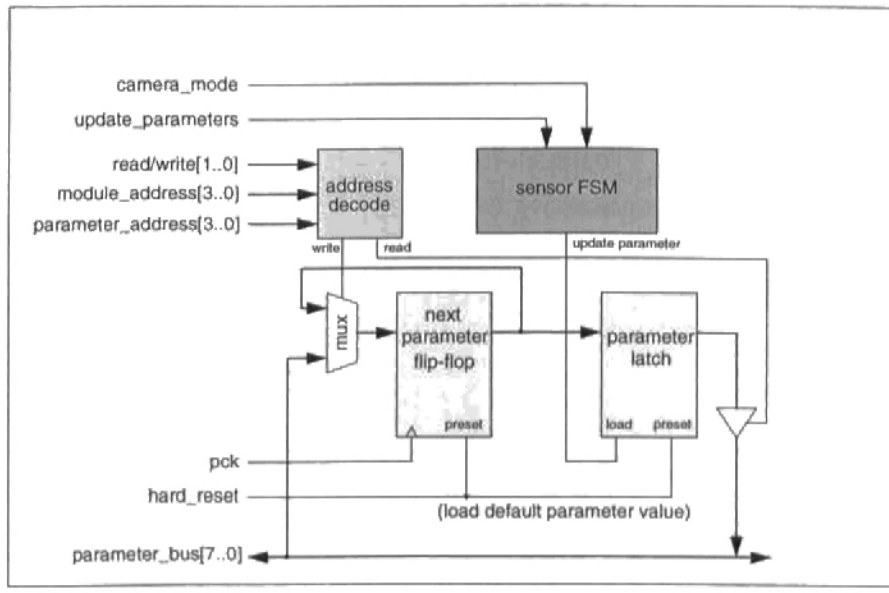


Figure 5-43. Parameter double-buffering scheme used on the camera.

5-10.3 Quiet/Noisy Parameter I/O

While the host can read and write parameter values to the host on any positive edge of *pck*, it can choose to observe the quiet periods defined as part of the switching noise management scheme. As discussed in Section 5-5.2.5, the sensor FSM holds the *quiet/noisy_I/O* signal low during the line blanking interval to inform the host that it should temporarily suspend parameter I/O for quiet operation. At the sub-pixel clock level, all parameter I/O transactions occur on the positive edge of *pck*. Therefore if the camera is configured in quiet mode all parameter I/O transfers that occur when the *quiet/noisy_I/O* signal is high can be considered quiet.

5-11. Camera Implementation

The single-chip camera was fabricated in a Lucent Technologies non-silicided, single-poly, 0.8-μm CMOS process, the same process used to produce the photogate sensor of Chapter 4.

Deposition of the CFA was performed after the completion of the CMOS manufacturing process. The die size is 10.2mm × 10.3mm and contains 740K transistors. A microphotograph of the digital multi-media camera chip prior to the deposition of the CFA is shown in Figure 5-44. The image sensor, PGA, A/D, and SRAM modules were full-custom designed and laid out. The camera digital system consisting of the interpolation, colour correction, image statistics, and control subsystems were synthesized from a VHDL description to a netlist of gates from a standard cell library. Layout of the digital circuits was performed by an automatic place-and-route tool. A breakdown of the area of different modules of the camera is given in Table 5-5.

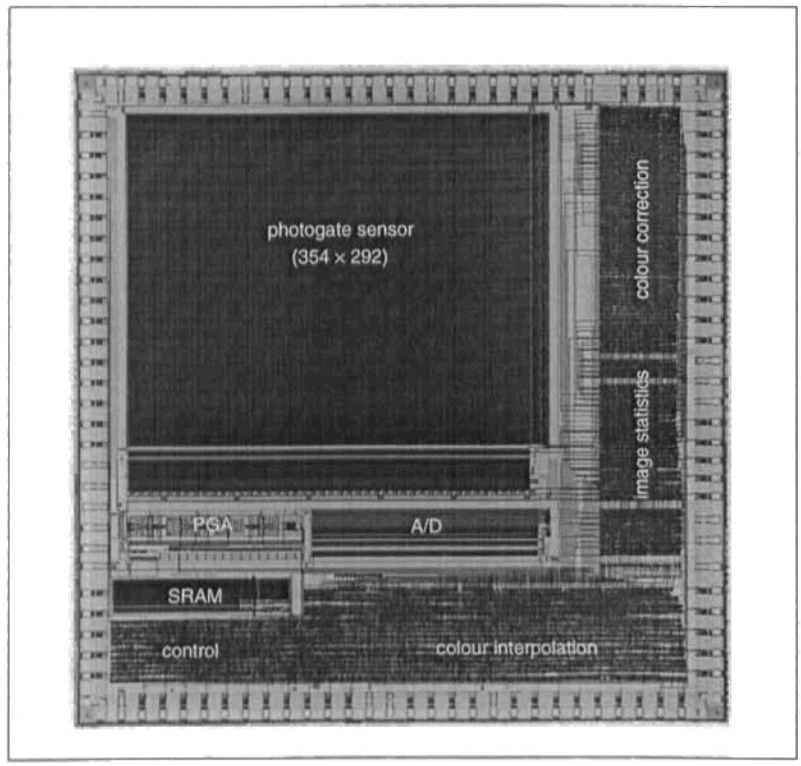


Figure 5-44. Die microphotograph of the single-chip camera prior to the deposition of the CFA. The die dimensions are 10.2mm × 10.3mm.

Module	Area (mm^2)	Percentage of Total Area
Image Sensor	45	42.8%
PGA	1.8	1.7%
A/D	3.6	3.4%
Digital Camera System	37	35.2%

Table 5-5. Chip area usage by camera module.

5-12. Camera Performance

All systems on the single-chip camera were found to operate as designed and a clean colour video image was produced at 30 frames/second when an external clock of $30MHz$ was supplied. The performance of the single-chip camera will now be described in terms of the impact of digital switching noise, the sensor characteristics, and power dissipation.

5-12.1 The Influence of Digital Switching Noise

During the design of the single-chip camera it was anticipated that digital switching noise might degrade the performance of the camera by coupling into sensitive analog circuits via the chip substrate. This led to the development of the switching noise management scheme described in Section 5-5.2 in which the clocks for the on-chip digital systems are suppressed for a number of intervals within each read-out cycle to form "quiet" periods. During the quiet period at the start of each row the analog sampling operations involved with sensor read-out are performed, i.e. the sampling of the reset and signal levels of the pixels in that row. Furthermore, a flag is set to request that the host temporarily suspend parameter I/O operations. During the quiet period within each pixel cycle the analog-to-digital conversion is performed. However, due to the additional timing complexity involved it was not possible to provide quiet periods for the sampling operations of the PGA. To enable the effectiveness of the switching noise management strategy to be evaluated a "noisy" camera mode was also supported which eliminates the quiet period for analog-to-digital conversion, and places no restrictions on parameter I/O. However, contrary to expectations it was found that switching noise did not influence camera system performance in any measurable way, in either quiet or noisy mode.

5-12.1.1 Switching Noise Waveforms

The video image produced by the camera was very clean with no artifacts that could be attributed to switching noise. Changing between quiet and noisy modes only produced a barely perceptible DC intensity shift in the displayed image. Significantly, the temporal noise floor of the sensor, including the noise contributions from the PGA and A/D converter, was measured in both quiet and noisy mode and found to be constant at $7.46mV\ RMS$ referred to the A/D input[1]. Some insight into switching noise present in the single-chip camera can be obtained by inspection of the clock and supply bounce waveforms shown in Figure 5-45. The top three traces are the master clock *fck*, the pixel clock *pck*, and the digital clock *dck*. The lower three traces are the output of the PGA, and the outputs of the digital and analog supply bounce sensors (Figure 5-16). The PGA waveform corresponds to a spatial transition in the image from bright to dark and is free from any spikes or noise components associated with the system

1. Under dark conditions the temporal noise floor was measured as 1.91 ADU RMS, for an A/D input range of 1.0V, a measured PGA gain of 13, and an integration period of 33ms.

clocks. The digital supply bounce waveform shows substantial bounce in *DVdd* that is correlated with *dck* and periodic. The quiet interval is clearly evident. The analog supply bounce waveform is of a much lower magnitude and with two main spikes each *pck* cycle. These spikes are correlated with *ack1* (not shown in Figure 5-45) and correspond to A/D converter sampling operations. The following spike is correlated with *pck* and is due to the column decoders and column amplifiers that transition on *pck*. The remaining noise on the analog supply bounce waveform is of lower magnitude and is due to *dck*.

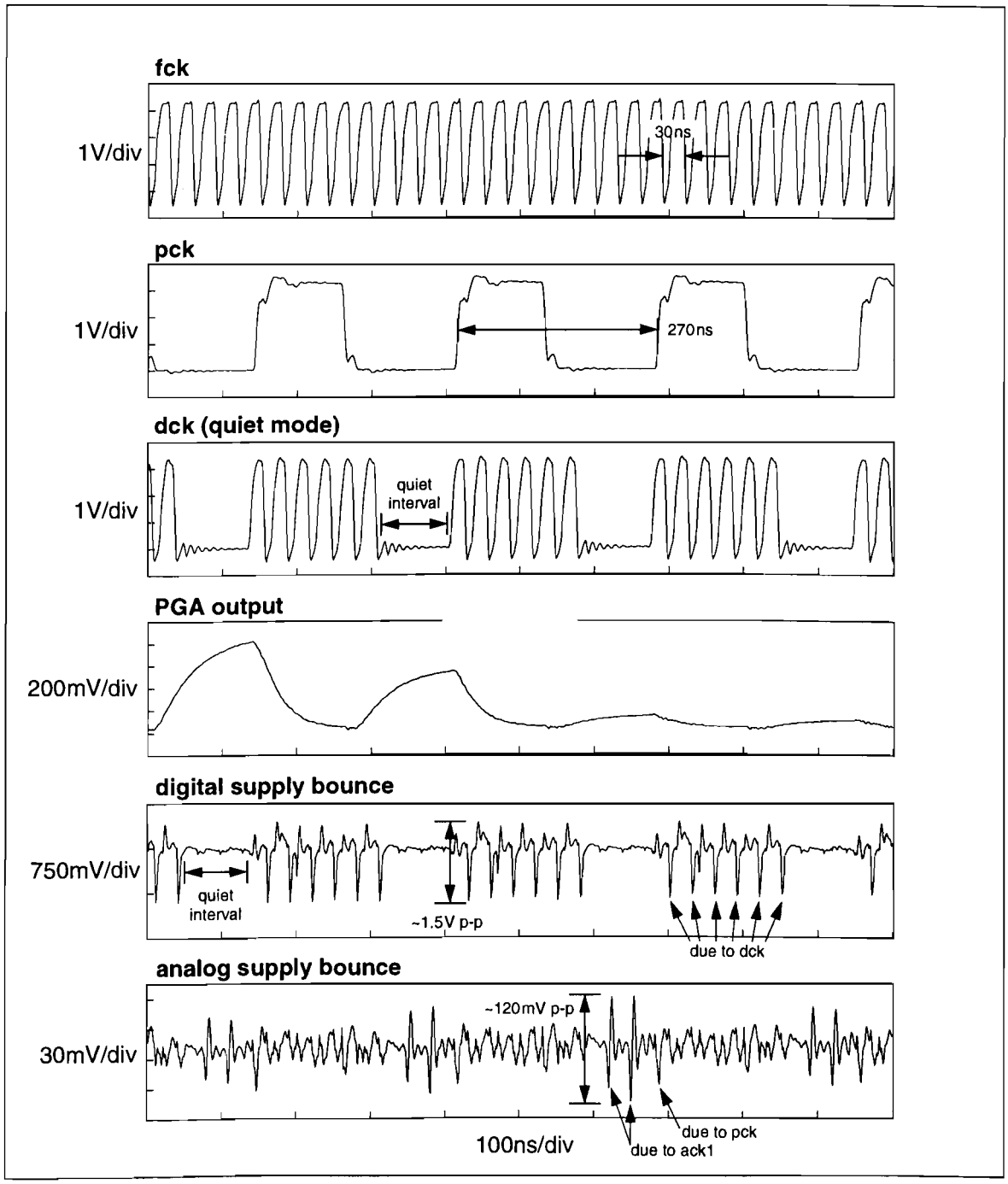


Figure 5-45. Waveforms of the camera clocks, PGA output, and supply bounce sensor outputs.

When the camera is configured in noisy mode the noise contribution from *dck* is shifted in phase and superimposed on the spikes correlated with *ack1* as shown in Figure 5-46. While the analog supply bounce waveform for quiet and noisy mode contains differences, for both modes the waveform is periodic. The highly periodic nature of the analog and digital supply bounce waveforms suggests that switching noise in the single-chip camera is dominated by transitions on the *pck* and *dck* clock trees and is largely data independent. As a consequence the analog circuits in the signal path are uniformly perturbed in the same manner each pixel cycle. Together with the differential architecture of the column circuits and PGA this results in no visible artifacts or measured temporal noise component that can be attributed to switching noise.

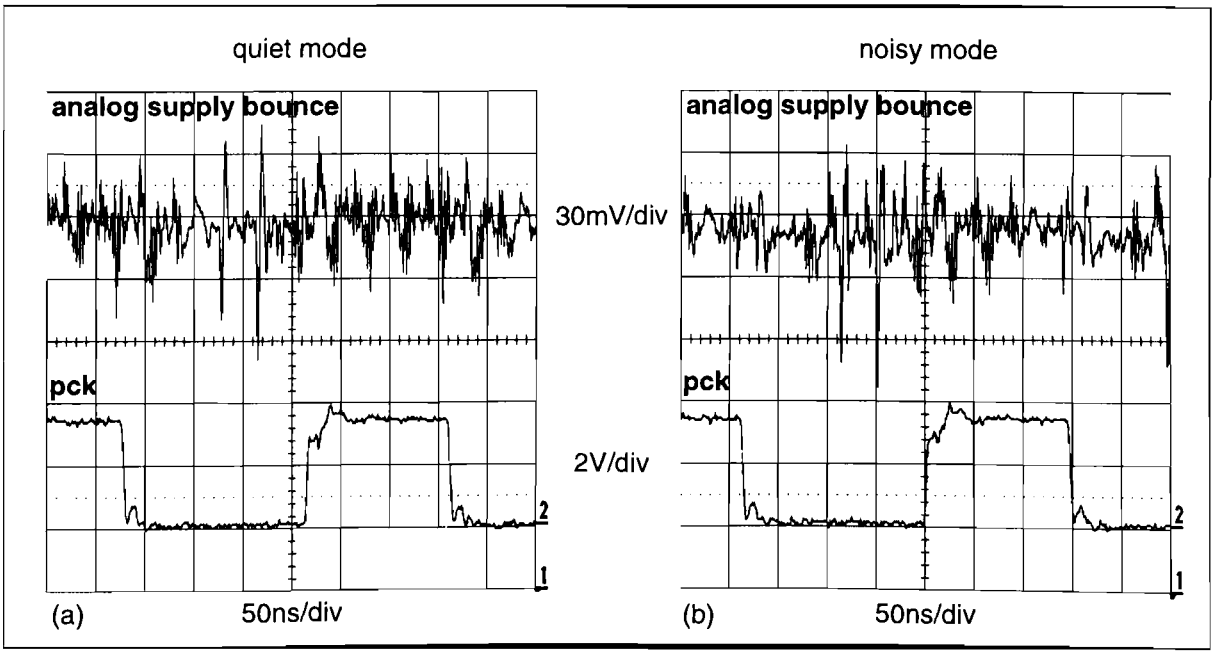


Figure 5-46. Analog supply bounce and pck waveforms in (a) quiet mode (b) noisy mode.

5-12.1.2 Switching Noise and Sensor Read-Out Operations

While the camera quiet/noisy mode can be used to quantify the impact of digital switching noise on PGA and A/D performance, investigating the impact of digital switching noise on the analog sampling operations associated with sensor read-out was more difficult. This is because the digital clock is suppressed during the line blanking period in both quiet and noisy modes. To generate additional digital noise during this interval requires the host performing an "artificial" parameter I/O operation each *pck* cycle. While this avenue was not rigorously pursued during evaluation of the single-chip camera, no image artifacts were observed that could be attributed to parameter I/O operations. Furthermore, it proved possible to account for the temporal noise floor of the sensor without assuming any contribution from digital switching noise.

These results suggests that quiet periods during the analog sampling operations associated with sensor read-out may not be necessary for satisfactory camera performance.

5-12.1.3 Accounting for the Camera Temporal Noise Floor

The temporal noise floor of the sensor can be expressed as:

$$\sigma_{t_{floor}} = \sqrt{\sigma^2_{t_{dark\ shot}} + \sigma^2_{t_{charge\ transfer}} + \sigma^2_{t_{read}} + \sigma^2_{t_{PGA}} + \sigma^2_{t_{A/D}}} \quad Volts\ RMS \tag{5-21}$$

where $\sigma_{t_{dark\ shot}}$ is the dark current shot noise, $\sigma_{t_{charge\ transfer}}$ is the charge transfer noise, $\sigma_{t_{read}}$ is the sensor read noise, $\sigma_{t_{PGA}}$ is the thermal noise of the PGA, and $\sigma_{t_{A/D}}$ is the thermal and quantization noise of the A/D converter. Potentially $\sigma_{t_{read}}$, $\sigma_{t_{PGA}}$, and $\sigma_{t_{A/D}}$ could all contain contributions from digital switching noise and hence be larger than their theoretical estimates. The temporal noise floor $\sigma_{t_{floor}}$ was measured in both quiet and noisy mode for $T_{int} = 33ms$ as $1.91 ADU\ RMS$ for a PGA gain equal of 13, and an A/D input range of $1V$. This gives

$$\sigma_{t_{floor}} = 1.91 \times \frac{1}{256} \times \frac{1}{13} = 573.9\mu V\ RMS \tag{5-22}$$

referred to the sensor output for $T_{int} = 33ms$.

However, when the inputs to the PGA are shorted to ground a value of $1.74 ADU\ RMS$ was obtained for the temporal noise floor. Under these conditions $\sigma_{t_{dark\ shot}}$, $\sigma_{t_{charge\ transfer}}$, and $\sigma_{t_{read}}$ are not measured and the temporal noise floor only contains contributions from $\sigma_{t_{PGA}}$ and $\sigma_{t_{A/D}}$. Hence

$$\sqrt{\sigma^2_{t_{PGA}} + \sigma^2_{t_{A/D}}} = 1.74 \times \frac{1}{256} \times \frac{1}{13} = 522.8\mu V\ RMS \tag{5-23}$$

referred to the sensor output. Subtracting this value in quadrature from (5-22) gives:

$$\sqrt{\sigma^2_{t_{dark\ shot}} + \sigma^2_{t_{charge\ transfer}} + \sigma^2_{t_{read}}} = 236.8\mu V\ RMS \tag{5-24}$$

A theoretical noise analysis of the column circuits by Loinaz gives $\sigma_{t_{read}} \approx 130\mu V\ RMS$ [Loinaz et al. 1998b]. The dark current density J_{dark} for the single-chip camera was measured as $80 pA/cm^2$ and the conversion gain G was found to be $40\mu V/electron$ referred to the sensor output (see Table 5-6). Eqns. (2-19), (2-21), and (2-22) give $\sigma_{t_{dark\ shot}} = 292.5\mu V\ RMS$ where $A_{pixel} = 3.24 \times 10^{-6} cm^2$, and $T_{int} = 33ms$ have been used. Adding the computed values for $\sigma_{t_{read}}$ and $\sigma_{t_{dark\ shot}}$ in quadrature gives $320.1\mu V\ RMS$, greater than the measured value in (5-24) before considering any charge transfer noise contribution[1]. Therefore the tem-

poral noise performance of the sensor can be accounted for without reference to any additional component introduced by digital switching noise.

The combined temporal noise of the PGA and A/D converter in (5-23) can be referred to the PGA output by multiplying by the gain of 13 to give $6.796mV\ RMS$. A theoretical analysis of the PGA architecture by Loinaz gave its thermal noise contribution as $\sigma_{t_{PGA}} \approx 6mV\ RMS$ referred to the PGA output for this value of gain. Subtracting this value in quadrature leaves $3.192mV\ RMS$ which includes the temporal noise of the A/D, and any contribution due to digital switching noise from the PGA or A/D. The theoretical quantization noise for an 8-bit A/D with a $1V$ input range is $1.127mV\ RMS$ computed using (A-11). Subtracting this value in quadrature from $3.192mV\ RMS$ yields $2.986mV\ RMS$ as the temporal noise to be attributed to thermal noise of the A/D, and possibly digital switching noise of the A/D or PGA. This is only $0.76ADU\ RMS$ ($1\ LSB = 3.906mV$), independent of whether the camera is in quiet or noisy mode. While a theoretical estimate of the temporal noise of the A/D is not available, this result suggests that the magnitude of digital switching noise in the PGA or A/D is small relative to the inherent thermal noise of the PGA and A/D. While this analysis does not preclude the existence of a noise component associated with digital switching noise, it does demonstrate that the digital switching noise contribution is small and it does not degrade camera performance in any measurable way.

5-12.2 Sensor Performance

The performance of the on-chip photogate sensor was quantified using the same definitions and techniques developed for the photogate sensor of Chapter 4. However, to characterize the sensor of the single-chip camera the on-chip PGA and A/D were employed rather than external circuits at the board level. The necessary experimental data was obtained by Marc Loinaz of Bell Laboratories, and the analysis was performed jointly with the author. A summary of the performance characteristics of sensor on the single-chip camera is given in Table 5-6 together with the corresponding values for the photogate sensor of Chapter 4.

By consideration of differences in pixel dimensions and read-out circuit architecture it is possible to show that the results presented in Table 5-6 for the single-chip camera are consistent with those of the photogate sensor of Chapter 4. The photogate pixels used in Chapter 4 and Chapter 5 are identical except for a uniform scaling factor. The origin of both pixels was a 20μm × 20μm design that was shrunk by 20% to give the pixel of Chapter 4 with dimensions of 16μm × 16μm, and 10% to give the pixel of Chapter 5 of size 18μm × 18μm. This means

1. Note that as the conversion gain of the single-chip camera is 40μV/electron, the difference between the calculated and measured noise for the sensor only corresponds to 2 electrons RMS referred to the pixel *FD* node.

that any sensor characteristics that is proportional to pixel area can be expected to be different by a factor of $0.9^2/0.8^2 \approx 1.3$.

The gain in the signal path of the two sensors is also different. The photogate sensor of Chapter 4 employed a source follower architecture (Figure 4-1) with a combined gain of 0.4, while the photogate sensor of the single-chip camera (Figure 5-7) employed unity-gain amplifiers to achieve a combined read-out gain of 0.9.

	Photogate Sensor of Chapter 4	**Single-Chip Camera Photogate Sensor**
Pixel Design	Single-poly photogate	Single-poly photogate
Technology	Lucent Technologies 0.8μm CMOS	Lucent Technologies 0.8μm CMOS
Resolution	352 × 288	354 × 292 (inc. two black rows)
Pixel Dimensions	16μm × 16μm	18μm × 18μm
Pixel Fill Factor (drawn active area)	35%	35%
Dark Current Density	183pA/cm^2 at 25°C	80pA/cm^2 at 25°C
Saturation	1.38V (49 K electrons)	1.2V (30 K electrons)
Temporal Noise Floor (30ms int., inc. CDS)	525.1μV RMS	573.9μV RMS (inc. PGA, A/D)
Dynamic Range (30ms int., inc. CDS)	68.4 dB	66.4 dB (inc. PGA, A/D)
Monochrome Sensitivity	4.25V/lux.s	7.0V/lux.s
Colour (without microlenses)	Red 1.30V/lux.s Green 1.12V/lux.s Blue 0.66V/lux.s	Red 1.32V/lux.s Green 1.51V/lux.s Blue 0.91V/lux.s
Conversion Gain	28μV/electron (70μV/electron pixel referred)	40μV/electron (50μV/electron pixel referred)
Fixed-pattern Noise	0.29% p-p of sat.	0.3% p-p of sat.
Supply Voltage	5.0V	3.3V

Table 5-6. Performance comparison between the photogate sensor of Chapter 4, and the photogate sensor integrated as part of the single-chip camera. All quantities unless otherwise stated are referred to the sensor output. The optical sensitivity values were obtained using a 3200K tungsten halogen lamp and colour compensating filter.

5-12.2.1 Conversion Gain

The difference in pixel conversion gain G_{FD} between the photogate sensors can be accounted for in terms of a difference in the capacitance of the pixel floating diffusion node C_{FD}. The capacitance C_{FD} is determined by the parasitic capacitance of the source of device *M2* and the gate of device *M3*. If it is assumed that C_{FD} is dominated by area capacitance rather than peripheral capacitance, it can expected that the ratio of the pixel conversion gain for the sensor of Chapter 4 to that of the single-chip camera will be $1/1.27 \approx 0.8$. From Table 5-6 this ratio is found to be $50/70 \approx 0.7$, close to the predicted ratio. The difference between con-

version gain G referred to the sensor output is accounted for by a combined gain in the signal path of 0.4 for the photogate sensor of Chapter 4, and 0.9 for the photogate sensor of the single-chip camera.

5-12.2.2 Optical Sensitivity

The ratio of the monochrome sensitivities is $7.0/4.25 \approx 1.6$. This can be explained in terms of a conversion gain ratio of $40/28 \approx 1.4$ and a pixel area ratio of 1.3 giving an expected ratio of $1.4 \times 1.3 \approx 1.8$, close to that found in practice. The differences in colour sensitivities are more difficult to account for because colour cross talk is dependent on absolute dimensions, slightly different colour filter characteristics were employed, and there are variations in the implementation of the optical light shields employed by both CFAs. The ratio of the sensitivities of the green and blue pixels is similar at $1.51/1.12 \approx 1.3$ and $0.91/0.66 \approx 1.4$ respectively. Surprisingly however, the sensitivity of the red pixels is virtually the same for both sensors. The author cannot explain this result.

5-12.2.3 Dynamic Range

The saturation level expressed as a voltage for the photogate sensor of Chapter 4 is 15% greater than that of the photogate sensor employed in the single-chip camera because a larger Vdd value was used, and the pixel unity-gain amplifier of the single-chip camera achieves a smaller signal swing than the source follower architecture under the bias conditions used. The difference in sensor conversion gains explains the difference in sensor saturation level expressed in electrons. The temporal noise floors for both sensors are similar, and the dynamic range of the single-chip camera is $2dB$ lower than that of the photogate sensor of Chapter 4.

5-12.2.4 Dark Current Density and Fixed-Pattern Noise

There is a considerable difference in dark current density between the two photogate sensors. This is not unexpected for while both sensors were fabricated in the same process, it is often found that there is significant dark current variation between sensors from different process runs, or even across the same wafer. While the fixed-pattern noise for both sensors is essentially the same expressed as a percentage peak-to-peak of saturation, when expressed in terms of a spatial variation in the number of dark electrons $\sigma_{N_{dark}}$ (see Section 4-4.4.3), the single-chip camera is shown to exhibits lower FPN. Using this measure the FPN of the single-chip camera is 15 *electrons RMS* compared with 23 *electrons RMS* for an integration period of 30ms and at 25°C. This result is consistent with the dark current density of the single-chip camera being substantially lower than that of the photogate sensor of Chapter 4.

5-12.3 Power Dissipation

The total power dissipation of the single-chip camera is 182mW when producing 352 × 288 24-bit RGB image data at 30 frames/second from a 3.3V supply. The power dissipation of different camera modules is given in Table 5-7.

Module	Power Dissipation (mW)	Percentage of Total Power
Image Sensor	20	11.0%
PGA	10	5.5%
A/D	40	22.0%
Camera Digital System	92	50.5%
Pad Frame	20	11.0%

Table 5-7. Chip power dissipation by camera module.

The power dissipation of the digital multi-media camera is very low when compared to other solid-state cameras. Unlike a CCD-based camera system the power dissipation is not dominated by the image sensor and clocking circuits, which for a typical CCD sensor are in the range of 2W to 25W depending on the sensor resolution and frame rate [Takizawa et al. 1983, Itakura et al. 1995]. Instead the camera digital system and A/D modules use the greatest percentage of power. Their contribution could be reduced through the use of alternative low-power architectures [Cho and Gray 1995].

5-13. Conclusion

In this chapter the architecture of the first single-chip CMOS digital colour camera has been described. It features a sophisticated switching noise management scheme and shares camera system functionality with a host computer. The camera was realized as a 740K transistor integrated circuit that produces 24-bit RGB pixel data of 352 × 288 resolution at 30 frames/second. The total power dissipation of the camera is only 182mW from a 3.3V supply. Significantly, camera system integration is achieved without any measurable performance degradation due to digital switching noise. Instead, camera performance is limited by that of the photogate sensor, and the resolution of the A/D converter.

5-13.1 Digital Switching Noise Does Not Limit Camera Performance

A switching noise management strategy was developed for the single-chip camera based on temporally separating analog and digital operations. By suppressing the clock to the camera digital system, "quiet" periods were introduced during analog sampling operations such as sensor read-out and A/D conversion. By also supporting a "noisy" mode of operation it was possible to demonstrate that digital switching noise does not influence camera performance in any

measurable way. Furthermore, the temporal noise floor of the camera can be accounted for in terms of the expected noise contributions from the sensor, PGA, and A/D without any reference to digital switching noise. The relative immunity of the camera from digital switching noise can be attributed to the use of separate analog and digital supplies, employing fully differential architectures in the sensor column circuits and the PGA, with perhaps a minor contribution from the quiet period during the line blanking interval. Despite this result, the need for quiet periods to manage digital switching noise cannot be ruled out if the other camera noise sources were reduced, or if very high A/D resolution was required. For example, a 16-bit A/D on a mixed signal integrated circuit has been reported for which quiet periods were needed to reduce performance degradation due to digital switching noise [Mayes and Chin 1996]. However, as most digital cameras use a 10 or 12-bit A/D converter it is likely that digital switching noise can be managed with separate analog and digital supplies and a differential architecture, without the added complexity of gating the clock to the camera digital system to produce quiet periods. In either case, the results obtained from the single-chip camera demonstrate that it is possible to produce integrated CMOS cameras whose performance is not limited by digital switching noise.

5-13.2 Future Integrated CMOS Cameras

By demonstrating that digital switching noise can be effectively managed at the circuit and system timing level it has been shown that producing a single-chip camera is technically possible. Therefore, the integration level of future digital CMOS colour cameras will be determined by other issues, predominantly economic. For example, while complete camera system integration is desirable to achieve the lowest possible power dissipation, other aspects such as the costs associated with depositing the colour filter array, and sensor packaging and testing may dictate that only partial system integration is optimal. Furthermore, for some applications it may not be possible to achieve complete camera system integration due to the large hardware requirements. For example, it is likely that digital cameras intended for multi-media applications will need to perform significant image compression. As the hardware requirements to implement compression techniques such as JPEG and MPEG are substantial, in the immediate future it will not be possible to integrate such hardware onto a single die with the image sensor and other camera signal processing modules [AVP 1995].

One technical issue that may potentially restrict the level of camera system integration is the need to keep the temperature of the imager as low as possible to minimize dark current. Dark current generation is very temperature dependent, doubling approximately every 8°C [Theuwissen 1995]. Therefore, heat generated from digital circuits on the same die as the imager may increase sensor dark current and reduce performance. While the architecture of the single-chip camera did not allow this effect to be investigated, the measured dark current density

of the camera is considerably lower than that of the corresponding monolithic photogate sensor fabricated in the same CMOS technology (Table 5-6). With present CMOS fabrication technology dark current performance is extremely process dependent, even sensors manufactured in the same process exhibit different dark current characteristics. Until dark current levels in CMOS sensors are reduced and stabilized through management at the technology level, it will be difficult to assess the impact of system integration on camera dark current performance.

Despite a number of reasons why it may be desirable to limit camera system integration, the ability to achieve system integration up to the maximum die size if required will give camera designers greater flexibility than is currently available with CCD technology. This is particularly so with regard to camera miniaturization. Moreover, any level of camera system integration that reduces the total parts count of the corresponding product leads to cost savings that can be passed onto the consumer.

CHAPTER 6 Conclusion

In this thesis the author has identified two important issues concerning the solid-state imaging technology known as CMOS Active Pixel Sensors, firstly the need to establish the fundamental performance limitations of this technology, and secondly to investigate how camera system integration influences imaging performance. Before each of these issues was addressed, prerequisite material was presented in Chapters 2 and 3. In Chapter 2 the principles of solid-state imaging technology were reviewed, the architecture and operation of CCD and CMOS APS image sensors were described, and non-idealities that limit the performance of solid-state image sensors were discussed. In Chapter 3 the requirements for realizing a digital colour camera were detailed, with particular emphasis on the necessary colour processing. In Chapter 4 the fundamental performance limitations of CMOS APS technology were established through the experimental characterization of a state-of-the-art colour CMOS photogate sensor. In Chapter 5 the influence of camera system integration on imaging performance was determined by the development and evaluation of a single-chip CMOS digital colour camera. The significance of all performance results obtained were demonstrated by comparison with data reported for CCD sensors. In the following section the major findings of Chapters 4 and 5 are summarized, and in the final section a number of conclusions regarding the future development of CMOS imaging technology are presented.

6-1. The Performance of CMOS APS Image Sensors

6-1.1 CMOS Sensors Are Primarily Device And Not Circuit Limited

While CMOS APS technology is superior to CCD technology in terms of power dissipation and camera system integration, the image quality obtained from CMOS APS sensors is inferior to that provided by high-end CCD sensors. This was demonstrated through the experimental evaluation of a colour CMOS photogate image sensor. It was found that while there is scope at the circuit level to increase the sensor saturation level and improve gain in the signal path, the

imaging performance of a CMOS sensor is primarily limited at the device level by fixed-pattern noise (FPN), low quantum efficiency, significant pixel cross talk, and incomplete charge transfer within each pixel.

6-1.1.1 Fixed-Pattern Noise

It was shown that using two levels of correlated-double sampling (CDS) it is possible to cancel all sensor FPN due to mismatch in the read-out circuits (Section 4-11). However, under these conditions the FPN performance becomes limited by dark current non-uniformity at low signal levels, and pixel conversion gain non-uniformity at high signal levels. Dark current in CMOS sensors is more than an order of magnitude greater than that found in CCD sensors with surface pinning (Section 4-4). Consequently the FPN performance of CMOS sensors is substantially worse than that of CCDs. Advancements in the FPN performance of CMOS sensors through reduced dark current and greater conversion gain uniformity can only be achieved at the fabrication process level.

6-1.1.2 Quantum Efficiency

The optical sensitivity of CMOS photogate sensors is limited by low quantum efficiency, particularly in the blue portion of the spectrum (Section 4-6 and Section 4-12). When compared to CMOS photodiode sensors and CCD sensors the quantum efficiency of the photogate sensor is a factor of 3 or 4 lower due to absorption in the polysilicon photogate. To significantly improve the optical performance of the photogate sensor would require reducing the thickness of the polysilicon photogate at the fabrication process level.

6-1.1.3 Colorimetric Accuracy

The colorimetric accuracy of CMOS sensors is limited by poor blue response and significant pixel cross talk (Section 4-13). Each of these issues can only be addressed at the fabrication process by increasing the quantum efficiency at short wavelengths, and changing the substrate doping concentration to reduce the diffusion length of minority carriers respectively. Cross talk could also be decreased by introducing channel stops between pixels.

6-1.1.4 Incomplete Charge Transfer

For the single-poly photogate pixel it is not possible to completely transfer all of the electrons collected under the photogate to the pixel floating diffusion node (Section 4-9). This is due to electrons being retained in the depletion region of the source of the pixel transfer device. As a result the single-poly photogate sensor is subject to charge transfer noise and image lag. Complete charge transfer can only be ensured by using alternative pixel designs such as the double-poly photogate pixel, or developing new pixel designs based on pinned photodiodes.

6-1.2 Non-Standard CMOS Is Required For Future Image Sensors

At present the imaging performance of CMOS APS sensors is not competitive with high-end CCD sensors. While satisfactory imaging performance for low-end applications may be attained from sensors manufactured in present generation CMOS fabrication technology, this may not be possible in future generations of CMOS technology due to increased dark current [Wong 1996]. It will therefore be necessary to introduce modifications to a standard CMOS fabrication process to address performance issues such as dark current, conversion gain non-uniformity, quantum efficiency, pixel cross talk, and incomplete charge transfer. It is likely that many techniques developed for CCD image sensors can be used with CMOS APS sensors with only relatively minor modifications to the standard CMOS fabrication process. For example, a CMOS APS sensor with pinned photodiodes to minimize dark current and image lag has already been produced with an additional module to a standard CMOS manufacturing process [Guidash et al. 1997]. Dark current may also be reduced through improved process cleanliness.

6-1.3 Camera Integration Does Not Compromise Performance

Through the development of a single-chip digital colour camera it has been demonstrated that CMOS APS technology can deliver complete camera system integration and extremely low power dissipation. Significantly, it has been shown that this can be achieved without degradation of camera system performance due to the coupling of digital switching noise into sensitive analog circuits via the substrate (Section 5-12.1). The architecture of the single-chip camera allowed the relative phase of the digital and analog system clocks to be varied to produce "quiet" or "noisy" periods in which sensitive analog sampling operations could be performed. It was found that this technique did not change the temporal noise performance of the camera. Instead sufficient immunity to digital switching noise was obtained by using separate analog and digital supplies, and differential architectures for the column circuits and programmable gain amplifier. Fundamentally the performance of the single-chip camera was limited by that of the sensor, and not as a result of integrating the entire camera system onto the same die as the sensor (Section 5-12.2). The ability to integrate camera system functionality in this manner without loss of camera performance provides CMOS APS technology with a significant advantage over CCD technology in terms of reducing power dissipation, the physical size, and potentially the cost of solid-state cameras.

6-2. The Future Of CMOS Imaging Technology

While it has been shown that producing the highest quality colour cameras in standard CMOS is not possible, the future of CMOS imaging technology is still very promising. The CMOS APS architecture is very attractive in terms of its extremely low power dissipation and

compatibility with camera system integration. Having demonstrated that camera system integration can be achieved without performance degradation gives the designer enormous flexibility in reducing the parts count of existing camera systems, and creates exciting new possibilities for camera miniaturization. Furthermore, the ability to cancel all circuit mismatch using correlated-double sampling means that the performance of future generations of CMOS image sensors will be entirely determined by what advanced pixel structures can be produced within a CMOS APS array. This means that ongoing development of CMOS APS technology will focus on what process modifications can be introduced to the CMOS fabrication process to manufacture high performance pixels without altering the behaviour of regular MOS transistors or significantly increasing the cost. As such the emphasis will be on device design rather than circuit design. It can be expected that as CMOS imaging technology matures it will seriously challenge the dominance of CCD technology in many solid-state imaging applications, particularly portable consumer imaging products.

Appendix A Testing Environment for the Photogate Sensor

A-1. The Digital Acquisition System

To enable the experimental characterization of the photogate sensor a circuit board was produced to digitally acquire image data from the sensor. The architecture of the circuit board is given in Figure A-1. The video difference amplifiers (VDA) and sample-and-hold stages (S/H) support two levels of correlated double sampling. The board timing was provided by a digital word generator and an Altera programmable logic device (PLD) generated the row and column addresses for the sensor. The digital image data produced by the board was acquired by a PC with a Matrox digital frame grabber and acquisition software. The analysis of the image data was performed off-line using the MATLAB software package.

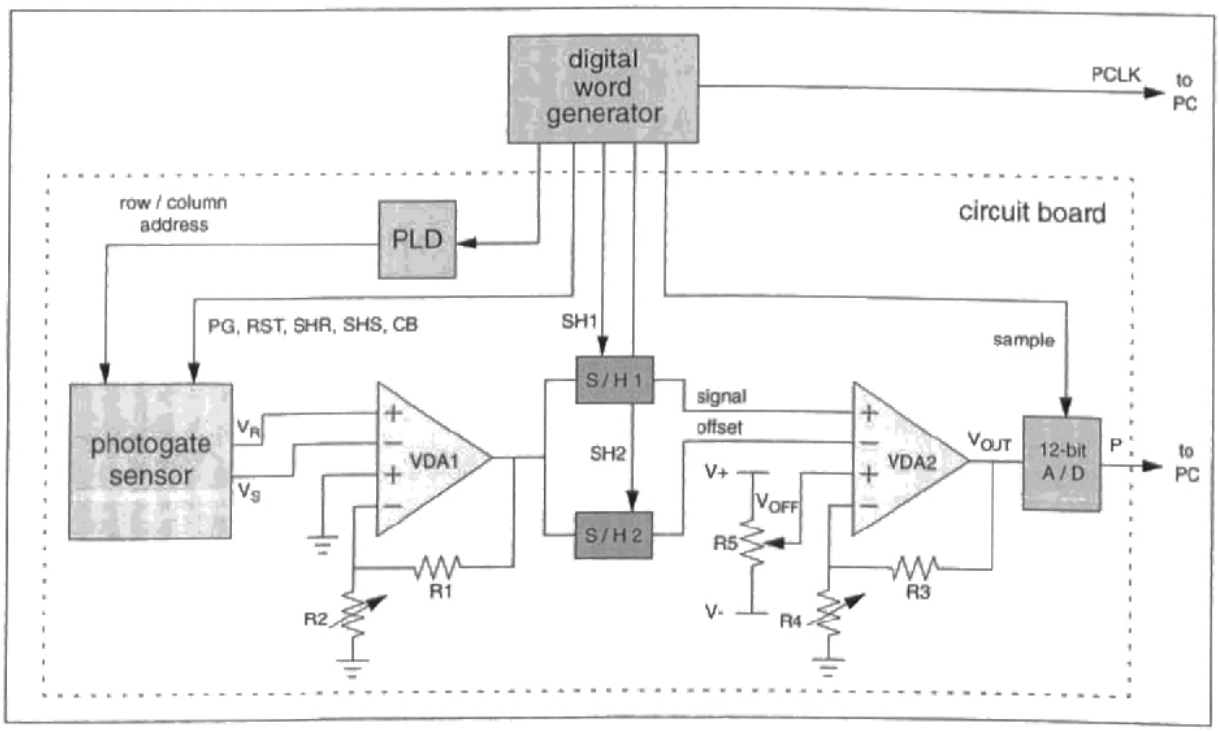


Figure A-1. Photogate sensor circuit board architecture.

A-1.1 Changing the System Gain

At various stages through the course of each measurement it was necessary to change the system gain and offset to ensure that the sensor signal and noise components were maximized with respect to the input range of the analog-to-digital convertor (A/D). This was achieved through the resistor networks *R1-R5*. Resistors *R1-R4* allowed the gain of the first and second

video difference amplifiers to be controlled according to (A-1) and (A-2) respectively. The potentiometer *R5* enabled the offset level of the second differential amplifier V_{OFF} to be adjusted.

$$A_{VDA1} = \frac{R1 + R2}{R2} \tag{A-1}$$

$$A_{VDA2} = \frac{R3 + R4}{R4} \tag{A-2}$$

For the majority of the sensor characterization experiments it was not necessary to perform two levels of correlated double sampling to measure the desired image quantities. Instead only one level of correlated double sampling was used to remove kTC noise and pixel offset mismatch. Consequently most of the experiments were performed with both the sample-and-hold stages and either the first or second video difference amplifier bypassed. The exception to this arrangement was the part of the optical sensitivity experiment discussed in Section 4-11 where the sensor fixed-pattern noise performance was quantified.

A-1.2 Acquiring Frames

Acquisition software on the PC permitted frames of image data from the photogate sensor to be acquired by the PC. To reduce the hard disk storage requirements when acquiring a large number of frames only a 122 × 100 sub-region of each image was actually saved to disk as shown in Figure A-2. By comparison with computations performed using images of full dimension it was possible to to demonstrate that this sub-region contained a sufficient number of pixels to estimate image statistics accurately.

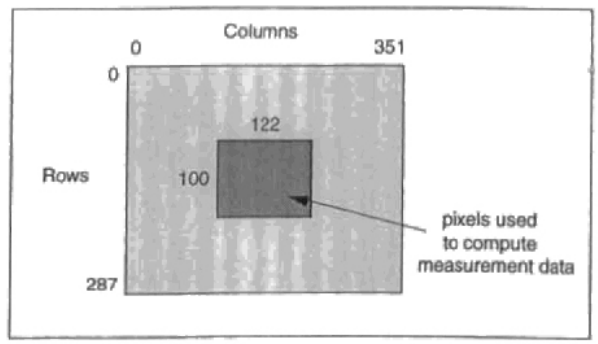


Figure A-2. The sub-region of the sensor image used to compute image statistics.

A-1.3 Referred Quantities

As part of the off-line experimental analysis measurement results were converted from analog-to-digital converter units into equivalent volts referred to the sensor output. The formula

used for converting a given quantity x measured in analog-to-digital converter units (ADU) into equivalent volts referred to the sensor output is given by:

$$x\ Volts = \frac{1}{A_{VDA1}}\left(\frac{x\ ADU}{A_{A/D}A_{VDA2}} - V_{OFF}\right) \tag{A-3}$$

The gain of the video differencing amplifiers A_{VDA1} and A_{VDA2} were found by measuring the resistor values R1-R4 used for a given experiment and applying (A-1) and (A-2) respectively. The gain of the analog-to-digital converter $A_{A/D}$ was computed according to:

$$A_{A/D} = \frac{number\ of\ digital\ levels}{input\ range\ (volts)} \tag{A-4}$$

The analog-to-digital converter on the circuit board was of 12-bit accuracy (4096 digital levels) and an input range of 2V so a value of 2048 was used for $A_{A/D}$.

Unless otherwise stated all measurement results given are expressed as a voltage or RMS voltage referred to the sensor output. However, occasionally it is useful to express measured quantities as an equivalent number of electrons or RMS electrons at the pixel floating diffusion node *FD*. Equation (A-5) is the required transformation where G is the sensor conversion gain.

$$x\ electrons = \frac{x\ Volts}{G} \tag{A-5}$$

A value of $G = 28\mu V/electron$ is used; see justification in Section 4-10.

A-2. Definitions of Performance Measures for the Photogate Sensor

For the photogate sensor the only quantity available for direct measurement is the sensor output voltage. However, a large number of sensor performance measures can be deduced from the mean sensor output voltage, and its temporal and spatial RMS variations.

For each data point in a given experiment a number of frames M were acquired, each of dimension 122×100 as illustrated in Figure A-2. As a preliminary step the mean signal level μ_{ij} for each pixel in the sensor array p_{ij} was estimated by averaging over a statistically significant number of frames M :

$$\mu_{ij} = \frac{1}{M}\sum_{k=1}^{M} p_{ij}(k)\ \ Volts \tag{A-6}$$

where i and j denote the pixel row and column indices and k is the frame number.

The temporal variance of each pixel σ_{ij}^2 was estimated using:

$$\sigma_{ij}^2 = \frac{1}{M-1} \sum_{k=1}^{M} (\mu_{ij} - p_{ij}(k))^2 \quad Volts\ RMS \tag{A-7}$$

A-2.1 Definition: The Mean Signal Level

The *mean signal level* of the sensor μ is defined as the mean of the pixel means μ_{ij} computed using (A-6).

$$\mu = \frac{1}{number\ of\ pixels} \sum_{i}^{rows} \sum_{j}^{columns} \mu_{ij} \quad Volts \tag{A-8}$$

A-2.2 Measuring the RMS Temporal Noise

The measured RMS temporal noise $\sigma_{t_{measured}}$ on the mean signal can be computed by (A-9) as the square root of the mean pixel variances calculated using (A-7).

$$\sigma_{t_{measured}} = \sqrt{\frac{1}{number\ of\ pixels} \sum_{i}^{rows} \sum_{j}^{columns} \sigma_{ij}^2} \quad Volts\ RMS \tag{A-9}$$

The mean signal level of the sensor μ was computed according to (A-8) and the measured RMS temporal noise $\sigma_{t_{measured}}$ was calculated using (A-9). By varying M between 10 and 1000 it was found that 100 frames ($M = 100$) were sufficient to estimate the mean signal level μ and the measured temporal RMS noise $\sigma_{t_{measured}}$ with a high degree of repeatablity to at least 3 significant figures.

However, the measured RMS temporal noise $\sigma_{t_{measured}}$ is not equivalent to the RMS temporal noise produced by the sensor σ_t due to additional noise introduced as part of the acquisition process. Instead $\sigma_{t_{measured}}$ is equal to:

$$\sigma_{t_{measured}} = \sqrt{\sigma_t^2 + \sigma_{t_{read\ CDS}}^2 + \sigma_{t_{A/D}}^2} \quad Volts\ RMS \tag{A-10}$$

where $\sigma_{t_{read\ CDS}}$ is the the temporal read noise of the amplifiers and sample-and-hold stages on the circuit board used to implement correlated-double sampling, $\sigma_{t_{A/D}}$ is the quantization noise of the A/D converter, and σ_t, $\sigma_{t_{read\ CDS}}$, and $\sigma_{t_{A/D}}$ are independent noise sources that add in quadrature.

A-2.3 Quantization Noise

The RMS quantization noise of an analog-to-digital convertor $\sigma_{t_{A/D}}$ is given by:

$$\sigma_{t_{A/D}} = \frac{d}{\sqrt{12}} \quad Volts\ RMS \tag{A-11}$$

where d is the voltage increment of a single digital level [Schrieber 1993].

The A/D that was used had 4096 digital levels (12-bit) and an input range of 2V giving $d = 488.2\mu V$. This yields $\sigma_{t_{A/D}} = 141.0\mu V\,RMS$ referred to the A/D input. Alternatively $\sigma_{t_{A/D}} = 0.2887 ADU\ RMS$ expressed in A/D units at the A/D output.

To ensure that quantization noise did not play a significant role in temporal noise measurements and could be omitted from (A-10), the gains of the video differencing amplifiers $A_{VDA\,1}$ and $A_{VDA\,2}$ were set at the start of each experiment such that the following condition was satisfied:

$$\sigma_{t_{measured}} \gg \sigma_{t_{A/D}} \tag{A-12}$$

A-2.4 Circuit Board Noise

The temporal noise of the video differencing amplifiers and the sample-and-hold stages used to implement correlated-double sampling was considered as a lumped temporal noise component $\sigma_{t_{read\,CDS}}$. To measure $\sigma_{t_{read\,CDS}}$ the photogate sensor chip was removed from the circuit board and the corresponding two inputs to the first video difference amplifier V_R and V_S were shorted to ground. 100 frames of image data were acquired and $\sigma_{t_{measured}}$ determined. If condition (A-12) was satisfied then $\sigma_{t_{read\,CDS}}$ was approximately equal to $\sigma_{t_{measured}}$. As $\sigma_{t_{read\,CDS}}$ was dependent on the gains of the video differencing amplifiers and the system bandwidth it was re-measured in this manner whenever these quantities were changed through the course of an experiment.

A-2.5 Definition: Sensor RMS Temporal Noise

The sensor RMS temporal noise σ_t was defined by re-arranging (A-10):

$$\sigma_t = \sqrt{\sigma^2_{t_{measured}} - \sigma^2_{t_{read\,CDS}}} \quad Volts\ RMS \tag{A-13}$$

where $\sigma_{t_{measured}}$ was computed according to (A-9), and $\sigma_{t_{read\,CDS}}$ was determined using the procedure outlined in Section A-2.4. Any small contribution from $\sigma_{t_{A/D}}$ is also removed from σ_t in this definition as it is implicitly included in the measurement of $\sigma_{t_{read\,CDS}}$.

A-2.6 Fixed-Pattern Noise

The photogate sensor architecture introduced both pixel and column fixed-pattern noise to the image data. To quantify the fixed-pattern noise a composite image F consisting of the 122 $\times$ 100 mean pixel values μ_{ij} as defined by (A-14) was formed.

$$F_{ij} = \mu_{ij} \ \ Volts \tag{A-14}$$

An example image F is shown in Figure A-3 corresponding to a uniform sensor faceplate illumination of 1-lux, an integration period of 30ms, and one level of correlated double sampling.

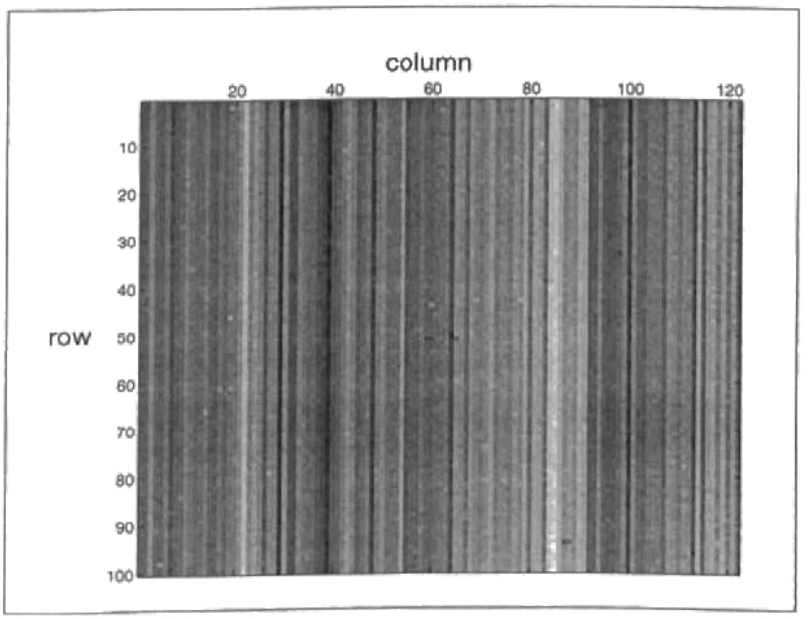


Figure A-3. F for 1-lux faceplate illumination, 30ms integration time, and one level of CDS. To emphasize the fixed-pattern noise the image has been scaled such that the minimum and maximum pixel values correspond to the minimum and maximum available grey levels respectively.

As an intermediate step the variances of the F_{ij} for each row and column of F were computed according to (A-15) and (A-16) respectively where the row and column means are calculated using (A-17) and (A-18).

$$\sigma_i^2 = \frac{1}{number\ of\ columns - 1} \sum_{j}^{columns} (\mu_i - F_{ij})^2 \ \ Volts\ RMS \tag{A-15}$$

$$\sigma_j^2 = \frac{1}{number\ of\ rows - 1} \sum_{i}^{rows} (\mu_j - F_{ij})^2 \ \ Volts\ RMS \tag{A-16}$$

$$\mu_i = \frac{1}{number\ of\ columns} \sum_{j}^{columns} F_{ij} \quad Volts \tag{A-17}$$

$$\mu_j = \frac{1}{number\ of\ rows} \sum_{i}^{rows} F_{ij} \quad Volts \tag{A-18}$$

A-2.7 Preliminary Definition for Pixel and Column Fixed-Pattern Noise

The RMS pixel fixed-pattern noise σ_p was defined as the square root of the mean variance of the columns of F, and the RMS column fixed-pattern noise σ_c was defined as the square root of the mean variance of the rows of F according to:

$$\sigma_p = \sqrt{\frac{1}{122} \sum_{i}^{122} \sigma_i^2} \quad Volts\ RMS \tag{A-19}$$

$$\sigma_c = \sqrt{\frac{1}{100} \sum_{j}^{100} \sigma_j^2} \quad Volts\ RMS \tag{A-20}$$

The RMS pixel fixed-pattern noise σ_p was defined as the square root of the mean variance of the columns of F, and the RMS column fixed-pattern noise σ_c was defined as the square root of the mean variance of the rows of F according to (A-19) and (A-20) respectively.

$$\sigma_p = \sqrt{\frac{1}{number\ of\ columns} \sum_{i}^{columns} \sigma_i^2} \quad Volts\ RMS \tag{A-21}$$

$$\sigma_c = \sqrt{\frac{1}{number\ of\ rows} \sum_{j}^{rows} \sigma_j^2} \quad Volts\ RMS \tag{A-22}$$

A-2.8 Problems with the Preliminary FPN Definitions

However, it was found that (A-21) and (A-22) could not be directly used as the RMS pixel and column FPN definitions of the photogate sensor due to an image artifact introduced during the sensor design. A bus sizing error in the sensor layout gave rise to a gradual voltage drop in the signal across each row and down each column of the fabricated sensor. This trend as illustrated in Figure A-4(a) where column 10 of Figure A-3 is shown plotted. Using (A-21) and (A-22) as the definitions of the pixel and column FPN on the raw F_{ij} values would result in the measured FPN being significantly dependent on the voltage drop along each row and column.

As this image artifact can be removed with correct sizing of the sensor buses, the author believed that its influence should not be included in any FPN calculations.

To remove the gradual drop in signal level across the rows and down the columns of the image F a digital spatial filter was employed. As FPN is predominantly due to random pixel and column offsets it is essentially high frequency in nature. Consequently a digital high pass filter was used to eliminate the low frequency voltage drop from F while leaving the FPN unchanged. Consistent with the classical difference equation description of a digital filter given in (A-23) a 5^{th} order high pass Butterworth filter was designed using the MATLAB software package whose coefficients are presented in (A-24) and (A-25).

$$\begin{aligned} y(n) &= b_1 x(n) + b_2 x(n-1) + \ldots + b_5 x(n-5) \\ &\quad - a_2 y(n-1) - \ldots - a_5 y(n-1) \end{aligned} \tag{A-23}$$

$$b = [0.8159 \ -4.9794 \ 8.1588 \ -8.1588 \ 4.0794 \ -0.8159] \tag{A-24}$$

$$a = [1.0000 \ -4.5934 \ 8.4551 \ -7.7949 \ 3.5989 \ -0.6657] \tag{A-25}$$

The filter coefficients were used in a zero phase forward and reverse digital filtering routine as part of MATLAB to realize a 10^{th} order high pass filter with a spatial cut-off frequency of 2% of the sampling rate. The application of the high pass filter on column 10 of Figure A-3 is illustrated in Figure A-4(b).

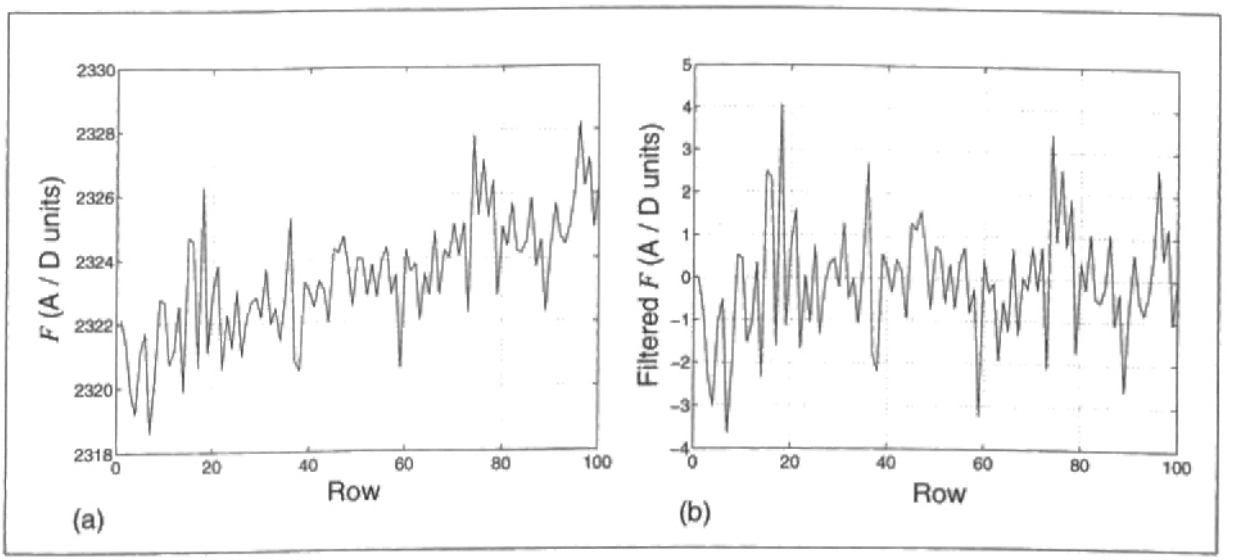


Figure A-4. (a) Column 10 of Figure A-3 (b) Column 10 of Figure A-3 after high pass filtering.

Two new composite images F_R and F_C were generated corresponding to the high pass filtered rows and columns of F respectively. Equation (A-26) and (A-27) describe this operation where *filter* denotes the application of the high pass filter on an image row or column vector.

$$F_{R_j} = filter(F_j) \tag{A-26}$$

$$F_{C_i} = filter(F_i) \tag{A-27}$$

The next step involved computing the spatial column variance of F_C and the spatial row variance of F_R according to (A-28) and (A-29) respectively where the requisite column and row means were determined using (A-30) and (A-31).

$$\sigma^2_{C_i} = \frac{1}{number\ of\ rows - 1} \sum_{j}^{rows} (\mu_{C_i} - F_{C_{ij}})^2 \quad Volts\ RMS \tag{A-28}$$

$$\sigma^2_{R_j} = \frac{1}{number\ of\ columns - 1} \sum_{i}^{columns} (\mu_{R_j} - F_{R_{ij}})^2 \quad Volts\ RMS \tag{A-29}$$

$$\mu_{C_i} = \frac{1}{number\ of\ rows} \sum_{j}^{rows} F_{C_{ij}} \quad Volts \tag{A-30}$$

$$\mu_{R_j} = \frac{1}{number\ of\ columns} \sum_{i}^{columns} F_{R_{ij}} \quad Volts \tag{A-31}$$

A-2.9 Definition: RMS Pixel Fixed-Pattern Noise

The RMS pixel fixed-pattern noise σ_p was defined as the square root of the mean variance of the columns of F_C according to:

$$\sigma_p = \sqrt{\frac{1}{number\ of\ columns} \sum_{i}^{columns} \sigma^2_{C_i}} \quad Volts\ RMS \tag{A-32}$$

A-2.10 Definition: RMS Column Fixed-Pattern Noise

The RMS column fixed-pattern noise σ_c was defined as the square root of the mean variance of the rows of F_R according to:

$$\sigma_c = \sqrt{\frac{1}{number\ of\ rows} \sum_{j}^{rows} \sigma^2_{R_j}} \quad Volts\ RMS \tag{A-33}$$

A-2.11 Definitions: FPN as a Percentage of Saturation Peak-to-Peak

The pixel and column FPN defined as a percentage of saturation peak-to-peak were computed using:

$$Pixel\ FPN\ \%\ sat.\ p\text{-}p\ = \frac{6\sigma_p}{\mu_{sat}} \times 100\% \tag{A-34}$$

$$Column\ FPN\ \%\ sat.\ p\text{-}p\ = \frac{6\sigma_c}{\mu_{sat}} \times 100\% \tag{A-35}$$

Appendix B Colorimetric Data and Methods for the Photogate Sensor

B-1. Measured Tristimulus Values for the Macbeth ColorChecker

A Minolta CR-110 Chroma Meter and DP-100 Data Processor were used to measure the luminous reflectance values Y and chromaticity coordinates (x, y) for each of the colour samples of the Macbeth ColorChecker with a D_{65} illuminant. For each colour sample a number of measurements were performed and the results averaged. Using (3-12) the CIE *(X, Y, Z)* tristimulus values for the colour samples were found. The matrix given in (4-62) was then applied to find the NTSC *(R, G, B)* tristimulus values for the colour samples. The mean *(X, Y, Z)* and NTSC *(R, G, B)* tristimulus values for the colour samples of the Macbeth ColorChecker are given in Table B-1.

Sample	Name	X	Y	Z	R	G	B
1	dark skin	11.03	9.88	6.09	36.92	21.54	13.78
2	light skin	35.71	33.18	24.37	114.26	75.35	55.88
3	blue sky	16.37	17.47	31.57	33.76	44.29	75.97
4	foliage	9.73	12.68	6.78	25.94	38.51	14.38
5	blue flower	23.43	22.03	41.28	55.46	48.96	99.92
6	bluish green	28.42	38.31	42.61	56.71	117.17	98.69
7	orange	34.23	28.35	4.95	128.31	56.43	8.60
8	purplish blue	11.84	10.40	33.08	19.80	20.27	81.35
9	moderate red	26.43	18.30	12.49	97.53	25.23	29.54
10	purple	7.76	6.06	13.02	20.60	10.14	31.86
11	yellow green	29.55	38.79	10.21	86.26	119.05	17.57
12	orange yellow	40.77	38.92	6.72	144.98	92.63	10.62
13	blue	7.32	5.14	27.33	8.83	5.68	67.94
14	green	12.71	20.71	8.88	28.05	70.79	17.48
15	red	19.10	11.54	4.52	76.24	10.22	10.62
16	yellow	52.91	56.92	9.60	178.5	151.8	13.86
17	magenta	21.85	16.94	28.01	64.71	28.57	68.11
18	cyan	11.84	15.48	34.33	11.78	45.27	82.79
19	white	70.58	74.75	79.82	189.11	192.00	186.71
20	neutral 8	47.07	49.83	49.83	125.65	127.91	126.13
21	neutral 6.5	29.36	31.15	33.63	78.26	80.12	78.71
22	neutral 5	15.28	16.17	17.43	40.84	41.50	40.81
23	neutral 3.5	7.02	7.50	8.18	18.55	19.40	19.15
24	black	2.89	3.06	3.33	7.69	7.86	7.79

Table B-1. The mean (X, Y, Z) tristimulus values for the 24 samples of the Macbeth ColorChecker colour rendition chart normalized to 100. The corresponding NTSC (R, G, B) tristimulus values normalized to 255.

B-2. Acquired Tristimulus Values for the Macbeth ColorChecker

An image of the Macbeth ColorChecker colour rendition chart was acquired by the colour photogate image sensor under D_{65} illumination using the experimental arrangement of Figure 4-43. The aperture on the lens assembly was $f/2.0$ and the integration period of the photogate sensor was 90ms. The image was interpolated and for each colour sample of the chart, sub-regions of 30 × 30 pixels were averaged to yield the mean tristimulus values $(R_{int}, G_{int}, B_{int})$ for each sample. The mean $(R_{int}, G_{int}, B_{int})$ values were normalized to 255 and are given in Table B-2..

Sample	Name	R_{int}	G_{int}	B_{int}
1	dark skin	41	32	30
2	light skin	112	88	82
3	blue sky	43	49	59
4	foliage	39	43	36
5	blue flower	68	66	81
6	bluish green	70	98	99
7	orange	109	65	48
8	purplish blue	31	36	54
9	moderate red	96	53	53
10	purple	36	31	36
11	yellow green	101	105	76
12	orange yellow	135	92	65
13	blue	18	22	39
14	green	46	63	49
15	red	86	44	43
16	yellow	189	151	111
17	magenta	99	62	72
18	cyan	31	56	74
19	white	206	202	207
20	neutral 8	150	144	148
21	neutral 6.5	98	95	95
22	neutral 5	56	54	53
23	neutral 3.5	27	26	25
24	black	14	13	12

Table B-2. The mean (R_{int}, G_{int}, B_{int}) tristimulus values for the 24 samples of the Macbeth ColorChecker colour rendition chart acquired by the colour photogate sensor and normalized to 255. The relative gains of the red, green, and blue pixel values were set to achieve an approximate white balance.

B-3. The Least-Squares Method

An analytical solution to the MSE in the CIE *XYZ* colour space was found using the least-squares method. The least-squares method is best expressed using matrices.

Let A be a 24×3 matrix whose rows contain the $(R_{int}, G_{int}, B_{int})$ interpolated tristimulus values from the colour photogate sensor given in Table B-2, and B be a 24×3 matrix whose rows contain the actual (X, Y, Z) tristimulus values for the colour samples given in Table B-1. An estimate of B, denoted $\hat{B}$, found by application of the matrix $\boldsymbol{H}$ can be computed using:

$$\hat{B} = A\boldsymbol{X} \tag{6-1}$$

through the introduction of a new variable $\boldsymbol{X} = \boldsymbol{H}^T$.

If the difference between B and $\hat{B}$ is defined as:

$$E = B - \hat{B} \tag{6-2}$$

then the objective function $f(\boldsymbol{X})$ for the MSE can be written:

$$f(\boldsymbol{X}) = E^T E \tag{6-3}$$

Substituting (6-2) and expanding using (6-1) yields:

$$f(\boldsymbol{X}) = B^T B - B^T A X - X^T A^T B + X^T A^T A X \tag{6-4}$$

Differentiating with respect to $\boldsymbol{X}$ and equating to zero to find the minimum yields:

$$\boldsymbol{X} = \left(A^T A\right)^{-1} A^T B \tag{6-5}$$

which can be solved by recognizing that $\left(A^T A\right)^{-1} A^T$ is the pseudo-inverse of matrix A which can be efficiently computed using the standard value decomposition [Golub and Van Loan 1996].

B-4. The Conjugate Gradient Method

The numerical optimization method used to minimize the RMS colour difference in the CIE $L^*u^*v^*$ colour space $(\Delta E^*_{uv})_{RMS}$ was the conjugate gradient algorithm [Chong and Zak 1996].

B-4.1 Formulating the Problem

As with the least-squared algorithm it is helpful to reformulate the conjugate gradient algorithm using matrices. The same definitions for A, B, $\hat{B}$, and X can be used. By transforming the respective rows of B and $\hat{B}$ to the CIELUV colour space the corresponding matrices B_{Luv} and $\hat{B}_{Luv}$ are obtained. If the element-by-element difference of these two matrices is given by:

$$E = B_{Luv} - \hat{B}_{Luv} \tag{B-1}$$

then the RMS colour difference can be computed according to:

$$f(X) = \sqrt{\sum_{(rows,\, columns)} E^{\wedge 2}} \tag{B-2}$$

where the $\wedge 2$ denotes the square of each matrix element and the summation is performed over the rows and columns of $E^{\wedge 2}$. $f(X)$ is the objective or cost function to be minimized by the conjugate gradient algorithm.

B-4.2 The Conjugate Gradient Algorithm

The formulation of the conjugate gradient algorithm used by the author can be described as follows:

1. Set the iteration count k to 0. Select an initial value X_0.
2. Compute the gradient of the cost function $G_0 = \nabla f(X_0)$. Set the initial direction equal to the negative gradient, $D_0 = -G_0$.
3. Perform a numerical line search to find a positive scalar α that minimizes $f(X_0 + \alpha D_0)$, or more generally $\alpha_k = argmin_{\alpha \geq 0} f(X_k + \alpha D_k)$. The line search routine is described in Section B-4.3.

   If the line search fails set $D_k = -G_k$ and $\alpha = 1.0$.
4. Calculate the next value for X using $X_{k+1} = X_k + \alpha_k D_k$.
5. Re-compute the gradient of the cost function $G_{k+1} = \nabla f(X_{k+1})$.

6. Calculate a convergence or stopping criteria. For example if $\|G_{k+1}\| < \varepsilon$ then stop, where ε is a very small positive constant.

7. Compute the Hestenes-Stiefel formula $\beta_k = \dfrac{G_{k+1}^T (G_{k+1} - G_k)}{D_k^T (G_{k+1} - G_k)}$. Note that for this formula to produce a scalar, the matrices G_{k+1}, G_k, and D_k must be first expressed as vectors. For example:

$$G_k = \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{21} & g_{22} & g_{23} \\ g_{31} & g_{32} & g_{33} \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & g_{13} & g_{21} & g_{22} & g_{23} & g_{31} & g_{32} & g_{33} \end{bmatrix}^T$$

8. Determine the next direction according to $D_{k+1} = -G_k + \beta_k D_k$. Every few iterations re-initialize the direction to the negative gradient instead, i.e. $D_{k+1} = -G_{k+1}$.

9. $k = k + 1$, go to step 3.

B-4.3 The Line Search Routine

The line search algorithm used with the conjugate gradient method is due to Dennis and Schnabel [Dennis and Schnabel 1989]. As with the Hestenes-Stiefel formula it is necessary to express all matrix quantities as vectors for the line search algorithm to operate correctly. The pseudo-code for the line search algorithm is as follows:

```
Initialize α = 1.0, α_low = 0.0, α_up = ∞, done = false.
While not(done) loop
  If f(X_k + αD_k) < f(X_k) + k_1 ∇f(X_k)^T αD_k then
    If ∇f(X_k + αD_k)^T αD_k ≥ k_2 ∇f(X_k)^T αD_k then
      done = true
    Else
      α_low = α
      If α_up = ∞ then
        α = 2α
      Else
        α = refine(α, α_low, α_up)
      End If
```

```
    Else
      α_up = α
      If α_low = 0 then
```

$$\alpha_m = \frac{-\alpha^2 \nabla f(X_k)^T D_k}{2\left(f(X_k + \alpha D_k) - f(X_k) - \alpha \nabla f(X_k)^T D_k\right)}$$

```
        α = max(α_m, c_1 α)
      Else
        α = refine(α, α_low, α_up)
      End If
    End If
  End Loop
```

If after 100 iterations of the loop the conditions necessary to satsify *done* had not been reached, the line search routine was deemed to have failed.

B-4.4 The Function *refine*

The function *refine* used by the line search routine is given by the following pseudo-code:

```
Function refine
  Begin
    δ = α_up − α_low
    X_low = X_k + α_low D_k
    X_up = X_k + α_up D_k
```

$$\alpha_m = \alpha_{low} - \frac{\delta^2 \nabla f(X_{low})^T D_k}{2\left(f(X_{up}) - f(X_{low}) - \delta \nabla f(X_{low})^T D_k\right)}$$

```
    α = min(max(α_m, α_low + c_2 δ), α_up − c_2 δ)
    Return α
End
```

B-4.5 Values Used for the Constants

The values used for the constants in the line search algorithm were $k_1 = 0.0001$, $k_2 = 0.8$, $c_1 = 0.1$, and $c_2 = 0.2$.

B-5. The $L^*u^*v^*$ Colour Difference Errors after Colour Correction

To quantify the colour error for each sample of the Macbeth ColorChecker after the application of the colour correction matrix, the $(\Delta L^*, \Delta u^*, \Delta v^*)$ colour difference errors were computed. This calculation was performed for the optimal colour correction matrices determined by minimizing the MSE_{XYZ} and $(\Delta E^*_{uv})_{RMS}$ colour error metrics respectively and the data is listed in Table B-3.

		Colour Error Metric MSE_{XYZ}				Colour Error Metric $(\Delta E^*_{uv})_{RMS}$			
Sample	Name	ΔL^*	Δu^*	Δv^*	ΔE^*_{uv}	ΔL^*	Δu^*	Δv^*	ΔE^*_{uv}
1	dark skin	0.31	6.32	7.83	10.07	0.91	6.05	7.04	9.33
2	light skin	1.35	5.82	0.25	5.97	1.53	6.31	0.73	6.53
3	blue sky	3.37	-0.79	0.10	3.46	2.67	-0.88	-0.70	2.89
4	foliage	-2.39	-0.54	1.97	3.14	-2.64	0.50	1.55	3.11
5	blue flower	1.20	0.43	-2.78	3.05	0.65	0.30	-3.15	3.23
6	bluish green	3.06	-1.30	2.94	4.44	1.73	-1.01	2.94	3.56
7	orange	4.11	2.94	-3.87	6.36	5.40	0.73	-5.48	7.73
8	purplish blue	2.27	1.83	-0.23	2.93	1.50	1.13	-1.35	2.31
9	moderate red	0.67	5.60	5.73	8.04	2.16	2.22	5.99	6.74
10	purple	-5.65	2.67	-6.34	8.90	-5.40	2.32	-6.81	9.0
11	yellow green	-0.94	-3.42	-1.59	3.88	-1.41	-1.32	-0.33	1.96
12	orange yellow	2.73	-3.58	-6.95	8.28	3.53	-3.49	-7.62	9.10
13	blue	3.70	2.71	-2.68	5.31	3.03	1.88	-3.19	4.79
14	green	-1.95	-5.06	1.89	5.74	-2.74	-3.85	2.46	5.33
15	red	-4.34	14.37	10.02	18.04	-2.49	9.39	9.91	13.88
16	yellow	-1.15	-1.84	2.71	3.47	-0.98	-0.04	3.66	3.79
17	magenta	-3.81	-20.74	-7.28	22.31	-2.93	-22.43	-6.44	23.52
18	cyan	-1.50	2.77	8.21	8.79	-3.14	1.91	6.34	7.33
19	white	0.49	2.70	0.19	2.75	-0.41	3.69	1.14	3.88
20	neutral 8	-1.16	-0.75	0.46	1.46	-1.85	0.07	1.14	2.18
21	neutral 6.5	-1.89	0.05	-3.78	4.22	-2.40	0.81	-3.40	4.25
22	neutral 5	-2.22	-0.22	-3.89	4.48	-2.44	0.35	-4.07	4.76
23	neutral 3.5	0.50	-1.36	-1.49	2.08	0.77	-1.09	-2.57	2.90
24	black	3.19	-2.99	1.55	4.64	4.53	-3.25	-0.73	5.62

Table B-3. The CIE $L^*u^*v^*$ colour difference errors for the samples of the Macbeth ColorChecker after the application of the colour correction matrices determined by minimizing the MSE in the CIE *XYZ* colour space using the least squares method, and by minimizing the RMS $L^*u^*v^*$ colour difference with the conjugate gradient method. The samples with the two largest colour difference errors have been highlighted.

Appendix C Parameters of the Integrated Digital Colour Camera

C-1. Camera System Control Parameters

C-1.1 Camera Control Parameters Set 1.

parameter_address[3..0]	Description	Default Value
0000	configuration word	00000000
0001	clock division factor [1..0] 00 - divide clock by 1 01 - divide clock by 2 10 - divide clock by 4 11 - divide clock by 8	00
0010	reset row offset [7..0]	00100011
0011	reset row offset [8]	1
0100	region-of-interest row start [7..0]	00000001
0101	region-of-interest row start [8]	0
0110	region-of-interest column start [7..0]	00000001
0111	region-of-interest column start [8]	0
1000	region-of-interest row finish [7..0]	00100000
1001	region-of-interest row finish [8]	1
1010	region-of-interest column finish [7..0]	01100000
1011	region-of-interest column finish [8]	1
1100	frame enable front porch [7..0]	00000001
1101	frame enable front porch [15..8]	00000000
1110	frame offset [7..0]	00000110
1111	frame offset [15..8]	00000011

Table C-1. Camera control parameters 1. The module_address[3..0] is 0000. The camera configuration word is defined in Section C-1.2.

C-1.2 Camera Configuration Word

Bit	Description	Default Value
0	quiet/noisy mode 0 - quiet 1 - noisy	0 (quiet)
[1..2]	mosaic pattern 00 - GRBG 01 - RGGB 10 - BGGR 11 - GBRG	00 (GRBG)
3	window type mode 0 - internal 1 - external	0 (internal)
4	input mode 0 - A / D 1 - external test input	0 (A / D)
[5..6]	output mode 00 - A / D, final FIFO value 01 - interpolation 10 - colour correction	00 (A / D, final FIFO value)
7	electronic shutter enable	0 (disabled)

Table C-2. Camera configuration word. The module_address[3..0] and parameter_address[3..0] are both 0000.

C-1.3 Camera Control Parameters Set 2

parameter_address[3..0]	Description	Default Value
0000	input latency [3..0]	0010 (A / D and PGA)
0001	black offset correction enable [0]	1 (enabled)
0010	crowbar enable [0]	1 (enabled)
0011	PGA red coefficient 1 [2..0]	000
0100	PGA red coefficient 2[2..0]	000
0101	PGA green coefficient 1 [2..0]	000
0110	PGA green coefficient 2[2..0]	000
0111	PGA blue coefficient 1 [2..0]	000
1000	PGA blue coefficient 2[2..0]	000

Table C-3. Camera control parameters 2. The module_address[3..0] is 0001.

C-2. Interpolation Coefficients

parameter_address [3..0]	Description	Default Interpolation Coefficients (module_address[3..0])		
		Red (0101)	Green (0110)	Blue (0111)
0000	common exponent [3..0]	0011	0011	0011
0001	coefficient 1 mantissa [5..0]	000010	000001	000010
0010	coefficient 2 mantissa [5..0]	000100	000010	000100
0011	coefficient 3 mantissa [5..0]	000010	000001	000010
0100	coefficient 4 mantissa [5..0]	000100	000010	000100
0101	coefficient 5 mantissa [5..0]	001000	000100	001000
0110	coefficient 6 mantissa [5..0]	000100	000010	000100
0111	coefficient 7 mantissa [5..0]	000010	000001	000010
1000	coefficient 8 mantissa [5..0]	000100	000010	000100
1001	coefficient 9 mantissa [5..0]	000010	000001	000010

Table C-4. Interpolation coefficient parameters. The numbering of the coefficients is consistent with Figure 5-29(a). The default values correspond to the interpolation filter kernels given in (5-10).

C-3. Colour Correction Coefficients

C-3.1 Colour Correction Coefficients Parameters

parameter_address [3..0]	Description	Default Value
0000	c_{11}	010000 10
0001	c_{12}	000000 10
0010	c_{13}	000000 10
0011	c_{21}	000000 10
0100	c_{22}	010000 10
0101	c_{23}	000000 10
0110	c_{31}	000000 10
0111	c_{32}	000000 10
1000	c_{33}	010000 10
1001	pre $offset_R$	00000000
1010	pre $offset_G$	00000000
1011	pre $offset_B$	00000000
1100	post $offset_R$	00000000
1101	post $offset_G$	00000000
1110	post $offset_B$	00000000

Table C-5. Colour correction coefficient parameters. The module_address[3..0] is 1001

C-3.2 Finding and Representing Colour Correction Coefficients

The optimal colour correction coefficients and offsets would typically be determined off-line by the host using a procedure similar to that described in Section 4-13.2. Such an optimization procedure would be realized using floating point arithmetic and hence the coefficients and offsets are found with floating point precision. A method is therefore required to compute

their closest value in the representation implemented in the colour correction subsystem described in Section 5-8.1. The pseudo-code for such an algorithm is as follows:

Starting with each coefficient c_{ij} in floating-point format:

```
If (c_ij ≥ -32/32) and (c_ij ≤ 31/32) then
   exponent = 3
   mantissa = round(32 × c_ij)
Else if (c_ij ≥ -32/16) and (c_ij ≤ 31/16) then
   exponent = 2
   mantissa = round(16 × c_ij)
Else if (c_ij ≥ -32/8) and (c_ij ≤ 31/8) then
   exponent = 1
   mantissa = round(8 × c_ij)
Else if (c_ij ≥ -32/4) and (c_ij ≤ 31/4) then
   exponent = 0
   mantissa = round(4 × c_ij)
Else
  Error : cannot represent c_ij
End if
```

where *round* performs a rounding operation to the nearest integer.

Once the integers *mantissa* and *exponent* have been found using this method they must be converted to a two's complement binary and an unsigned binary representation respectively.

As an example, using this method to find the closest representation of $c_{11} = 1.1731$ gives $exponent = 2$ and $mantissa = 19$, and yields the coefficient *010011 10*.

C-4. Parameters of the Image Statistics Subsystem

parameter_address[3..0] (module_address[3..0])	Description	parameter_address[3..0] (module_address[3..0])	Description (Default Value)
0 (0010)	red bin 0 [7..0]	0 (0011)	blue bin 0 [7..0]
1	red bin 0 [15..8]	1	blue bin 0 [15..8]
2	red bin 1 [7..0]	2	blue bin 1 [7..0]
3	red bin 1 [15..8]	3	blue bin 1 [15..8]
4	red bin 2 [7..0]	4	blue bin 2 [7..0]
5	red bin 2 [15..8]	5	blue bin 2 [15..8]
6	red bin 3 [7..0]	6	blue bin 3 [7..0]
7	red bin 3 [15..8]	7	blue bin 3 [15..8]
8	green bin 0 [7..0]	0 (0100)	threshold 0 [7..0] (00000000)
9	green bin 0 [15..8]	1	threshold 1 [7..0] (01000000)
10	green bin 1 [7..0]	2	threshold 2 [7..0] (10000000)
11	green bin 1 [15..8]	3	threshold 3 [7..0] (11000000)
12	green bin 2 [7..0]	4	threshold 4 [7..0] (11111111)
13	green bin 2 [15..8]		
14	green bin 3 [7..0]		
15	green bin 3 [15..8]		

Table C-6. Image statistics parameters. Note that threshold 0 to threshold 4 must contain monotonically increasing values.

References

Ackland and Dickinson 1996 B. Ackland and A. Dickinson, "Camera on a chip", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 22-25, February 1996.

Agwani *et al.* 1994 S. Agwani, D. Dobson, W. Washkurak, and S. Chamberlain, "A trilinear, 32 stage, selectable TDI CCD image sensor for high resolution colour scanning applications", *Proceedings of the SPIE*, Vol. 2172, pp 124-132, February 1994.

Akimoto *et al.* 1991 H. Akimoto, H. Ando, H. Nakagawa, Y. Nakahara, M. Hikiba, and H. Ohta, "A 1/3-in 410000-pixel CCD image sensor with feedback field-plate amplifier", *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 12, pp 1907-1914, December 1991.

Andersson and Shelby 1994 R. L. Andersson and K. A. Shelby, "A variable shutter timing mechanism for automatic gain control in a digital camera arrangement", *Bell Laboratories Internal Memorandum*, August 4, 1994.

Andoh *et al.* 1990 F. Andoh, K. Taketoshi, J. Yamazaki, M. Sugawara, Y. Fujita, and K. Mitani, "A 250,000-pixel image sensor with FET amplification at each pixel for high-speed television systems", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 212-213, February 1990.

Ando *et al.* 1991 H. Ando, M. Nakai, H. Akimoto, H. Ono, N. Ozawa, S. Ohba, T. Suzuki, M. Uehara, and M. Hikiba, "A 1/2-in CCD imager with lateral overflow-gate shutter", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 960-964, May 1991.

Aoki *et al.* 1982 M. Aoki, H. Ando, S. Ohba, I. Takemoto, S. Nagahara, T. Nakano, M. Kubo, and T. Fujita, "2/3-inch format MOS single-chip color imager", *IEEE Transactions on Electron Devices*, Vol. ED-29, No. 4, pp 745-750, April 1982.

AVP 1995 Video/Audio Processor AV4400A Advance Data Sheet, Lucent Technologies Microelectronics, 1995.

Aw and Wooley 1996 C. H. Aw and B. A. Wooley, "A 128×128-pixel standard CMOS image sensor with electronic shutter", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 180-181, February 1996.

Barbe 1975 D. F. Barbe, "Imaging devices using the charge-coupled concept", *Proceedings of the IEEE*, Vol. 63, No. 1, pp 38-67, January 1975.

Bayer 1976 B. E. Bayer, "Color imaging array", U.S. Patent 3 971 065, July 1976.

Blalack and Wooley 1995 T. Blalack and B. A. Wooley, "The effects of switching noise on an oversampling A/D converter", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 200-201, February 1995.

Blanksby *et al.* 1997 A. J. Blanksby, M. J. Loinaz, D. A. Inglis, and B. D. Ackland, "Noise performance of a color CMOS photogate image sensor", *International Electron Device Meeting Digest of Technical Papers*, Washington D.C., pp 205-208, December 7-10, 1997.

Bosiers *et al.* 1991 J. T. Bosiers, A. C. Kleinmann, B. G. Dillen, H. L. Peek, A. L. Kokshoorn, N. J. Daemen, A. G. van der Sijde, and L. T. van Gaal, "A 2/3-in 1187(H) × 581(V) S-VHS-compatible frame-transfer CCD for ESP and movie mode", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 1059-1068, May 1991.

Bosiers et al. 1995 J. T. Bosiers, E. Roks, H. L. Peek, A. C. Kleimann, and A. G. van der Sijde, "An S-VHS compatible 1/3″ color FT-CCD imager with low dark current by surface pinning", *IEEE Transactions on Electron Devices*, Vol. 42, No. 8, pp 1449-1460, August 1995.

Boyle and Smith 1970 W. S. Boyle and G. E. Smith, "Charge-coupled semiconductor devices", *Bell Systems Technical Journal*, Vol. 49, pp 587, 1970.

Burke and Gajar 1991 B. Burke and S. Gajar, "Dynamic suppression of interface-state dark current in buried-channel CCD's", *IEEE Transactions on Electron Devices*, Vol. 38, No. 2, pp 285-290, 1991.

Carnes and Kosonocky 1972 J. E. Carnes and W. F. Kosonocky, "Noise sources in charge-coupled devices", *RCA Rev.*, Vol. 33, pp 327-343, June 1972. also in *Charge-Coupled Devices and Applications*, Eds: R. Melen and D. Buss, IEEE Press, pp 87-103, 1977.

Centen 1991 P. Centen, "CCD on-chip amplifiers: Noise performance versus MOS transistor dimensions", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 1206-1216, May 1991.

Chamberlain 1969 S. G. Chamberlain, "Photosensitivity and scanning of silicon image detector arrays", *IEEE Journal of Solid-State Circuits*, Vol. SC-4, No. 6, pp 333-342, December 1969.

Chan and Youe 1995 W. -H. Chan and C. T. Youe, "Video CCD based portable digital still camera", *IEEE Transactions on Consumer Electronics*, Vol. 41, No. 3, pp 455-459, August 1995.

Cho and Gray 1995 T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35mW pipeline A/D converter", *IEEE Journal of Solid-State Circuits*, Vol. 30, No. 3, pp 166-172, March 1995.

Chong and Zak 1996 E. K. P. Chong and S. H. Zak, *An Introduction to Optimization*, John Wiley and Sons, 1996.

CIE 1957 *CIE International Lighting Vocabulary*, Second Edition, Paris, 1957.

Cohen and Kappauf 1982 J. B. Cohen and W. E. Kappauf, "Metameric color stimuli, fundamental metamers, and Wyszecki's metameric blacks", *American Journal of Psychology*, Vol. 95, No. 4, pp 537-564, Winter 1982.

Connectix Connectix Color Quickcam, http://www.connectix.com

Daemen and Peek 1994 N. Daemen and H. L. Peek, "Microlenses for image sensors", *Philips Journal of Research*, Vol. 48, pp 281-297, 1994.

Dennis and Schnabel 1989 J. E. Dennis and R. B. Schnabel, "A view of unconstrained optimization", *Optimization*, Vol. 1, (Editors G. L. Nemhauser, A. H. G. Rinnooy Kan, and M. J. Todd), Elsevier Science, Amsterdam, 1989.

Dickinson *et al.* 1995a A. Dickinson, B. Ackland, E. -S. Eid, D. Inglis, and E. R. Fossum, "A 256×256 CMOS active pixel image sensor with motion detector", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 226-227, February 1995.

Dickinson *et al.* 1995b A. Dickinson, B. Ackland, E. -S. Eid, D. Inglis, and E. R. Fossum, "Standard CMOS active pixel image sensors for multimedia applications", *Proceedings of the Sixteenth Conference on Advanced Research in VLSI*, Chapel Hill, NC, pp 214-224, March 27-29, 1995.

Dickinson et al. 1995c A. Dickinson, B. Ackland, K. Azadet, D. Inglis, S. Mendis, P. Jones, and E. R. Fossum, "A one million pixel CMOS active pixel image sensor", Unpublished, 1995.

Dickinson 1996 A. Dickinson, "A 1024×1024 CMOS active pixel image sensor", *Solid-State Circuits Technology Workshop on CMOS Imaging Technology*, San Francisco, CA, February 7, 1996.

Dillon *et al.* 1976 P. L. P. Dillon, A. T. Brault, J. R. Horak, E. Garcia, T. W. Martin, and W. A. Light, "Fabrication and performance of color filter arrays for solid-state imagers", *International Electron Device Meeting Digest of Technical Papers*, Washington D.C., December 1976.

D'Luna and Parulski 1991 L. J. D'Luna and A. Parulski, "A systems approach to custom VLSI for a digital color imaging system", *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 5, pp 727-737, May 1991.

Doyle B. Doyle, "DV cassette: The new wave of digital camcorders", http://www.dtv-group.com/DigVideo/DVC/DVC.html

Dubois 1985 E. Dubios, "The sampling and reconstruction of time-varying imagery with application in video systems", *Proceedings of the IEEE*, Vol. 73, No. 4, pp 502-522, April 1985.

Engelhardt and Seitz 1993 K. Engelhardt and P. Seitz, "Optimum color filters for CCD digital cameras", *Applied Optics*, Vol. 32, No. 16, pp 3015-3023, June 1993

Farrier *et al.* 1997 M. Farrier, C. Smith, and W. Pfister, "Design and processing aspects of a 50 megapixel full frame CCD image sensor", *Proceedings of the 1997 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Bruges, Belgium, June 5-7, 1997.

Firewire *IEEE Std 1394 - IEEE Standard for a High Performance Serial Bus*, IEEE New York, August 1996.

Flory 1985 R. E. Flory, "Image acquisition technology", *Proceedings of the IEEE*, Vol. 73, No. 4, pp 613-637, April 1985.

Fossum 1993 E. R. Fossum, "Active pixel sensors: Are CCDs dinosaurs?", *Proceedings of the SPIE*, Vol. 1900, pp 2-14, 1993.

Fossum 1994a E. R. Fossum, "Assessment of image sensor technology for future NASA missions", *Proceedings of the SPIE*, Vol. 2172, pp 38-53, February 1994.

Fossum 1994b E. R. Fossum, "Ultra low power imaging systems using CMOS image sensor technology", *Proceedings of the SPIE*, Vol. 2267, pp 1-5, 1994.

Fossum 1997 E. R. Fossum, "CMOS image sensors: Electronic camera-on-a-chip", *IEEE Transactions on Electron Devices*, Vol. 44, No. 10, pp 1689-1698, October 1997.

Fowler *et al.* 1994 B. Fowler, A. E. Gamal, and D. X. D. Yang, "A CMOS area image sensor with pixel-level A/D conversion", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 226-227, February 1994.

Furukawa *et al.* 1992 J. Furukawa, I. Hiroto, Y. Takamura, T. Wada, Y. Keigo, A. Izumi, K. Nishibori, R. Tatebe, S. Kitayama, M. Shimura, and H. Matsui, "A 1/3-inch 380L pixel (effective) IT-CCD image sensor", *IEEE Transactions on Consumer Electronics*, Vol. 38, No. 3, pp 595-600, August 1992.

Golub and Van Loan 1996 G. H. Golub and C. F. Van Loan, *Matrix Computations*, Third Edition, John Hopkins University Press, Baltimore, 1996.

Guidash *et al.* 1997 R. M. Guidash, T. -H. Lee, P. P. K. Lee, D. H. Sackett, C. I. Drowley, M. S. Swenson, L. Arbaugh, R. Hollstein, F. Shapiro, and S. Domer, "A 0.6 μm CMOS pinned photodiode color imager technology", *International Electron Device Meeting Digest of Technical Papers*, Washington D.C., pp 927-929, December 7-10, 1997.

Hall 1989 R. Hall, *Illumination and Color in Computer Generated Imagery*, Springer-Verlag, New York, 1989.

Hanma *et al.* 1983 K. Hanma, M. Masuda, H. Nabeyama, and Y. Saito, "Novel technologies for automatic focusing and white balancing of solid-state color video camera", *IEEE Transactions on Consumer Electronics*, Vol. CE-29, No. 3, pp 376-382, August 1983.

Hibbard 1995 R. H. Hibbard, "Apparatus and method for adaptively interpolating a full color image utilizing luminance gradients", U.S. Patent 5 382 976, January 1995.

Hojo *et al.* 1991 J. Hojo, Y. Naito, H. Mori, K. Fujikawa, N. Kato, T. Wakayama, E. Komatsu, and M. Itasaka, "A 1/3-in 510(H) × 492(V) CCD image sensor with mirror image function", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 954-959, May 1991.

Holland *et al.* 1997 S. E. Holland, G. Goldhaber, D. E. Groom, W. W. Moses, C. R. Pennypacker, S. Perlmutter, N. W. Wang, R. J. Stover, and M. Wei, "Development of back-illuminated, fully-depleted CCD image sensors for use in astronomy and astrophysics", *Proceedings of the IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Bruges, Belgium, June 5-7, 1997.

Holst 1996 G. C. Holst, *CCD Arrays, Cameras, and Displays*, JCD Publishing, Winter Park, Florida, and SPIE Optical Engineering Press, Bellingham, Washington, 1996.

Hunt 1970 R. W. G. Hunt, "Objectives in colour reproduction", *Journal of Photographic Science*, Vol. 18, pp 205-212, 1970.

Hunt 1995 R. W. G. Hunt, *Measuring Colour*, Second Edition, Ellis Horwood, London, 1995.

Hurwitz *et al.* 1997 J. E. D. Hurwitz, P. B. Denyer, D. J. Baxter, and G. Townsend, "An 800K-pixel color CMOS sensor for consumer still cameras", *Proceedings of the SPIE*, Vol. 3019, pp 115-124, 1997.

Imaide *et al.* 1986 T. Imaide, R. Nishimura, M. Noda, and M. Masuda, "Single-chip color cameras with reduced aliasing", Journal of Imaging Technology, Vol. 12, No. 5, pp 258-260, October 1986.

Imaide et al. 1990 T. Imaide, Y. Takagi, A. Nishizawa, M. Yamamoto, and M. Masuda, "A compact CCD color camera system with digital AWB control", *IEEE Transactions on Consumer Electronics*, Vol. 36, No. 4, pp 885-891, November 1990.

Ishihara et al. 1982 Y. Ishihara, E. Oda, H. Tanigawa, N. Teranishi, E. Takeuchi, I. Akiyama, K. Arai, M. Nishimura, and T. Kamata, "Interline CCD image sensor with an anti-blooming structure", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 168-169, February 1982.

Itakura *et al.* 1995 K. Itakura, T. Nobusada, Y. Toyoda, Y. Saitoh, N. Kokusenya, R. Nagayoshi, H. Tanaka, and M. Ozaki, "An aspect ratio switchable 2/3-inch 800k-pixel CCD image sensor", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 220-221, February 1995.

ITU 1995 *Video Coding for Low Bit Rate Communication*, Draft ITU-T Recommendation H.263, International Telecommunications Union, July 1995.

Izawa *et al.* 1990 F. Izawa, S. Yamaguchi, M. Nakagawa, A. Yamauchi, M. Sasaki, M. Umeda, Y. Uetani, and Y. Tagami, "Digital still video camera using semiconductor memory card", *IEEE Transactions on Consumer Electronics*, Vol. 36, No. 1, pp 1-9, February 1990.

Kamasz *et al.* 1994 S. R. Kamasz, M. G. Farrier, F. Ma, R. Sabila, and S. G. Chamberlain, "A high frame rate, motion compensated 25.4 megapixel image sensor", *Proceedings of the SPIE*, Vol. 2172, pp 155-166, February 1994.

Knop and Morf 1985 K. Knop and R. Morf, "A new class of mosaic color encoding patterns for single-chip cameras", *IEEE Transactions on Electron Devices*, Vol. ED-32, No. 8, pp 1390-1395, August 1985.

Kodak Kodak DCS460, http://www.kodak.com/daiHome/DCS/DCSIndex.shtml

Koike *et al.* 1980 N. Koike, I. Takemoto, K. Satoh, S. Hanamura, S. Nagahara, and M. Kubo, "MOS area sensor: Part I - Design considerations and performance of an n-p-n structure 484 × 384 element color MOS imager", *IEEE Transactions on Electron Devices*, Vol. ED-27, No. 8, pp 1676-1681, August 1980.

Kollarits and Gibbon 1990 R. V. Kollarits and D. C. Gibbon, "Improving the color fidelity of cameras for advanced television systems", *Bell Laboratories Technical Memorandum*, May 1, 1990.

Konishi and Iwabe 1997 M. Konishi and K. Iwabe, "Reviews on digital still cameras", *Proceedings of the IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Bruges, Belgium, June 5-7, 1997.

Kreyszig 1988 E. Kreyszig, *Advanced Engineering Mathematics*, Sixth Edition, John Wiley and Sons, 1988.

Kuriyama *et al.* 1991 T. Kuriyama, H. Kodama, T. Kozono, Y. Kitahama, Y. Morita, and Y. Hiroshima, "A 1/3-in 270 000 pixel CCD image sensor", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 949-953, May 1991.

Kyomasu 1991 M. Kyomasu, "A new MOS imager using photodiode as current source", *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 8, pp 1116-1122, August 1991.

Lavine *et al.* 1983 J. P. Lavine, E. A. Trabka, B. C. Burkey, T. J. Tredwell, E. T. Nelson, and C. Anagnostopoulosm "Steady-state photocarrier collection in silicon imaging devices", *IEEE Transactions on Electron Devices*, Vol. ED-30, No. 9, pp 1123-1134, September 1983.

Lenz and Lenz 1996 R. Lenz and U. Lenz, "The MARC project: colorimetric acquisition and printing of paintings with 20 000 × 20 000 pixels with an electronic camera", *Proceedings of the SPIE*, Vol. 2950, pp 325-332, 1996.

Levine *et al.* 1994 P. A. Levine, D. J. Sauer, F. -L. Hsueh, F. V. Shallcross, G. C. Taylor, G. M. Meray, J. R. Tower, L. Harrison, and W. Lawler, "Multi-port backside illuminated CCD imagers for moderate to high frame rate camera applications", *Proceedings of the SPIE*, Vol. 2172, pp 100-114, February 1994.

Liu *et al.* 1995 Y. -C. Liu, W. -H. Chan, and Y. -Q. Chen, "Automatic white balance for digital still camera", *IEEE Transactions on Consumer Electronics*, Vol. 41, No. 3, pp 460-466, August 1995.

Loinaz 1996 M. J. Loinaz, "White pixel defects in CMOS imaging arrays", *Solid-State Circuits Technology Workshop on CMOS Imaging Technology*, San Francisco, CA, February 7, 1996.

Loinaz *et al.* 1998a M. J. Loinaz, K. J. Singh, A. J. Blanksby, D. A. Inglis, K. Azadet, and B. D. Ackland, "A 200-mW 3.3-V CMOS color camera IC producing 352×288 24-b video at 30 frames/s", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 168-169, February 5-7, 1998.

Loinaz *et al.* 1998b M. J. Loinaz, K. J. Singh, A. J. Blanksby, D. A. Inglis, K. Azadet, and B. D. Ackland, "A 200-mW 3.3-V CMOS color camera IC producing 352×288 24-b video at 30 frames/s", To appear in *IEEE Journal of Solid-State Circuits*, 1988.

Macbeth *The Macbeth ColorChecker Color Rendition Chart*, Macbeth, Baltimore, MD.

Mansoorian *et al.* 1997 B. Mansoonrian, G. Yang, R. Panicacci, C. Wrigley, C. Staller, B. Pain, and E. Fossum, "Megapixel CMOS APS with analog and digital readout", *Proceedings of the 1997 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Bruges, Belgium, June 5-7, 1997.

Martinez *et al.* 1993 K. Martinez, J. Cupitt, and D. Saunders, "High resolution colorimetric imaging of paintings", *Proceedings of the SPIE*, Vol. 1901, pp 25-36, 1993.

Mayes and Chin 1996 M. K. Mayes and S. W. Chin, "Monolithic low-power 16b 1Msample/s self-calibrating pipeline ADC", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 312-313, 1996.

M^{c}Grath *et al.* 1997 R. D. M^{c}Grath, V. S. Clark, P. K. Duane, L. G. M^{c}Ilrath, and W. D. Washkurak, "Current-mediated, current-reset 768×512 active pixel sensor array", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 182-183, February 1997.

M^{c}Ilrath *et al.* 1997 L. G. M^{c}Ilrath, V. S. Clark, P. K. Duane , R. D. M^{c}Grath, and W. D. Washkurak, " Design and analysis of a 768×512 current-mediated active pixel array image sensor", *IEEE Transactions on Electron Devices*, Vol. 44, No. 10, pp 1706-1715, October 1997.

Mendis et al. 1993a S. K. Mendis, B. Pain, R. H. Nixon, and E. R. Fossum, "Low-light-level sensor with on-chip signal processing", *Proceedings of the SPIE*, Vol. 1952, pp 1-11, 1993.

Mendis et al. 1993b S. Mendis, S. Kemeny, and E. R. Fossum, "A 128 × 128 CMOS active pixel image sensor for highly integrated imaging systems", *International Electron Device Meeting Digest of Technical Papers*, pp 583-586, 1993.

Mendis *et al.* 1994a S. K. Mendis, S. E. Kemeny, R. C. Gee, B. Pain, Q. Kim, and E. R. Fossum, "Progress in CMOS active pixel image sensors", *Proceedings of the SPIE*, Vol. 2172, pp 19-29, February 1994.

Mendis *et al.* 1994b S. Mendis, S. E. Kemeny, and E. R. Fossum, "CMOS active pixel sensor", *IEEE Transactions on Electron Devices*, Vol. 41, No. 3, pp 452-453, March 1994.

Mendis *et al.* 1997a S. K. Mendis, S. E. Kemeny, R. C. Gee, B. Pain, C. O. Staller, Q. Kim, and E. R. Fossum, "CMOS active pixel image sensors for highly integrated imaging systems", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 2, pp 187-197, February 1997.

Mendis *et al.* 1997b S. Mendis, A. J. Budrys, J. Lin, and K. Cham, "Active pixel image sensors in 0.35μm CMOS technology", *Proceedings of the 1997 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Bruges, Belgium, June 5-7, 1997.

Morimoto *et al.* 1995 M. Morimoto, K. Orihara, N. Mutoh, A. Toyoda, M. Ohbo, Y. Kawakami, T. Nakano, K. Chiba, S. Kawai, K. Hatano, K. Arai, M. Nishimura, Y. Nakshiba, A. Kohno, I. Akiyama, N. Teranishi, and Y. Hokari, "A 1-inch 2-M pixel HDTV CCD image sensor with tungsten photo-shield and H-CCD shunt wiring", *IEEE Transactions on Electron Devices*, Vol. 42, No. 1, pp 50-57, 1995.

Morimura *et al.* 1990 A. Morimura, K. Uomori, Y. Kitamura, A. Fujioka, J. Harada, S. Iwamura, and M. Hirota, "A digital video camera system", *IEEE Transactions on Consumer Electronics*, Vol. 36, No. 4, pp 866-876, November 1990.

Mutoh *et al.* 1991 N. Mutoh, M. Morimoto, M. Nishimura, N. Teranishi, and E. Oda, "New low-noise output amplifer for high-definition CCD image sensor", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 1048-1051, May 1991.

Mutoh *et al.* 1995 N. Mutoh, K. Orihara, Y. Kawakami, T. Nakano, S. Kawai, I. Murakami, A. Tanabe, S. Suwazono, K. Arai, N. Teranishi, M. Furumiya, M. Morimoto, K. Hatano, K. Minami, and Y. Hokari, "A 1/4-inch 380k pixel IT-CCD image sensor employing gate-assisted punchthrough read-out mode", *IEEE Transactions on Electron Devices*, Vol. 42, No. 10, pp 1783-1788, October 1995.

Mutoh *et al.* 1997 N. Mutoh, S. Kawai, T. Yamada, Y. Kawakami, T. Nakano, K. Orihara, and N. Teranishi, "Driving voltage reduction of shift registers in IT-CCD image sensors", *Proceedings of the 1997 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Bruges, Belgium, June 5-7, 1997.

Naito *et al.* 1995 Y. Naito, A. Kobayashi, T. Ishigami, S. Nakagawa, Y. Shimohida, A. Izumi, and H. Endo, "A 1/3-inch 360k pixel progressive scan CCD image sensor", *IEEE Transactions on Consumer Electronics*, Vol. 31, No. 3, August 1995.

Nakamura *et al.* 1995 J. Nakamura, S. E. Kemeny, and E. R. Fossum, "CMOS active pixel image sensor with simple floating gate pixels", *IEEE Transactions on Electron Devices*, Vol. 42, No. 9, pp 1693-1694, September 1995.

Nakamura *et al.* 1997 J. Nakamura, B. Pain, T. Nomoto, T. Nakamura, and E. R. Fossum, "On-focal-plane signal processing for current-mode active pixel sensors", *IEEE Transactions on Electron Devices*, Vol. 44, No. 10, pp 1747-1758, October 1997.

Nakamura *et al.* 1986 T. Nakamura, K. Matsumoto, R. Hyunga, and A. Yusa, "A new MOS image sensor operating in a non-destructive readout mode", *International Electron Device Meeting Digest of Technical Papers*, pp 353-356, 1986.

Netravali and Haskell 1988 A. N. Netravali and B. G. Haskell, Digital Pictures: Representation and Compression, Plenum Press, New York, 1988.

Nishida *et al.* 1988 Y. Nishida, J. Koike, T. Watanabe, Y. Iino, H. Ohtake, M. Abe, and S. Yoshikawa, "Wide dynamic range HDTV image sensor with aliasing suppression", *IEEE Transactions on Consumer Electronics*, Vol. 34, No. 3, August 1988.

Nishima *et al.* 1995 O. Nishima, N. Kato, T. Higuchi, Y. Wataya, M. Oohashi, E. Machishima, J. Kuroiwa, and K. Kusano, "A 1/4-inch 380k-pixel IT-CCD image sensor", *IEEE Transactions on Consumer Electronics*, Vol. 41, No. 3, pp 430-435, August 1995.

Nisizawa *et al.* 1979 J. Nisizawa, T. Tamamushi, and T. Ohmi, "Static induction transistor image sensors", *IEEE Transactions on Electron Devices*, Vol. 26, No. 12, pp 1970-1977, 1979.

Nixon *et al.* 1995 R. H. Nixon, S. E. Kemeny, C. O. Staller, and E. R. Fossum, "128×128 CMOS photodiode-type active pixel sensor with on-chip timing, control, and signal chain electronics", *Proceedings of the SPIE*, Vol. 2415, pp 1-8, 1995.

Nixon *et al.* 1996a R. H. Nixon, S. E. Kemeny, C. O. Staller, and E. R. Fossum, "A 256 × 256 CMOS Active Pixel Sensor Camera-on-a-Chip", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 178-179, February, 1996.

Nixon *et al.* 1996b R. H. Nixon, S. E. Kemeny, B. Pain, C. O. Staller, and E. R. Fossum, "256 × 256 CMOS Active Pixel Sensor Camera-on-a-Chip", *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 12, pp 2046-2050, December 1996.

Noble 1968 P. J. W. Noble, "Self-scanned silicon image detector arrays", *IEEE Transactions on Electron Devices*, Vol. ED-15, No. 4, pp 202-209, April 1968.

Noda *et al.* 1986 M. Noda, T. Imaide, T. Kinugasa, and R. Nishimura, "A solid-state color video camera with a horizontal readout MOS imager", *IEEE Transactions on Consumer Electronics*, Vol. CE-32, No. 3, pp 329-336, August 1986.

Oba *et al.* 1997 E. Oba, K. Mabuchi, Y. Iida, N. Nakamura, and H. Miura, "A 1/4 inch 300k square pixel progressive scan CMOS active pixel image sensor", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 180-181, February 1997.

Ohba *et al.* 1980 S. Ohba, M. Nakai, H. Ando, S. Hanamura, S. Shimada, K. Satoh, K. Takahashi, M. Kubo, and T. Fujita, "MOS area sensor: Part II - low noise MOS area sensor with antiblooming photodiodes", *IEEE Transactions on Electron Devices*, Vol. ED-27, No. 8, pp 1682-1687, August 1980.

Ohno 1996 S. Ohno, "Digital photography and color printing", *Journal of Imaging Science and Technology*, Vol. 40, No. 6, pp 556-567, November/December 1996.

Onga *et al.* 1990 M. Onga, M. Kawamata, M. Sase, I. Masuda, F. Yamaguchi, and R. Kawai, "New signal processing LSIs for the 8mm camcorder", *IEEE Transactions on Consumer Electronics*, Vol. 36, No. 3, pp 494-502, August 1990.

Ozaki *et al.* 1991 T. Ozaki, H. Kinugasa, and T. Nishida, "A low-noise line-amplified MOS imaging devices", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 969-975, May 1991.

Ozaki *et al.* 1994 T. Ozaki, H. Ono, H. Tanaka, A. Sato, M. Nakai, and T. Nishida, "A high-packing density pixel with punchthrough read-out method for an HDTV interline CCD", *IEEE Transactions on Electron Devices*, Vol. 41, No. 7, pp 1128-1135, July 1994.

Ozawa and Takahashi 1991 N. Ozawa and K. Takahashi, "A correlative coefficient multiplying (CCM) method for chrominance moire reduction in single-chip color video cameras", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 1217-1225, May 1991.

Parulski 1985 K. A. Parulski, "Color filters and processing alternatives for one-chip cameras", *IEEE Transactions on Electron Devices*, Vol. ED-32, No. 8, pp 1381-1389, August 1985.

Parulski *et al.* 1989 K. A. Parulski, L. J. D'Luna, and R. H. Hibbard, "A digital color CCD imaging system using custom VLSI circuits", *IEEE Transactions on Consumer Electronics*, Vol. 35, No. 3, pp 382-389, August 1989.

Parulski and Jameson 1996 K. Parulski and P. Jameson, "Enabling technologies for a family of digital cameras", *Proceedings of the SPIE*, Vol. 2654, pp 156-163, 1996.

Poynton 1996 C. A. Poynton, *A Technical Introduction to Digital Video*, John Wiley & Sons Inc, New York 1996.

Quicktake Apple Quicktake 150, http://support.info.apple.com/qtake/press.html

Razavi 1995 B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, New Jersey, 1995.

Reklaitis *et al.* 1983 G. V. Reklaitis, A. Ravindran, and K. M. Ragsdell, *Engineering Optimization: Methods and Applications*, John Wiley and Sons, New York, 1983.

Renshaw *et al.* 1990 D. Renshaw, P. Denyer, G. Wang, and M. Lu, "ASIC vision", *Proceedings of the IEEE Custom Integrated Circuit Conferences*, pp 7.3.1-7.3.4, 1990.

Saks 1980 N. S. Saks, "A technique for suppressing dark current generated by interface states in buried channel CCD imagers", *IEEE Electon Device Letters*, EDL-1, No. 7, pp 131-133, July 1980.

Satoh *et al.* 1997 T. Satoh, N. Mutoh, M. Furumiya, I. Murakami, S. Suwazono, C. Ogawa, K. Hatano, H. Utsumi, S. Kawai, K. Arai, M. Morimoto, K. Orihara, T. Tamura, N. Teranishi, and Y. Hokari, "Optical limitations to cell size reduction in IT-CCD image sensors", *IEEE Transactions on Electron Devices*, Vol. 44, No. 10, pp 1599-1603, October 1997.

Schaeffer et al. 1994 C. J. Schaeffer, H. Stoldt, B. G. M. Dillen, H. L. Peek, and W. Hoekstra, "High-speed, high-performance 1M pixel imager for machine vision applications", *Proceedings of the SPIE*, Vol. 2172, pp 115-123, 1994.

Scheffer *et al.* 1997 D. Scheffer, B. Dierickx, and G. Meynants, "Random addressable 2048×2048 active pixel image sensor", *IEEE Transactions on Electron Devices*, Vol. 44, No. 10, pp 1716-1720, October 1997.

Schrieber 1993 W. F. Schrieber, *Fundamentals of Electronic Imaging Systems: Some Aspects of Image Processing*, Third Edition, Springer-Verlag, Berlin, 1993.

Smith *et al.* 1997 C. Smith, E. Fox, M. Miethig, and M. Farrier, "A low smear p-substrate frame interline transfer sensor with kTC noise reduction", *Proceedings of the 1997 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Bruges, Belgium, June 5-7, 1997.

Smith *et al.* 1998 S. Smith, J. Hurwitz, M. Torrie, D. Baxter, A. Holmes, M. Panaghiston, R. Henderson, A. Murray, S. Anderson, and P. Denyer, "A single-chip CMOS 306×244-pixel NTSC video camera", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 170-171, February 5-7, 1998.

Solhusvik *et al.* 1996 J. Solhusvik, C. Cavadore, F. X. Audoux, N. Verdier, J. Farre, O. Saint-Pe, R. Davancens, and J. P. David, "Recent experimental results from a CMOS active pixel sensor with photodiode and photogate pixels", *Proceedings of the SPIE*, Vol. 2950, pp 18-24, October 1996.

Sony Sony DCR-DX700 Digital Handicam, http://www.sel.sony.com/SEL/consumer/camcorder/equip.html

Sproson 1983 W. N. Sproson, *Colour Science in Television and Display Systems*, Adam Hilger Ltd, Bristol, 1983.

Stevens et al. 1991 E. G. Stevens, B. C. Burkey, D. N. Nichols, Y. S. Yee, D. L. Losee, T. -H. Lee, T. J. Tredwell, and R. P. Khosla, "A 1-megapixel, progressive-scan image sensor with antiblooming control and lag-free operation", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 981-988, May 1991.

Stevens and Lavine 1994 E. G. Stevens and J. P. Lavine, "An analytical, aperture, and two-layer carrier diffusion MTF and quantum efficiency model for solid-state image sensors", *IEEE Transactions on Electron Devices*, Vol. 41, No. 10, pp 1753-1760, October 1994.

Stimson 1974 A. Stimson, *Photometry and Radiometry for Engineers*, John Wiley and Sons, 1974.

Streetman 1990 B. G. Streetman, *Solid-State Electronic Devices*, Third Edition, Prentice Hall, New Jersey, 1990.

Su *et al.* 1993 D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits", *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 4, pp 420-430, April 1993.

Suzuki *et al.* 1990 S. Suzuki, T. Kusunoki, and M. Mori, " Color characteristic design for color scanners", *Applied Optics*, Vol. 29, No. 34, pp 5187-5192, December 1990.

Tabei *et al.* 1991 M. Tabei, K. Kobayashi, and M. Shizukuishi, "A new CCD architecture of high-resolution and sensitivity for color digital still picture", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 1052-1058, May 1991.

Takemura *et al.* 1995 Y. Takemura, K. Suda, H. Serita, H. Kotaki, T. Sugiki, A. Iida, O. Osonoe, T. Sakurai, K. Ooi, N. Sasano, and H. Sekine, "HDTV compact digital camera using 2/3˝ 1.3M CCD image sensor", *IEEE Transactions on Consumer Electronics*, Vol. 41, No. 1, pp 81-88, February 1995.

Takizawa et al. 1983 Y. Takizawa, H. Kotaki, K. Saito, T. Sugiki, and Y. Takemura, "Field integration mode CCD color television camera using a frequency interleaving method", *IEEE Transactions on Consumer Electronics*, Vol. CE-29, No. 3, pp 358-364, August 1983.

Tanaka *et al.* 1989 N. Tanaka, T. Ohmi, and Y. Nakamura, "A novel bipolar imaging device with self-noise reduction capacity", *IEEE Transactions on Electron Devices*, Vol. 36, No. 1, pp 31-37, 1989.

Teranishi *et al.* 1982 N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, and K. Arai, "No image lag photodiode structure in the interline CCD image sensor", *International Electron Device Meeting Digest of Technical Papers*, pp 324-327, 1982.

Theuwissen 1994 A. J. P. Theuwissen, "CCD Imaging", *Philips Journal of Research*, Vol. 48, pp 147-158, 1994.

Theuwissen 1995 A. J. P. Theuwissen, *Solid-State Imaging with Charge-Coupled Devices*, Kluwer Academic Publishers, Dordrecht, Netherlands, 1995.

Toren and Bisschop 1994 W. J. Torren and J. Bisschop, "Complete characterization of dark current in frame transfer image sensors", *Philips Journal of Research*, Vol. 48, pp 207-231, 1994.

USB *Universal Serial Bus Specification*, Version 0.99, August 28, 1995.

Vrhel and Trussell 1994 M. J. Vrhel and H. J. Trusell, "Filter considerations in color correction", *IEEE Transactions on Image Processing*, Vol. 3, No. 2, pp 147-161, March 1994.

Vrhel and Trussell 1995 M. J. Vrhel and H. J. Trusell, "Optimal color filters in the presence of noise", *IEEE Transactions on Image Processing*, Vol. 4, No. 6, pp 814-823, June 1995.

Walden *et al.* 1972 R. H. Walden, R. H. Krambeck, R. J. Strain, J. M^{c}Kenna, N. L. Schyer, and G. E. Smith, "The buried-channel charge coupled device", *Bell Systems Technical Journal*, Vol. 51, pp 1635-1640, 1972.

Wang *et al.* 1994 J. -C. Wang, D. -S. Su, D. -J. Hwung, and J. -C. Lee, "A single-chip CCD signal processor for digital still cameras", *IEEE Transactions on Consumer Electronics*, Vol. 40, No. 3, pp 476-483, August 1994.

Watanabe *et al.* 1997 T. Watanabe, E. Koyama, K. Yamamoto, E. Akaike, S. Takano, T. Inoue, K. Okada, T. Kawasaki, H. Urabe, H. Adachi, J. Nakai, and K. Misawa, "A high performance 5V-only 1/5-inch 220k-pixel CCD image sensor", *Proceedings of the 1997 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Bruges, Belgium, June 5-7, 1997.

Weckler 1967 G. P. Weckler, "Operation of p-n junction photodetectors in a photon flux integrating mode", *IEEE Journal of Solid-State Circuits*, Vol. SC-2, No. 3, pp 65-73, September 1967.

Weste and Eshraghian 1985 N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design*, Addison-Wesley, 1985.

White *et al.* 1974 M. H. White, D. R. Lampe, F. C. Blaha, and I. A. Mack, "Characterization of surface channel CCD image arrays at low light levels", *IEEE Journal of Solid-State Circuits*, Vol. SC-9, No. 1, pp 1-13, February 1974.

Wilson 1997 R. Wilson, "Kodak, Motorola team on imaging chips for cameras", *EE Times*, Issue 959, June 23, 1997.

Wong 1996 H. S. Wong, "Technology and device scaling considerations for CMOS imagers", *IEEE Transactions on Electron Devices*, Vol. 43, No. 12, pp 2131-2142, December 1996.

Wong *et al.* 1998 H. -S. P. Wong, R. T. Chang, E. Crabbé, and P. D. Agnello, "CMOS active pixel image sensors fabricated using a 1.8-V, 0.25-μm CMOS technology", *IEEE Transactions on Electron Devices*, Vol. 45, No. 4, pp 889-894, April 1998.

Wyszecki and Stiles 1982 G. Wyszecki and W. S. Stiles, *Color Science: Concepts and Methods, Quantitative Data and Formulae*, Second Edition, John Wiley & Sons Inc., 1982.

Yadid-Pecht *et al.* 1991 O. Yadid-Pecht, R. Ginosar, and Y. S. Diamand, "A random access photodiode array for intelligent image capture", *IEEE Transactions on Electron Devices*, Vol. 38, No. 8, pp 1772-1780, August 1991.

Yadid-Pecht *et al.* 1997 O. Yadid-Pecht, B. Pain, C. Staller, C. Clark, and E. Fossum, "CMOS active pixel sensor star tracker with regional electronic shutter", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 2, pp 285-288, February 1997.

Yamagishi *et al.* 1991 M. Yamagishi, M. Negishi, H. Yamada, T. Tsunakawa, K. Shinohara, T. Ishimaru, Y. Kamide, Y. Yamazaki, H. Abe, H. Kanbe, Y. Tomiya, K. Yonemoto, T. Iizuka, S. Nakamura, K. Harada, and K. Wada, "A 2 million pixel FIT-CCD image sensor for HDTV camera systems", *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, pp 976-980, 1991.

Yamaguchi *et al.* 1997 T. Yamaguchi, I. Shimizu, K. Henmi, H. Tanaka, T. Tanaka, H. Matsumaru, M. Miyashita, I. Ihara, S. Tashiro, M. Yamanaka, Y. Nishi, K. Tachikawa, and H. Komobuchi, " A 2V driving voltage 1/3-inch 410k-pixel hyper-D range CCD", *Proceedings of the 1997 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Bruges, Belgium, June 5-7, 1997.

Yang *et al.* 1996 D. X. D. Yang, H. Min, B. Fowler, A. E. Gamal, M. Beiley, and K. Cham, "Test structures for characterization and comparative analysis of CMOS image sensors", *Proceedings of the SPIE*, Vol. 2950, pp 8-17, October 1996.

Zeki 1993 S. Zeki, *A Vision of the Brain*, Blackwell Scientific Publications, Oxford, 1993.

Zen *et al.* 1994 H. Zen, S. H. Kim, J. H. Jang, H. S. Chun, and C. H. Lee, "A new digital camera processor with separated Y and C gamma control", *IEEE Transactions on Consumer Electronics*, Vol. 40, No. 3, pp 610-615, August 1994.

Zhou *et al.* 1997 Z. Zhou, B. Pain, and E. R. Fossum, "CMOS active pixel sensor with on-chip successive approximation analog-to-digital converter", *IEEE Transactions on Electron Devices*, Vol. 44, No. 10, pp 1759-1763, October 1997.

Relevant Publications

A. J. Blanksby, M. J. Loinaz, D. A. Inglis, and B. D. Ackland, "Noise performance of a color CMOS photogate image sensor", *International Electron Device Meeting Digest of Technical Papers*, Washington D.C., pp 205-208, December 7-10, 1997.

M. J. Loinaz, K. J. Singh, A. J. Blanksby, D. A. Inglis, K. Azadet, and B. D. Ackland, "A 200-mW 3.3-V CMOS color camera IC producing 352×288 24-b video at 30 frames/s", *International Solid-State Circuit Conference Digest of Technical Papers*, San Francisco, CA, pp 168-169, February 5-7, 1998.

M. J. Loinaz, K. J. Singh, A. J. Blanksby, D. A. Inglis, K. Azadet, and B. D. Ackland, "A 200-mW 3.3-V CMOS color camera IC producing 352×288 24-b video at 30 frames/s", *IEEE Journal of Solid-State Circuits,* Vol. 33, No. 12, pp 2092-2103, December 1998.

Colour Plate 1

(a) Colour errors resulting from the application of the colour correction matrix determined by minimizing the MSE_{XYZ} using the least squares algorithm. The centre portion of each sample gives the desired colour while the surround gives the colour rendered by the colour correction matrix.

(b) Colour errors resulting from the application of the colour correction matrix determined by minimizing $(\Delta E^*_{uv})_{RMS}$ using the conjugate gradient algorithm.

Colour Plate 2

(a) Image acquired by the photogate sensor after spatial interpolation (D_{65} illumination, 4.3-lux).

(b) Image acquired by the photogate sensor after colour correction.