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# **Energy Minimization of Portable Multimedia Systems through Rate Selection and Dynamic Voltage Scaling**

by

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# Abstract

Dynamic supply voltage and frequency scaling involves variation of supply voltage and clock frequency at run-time to minimize the total energy consumption of electronic systems. This method is very effective in reducing energy consumption because of the quadratic relationship between energy and supply voltage. However, use of dynamic voltage and clock scaling requires careful design of systems to function across a range of supply voltages (and frequencies), and additional circuitry such as DC-DC converters.

Dynamic voltage scaling can provide energy savings and extend battery life of portable devices. This thesis focuses on portable multimedia applications operating in fixed throughput mode. These applications have a constant processing requirement, and less than maximum workload levels are characterized by idling, and consequently idle losses. By using dynamic voltage scaling, the processing speed of data samples can be altered at run-time to eliminate idle losses. For optimum energy savings, dynamic voltage scaling requires an infinite number of voltage levels. However, supporting such continuous voltage levels involves introduction of complexities such as closed loop feedback into the DC-DC converter. Moreover, output capacitance of the DC-DC converter must be significantly reduced to achieve fast voltage transitions. This however results in increased output voltage ripple, reduced converter efficiency at low voltages, and decreased system stability. An alternative approach is to use a small number of discrete voltage levels or voltage quantizations and provide open-loop voltage switching. This approach is called the voltage quantization model. Since this approach involves the use of a small number of voltage levels, most workloads can no longer be translated to unique supply voltage levels for voltage scaling, and this leads to selection of higher than ideal voltage quantizations for voltage scaling. This causes idle periods and consequently increased idle losses.

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Prior research shows two approaches for reducing idle losses in the voltage quantization model. They are clock gating and voltage dithering. The clock gating technique turns off the clock to minimize energy loss, and this requires special circuitry and special hardware design. Moreover, this technique is only useful when used at a low frequency due to the overheads associated with clock gating. Since fixed throughput mode involves continuous data processing, idle loss reduction through clock gating is ineffective for this class of applications. Voltage dithering on the other hand eliminates idle loss by processing a data sample at two voltage quantizations. However, this increases the number of voltage transitions and consequently increases the transition energy cost and switching noise. Moreover, voltage dithering becomes infeasible when the sample period of the computation becomes comparable to voltage transition time.

In this thesis we propose an alternative algorithmic approach to reducing idle losses in the voltage quantization model. The proposed rate selection approach uses the novel concept of transforming the workload distribution of data sequences to eliminate idle losses. The thesis also presents a number of enhancements to the rate selection approach that improve the energy efficiency and minimize the computational overhead. Our experimental results indicate that the rate selection approach is more energy efficient compared to the best existing approaches, while also significantly reducing the total number of voltage transitions.