Design Techniques for Low Power Mixed Analog-Digital Circuits with Application to Smart Wireless Systems

by

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Contents

Abstract

This dissertation presents and discusses new design techniques for mixed analog-digital circuits with emphases on low power and small area for standard low-cost CMOS VLSI technology. The application domain of the devised techniques is radio frequency identification (RFID) systems, however the presented techniques are applicable to wide range of mixed mode analog-digital applications. Hence the techniques herein apply to a range of smart wireless or mobile systems. The integration of both analog and digital circuits on a single substrate has many benefits such as reducing the system power, increasing the system reliability, reducing the system size and providing high inter-system communications speed – hence, a cost effective system implementation with increased performance. On the other hand, some difficulties arise from the fact that standard low-cost CMOS technologies are *tuned* toward maximising digital circuit performance and increasing transistor density per unit area. Usually these technologies have a wide spread in transistor parameters that require new design techniques that provide circuit characteristics based on relative transistor parameters rather than on the absolute value of these parameters.

This research has identified new design techniques for mostly analog and some digital circuits for implementation in standard CMOS technologies with design parameters dependent on the relative values of process parameters, resulting in technology independent circuit design techniques. The techniques presented and discussed in this dissertation are (*i*) applied to the design of low-voltage and low-power controlled gain amplifiers, (*ii*) digital trimming techniques for operational amplifiers, (*iii*) low-power and low-voltage Schmitt trigger circuits, (*iv*) very low frequency to medium frequency low power oscillators, (*v*) low power Gray code counters, (*vi*) analog circuits utilising the neuron MOS transistor, (*vii*) high value floating resistors, and (*viii*) low power application specific integrated circuits (ASICs) that are particularly needed in radio frequency identification systems. The new techniques are analysed, simulated and verified experimentally via five chips fabricated through the MOSIS service.

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Declaration

This work contains no material which has been accepted for the award of any other degree or diploma in any university or other tertiary institution and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text.

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AC Alternating current

ADC Analog to digital converter

ASIC Application specific integrated circuits

CMC Current mirror configuration

CMC Current mirror transistor configuration

CMOS Complementary Metal Oxide Field Effect Transistor

CPL Complementary Pass Transistor Logic

CVSL Cascade voltage switch logic

DAC Digital to analog converter

DSP Digital signal processor

EEROM Electrically erasable read-only memory

FII Finite input impedance

FPAA Field programmable analog array

FPGA Field programmable gate array

ISD Integrated Silicon Design Pty. Ltd.

ISD9664 ISD Pty. Ltd. transponder chip

KCL Kirchoff's current law

Li Lithium

LiIon Lithium-Ion

MOSFET Metal Oxide Field Effect Transistor

NiCd Nickel-Cadmium

NiMH Nickel Metal-Hydride

NiZn Nickel-Zinc

nMOS or n-MOS n-type MOSFET

npn Bipolar transistor of n-p-n type

PLL Phase locked loop

PMD Program mode detection circuit

PMD Program mode detection

pMOS or p-MOS p-type MOSFET

PTC Parallel transistor configuration

RAM Random access memory

RF Radio frequency

RFID Radio frequency identification system

RMS Root mean square

SC Switched capacitor

STC Series transistor configuration

TDC Time-to-delay converter

ULSI Ultra large scale integration

VHVF Very high value floating resistor

VLSI Very large scale integration

EMSO Extended mode Schmitt oscillator

List of Symbols

β_i	The intrinsic transconductance parameter of transistor i defined as $K_i'W/L$, A/V^2
ΔV	An equivalent threshold voltage mismatch, V
ϵ_{si}	The dielectric constant of silicon, 1.0359e-10 F/m
η	The emission factor or subthreshold slope of a pn junction
γ	The body effect factor, V$^{1/2}$
γ_g	the floating gate gain factor
g_{m_i}	The transconductance of transistor i, A/V
μ_i	The surface mobility of carriers type i, cm^2/Vs
$\overline{\mu}$	The nominal channel mobility, cm^2/Vs
$\overline{C}_{ox}$	The nominal oxide capacitance per unit area, F/m^2
$\overline{L}$	The nominal length of the transistor, m
$\overline{Q}_D$	The nominal space charge densities per unit area, C/m^2
$\overline{Q}_{ii}$	The ion implanted charge densities per unit area, C/m^2
$\overline{Q}_{ss}$	The surface state charge densities per unit area, C/m^2
$\overline{t}$	The nominal oxide thickness, m
$\overline{V}_T$	The nominal threshold voltage, V
$\overline{W}$	The nominal width of the transistor, m
ϕ	The flat band voltage, V
ϕ_F	The Fermi potential in the bulk, V
ϕ_F	The floating gate voltage, V
ϕ_{MS}	The gate-semiconductor function difference, V
ψ_s	The channel surface potential, V
σ_{g_μ}	The global standard deviation of channel mobility, cm^2/Vs

σ_{g_L}	The standard deviation of transistor length due to global variation, m
$\sigma_{g_{ox}}$	The global standard deviation of the oxide thickness, m
$\sigma_{g_{q_{ii}}}$	The standard deviations of the global ion-implanted charge, C
$\sigma_{g_{q_{ss}}}$	The standard deviations of the global surface-state charge, C
σ_{g_W}	The standard deviation of transistor width due to global variation, m
σ_{l_μ}	The local standard deviation of channel mobility, cm^2/Vs
σ_{l_L}	The standard deviation of transistor length due to local variation, m
$\sigma_{l_{ox}}$	The local standard deviation of the oxide thickness, m
$\sigma_{l_{q_{ii}}}$	The standard deviations of the local ion-implanted charge, C
$\sigma_{l_{q_{ss}}}$	The standard deviations of the local surface state charge, C
σ_{l_W}	The standard deviation of transistor width due to local variation, m
ε_{ox}	The permitivity of oxide layer, F/cm
C_{gs}	The gate to source capacitance, F
C_{ox}	The gate oxide capacitance per unit area, $F/\mu m^2$
d_e	The correlation radius of the local length variation
d_{l_μ}	The correlation radius of the local mobility variation
d_q	The correlation radius of local charge variation
g_{d_i}	The output conductance of transistor i, S
$K_i^{'}$	The transconductance parameter of transistor i is defined as $\mu_i C_{ox}$ or $\mu_i \varepsilon_{ox}/T_{ox}$, A/V^2
n	The subthreshold slope of a MOS transistor
N_{eff}	The substrate doping density, cm^{-3}
q	The electron charge, 1.60212e-19 C
Q_F	The charge on the floating gate, C

S_i The width to length ratio of transistor i

T_{ox} The thickness of the oxide layer, m

U_t The thermal voltage, V

$V_{d,sat}$ Drain saturation voltage, V

V_{dd} Supply voltage, V

V_{HL} The input voltage at which the Schmitt trigger circuit output switches from high to low, V

V_{ios} The introduced offset voltage, V

V_{LH} The input voltage at which the Schmitt trigger circuit output switches from low to high, V

V_{th} MOSFET threshold voltage, V

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Chapter 1

Introduction and Motivation

THE aims of this research are to present and discuss new design techniques for mixed analog-digital circuits. The new techniques can be used to improve system performance through circuit design. The applicable performance criteria are in terms of power consumption and silicon real estate area. The presented techniques are relevant to a wide range of applications, however the research focus is directed toward mobile systems and more specifically toward the transponder part of the RFID system. This part was targeted as it is the only mass produced part of the RFID system and its power consumption and area have a great impact on the RFID system performance and cost.

The presented techniques target standard low-cost CMOS technologies. The new techniques rely on relative process parameters rather than the absolute value of these parameters, resulting in designs that are robust against process variation and temperature effects and can generally be scaled to future CMOS technologies with minimal amount of effort.

1.1 Mixed Signal Systems

The great advances in integrated microelectronic technology have led to enormous progress in a number of research areas such as wired and wireless communications, telemetry, biomedical devices, optoelectronics, mechatronics, mobile computing, etc. These research areas resulted in a large number of applications such as pocket calculators, personal computers, mobile phones, wristwatches, hearing aids, pacemakers, etc. These applications are examples where the advances in microelectronic technology have greatly influenced human life.

The increasing demands for portable systems have led to an increased interest into designing fully integrated systems that can sustain their operation for a long time using a very small amount of power. The sources of energy for portable devices are from chemical batteries or rectified from a radio frequency RF[1] source. Hence, mobile devices should consume a very small amount of power and have a small form factor. The common requirements of these devices are low cost, small size and reliable operation over a long period of time. In [Al-Sarawi *et al.* 1998] – also listed in Appendix A – it has been shown that three dimensional packaging integration does lead to increasing system reliability and reducing its power and cost. For example, a 30–40 times reduction in size and weight is achievable using 3-D technology compared to 2-D integration and 5–10 times improvement in silicon efficiency [Ladd 1993]. Silicon efficiency refers to an efficient utilisation of real estate area on a silicon dice. It has been reported in [Ramprasad *et al.* 1999, Chandrakasan *et al.* 1992b] that more than 30% of a chip power is typically dissipated in the input/output pins and drivers. Hence, by increasing the level of integration, more and more components are integrated on the same substrate – resulting in designs dominated by interconnects, while input/output pins are reduced. However, the complexity of the internal interconnect increases according to *Rent's rule* [Verplaetse 2001, Christie & Stroobandt 2000], which is an experimental rule that presents a power law relationship between the average terminal count T_{avg} and the average module size B_{avg} obtained by a certain net cut minimising method. The rule is written mathematically as

$$T_{avg} = kB_{avg}^{p}, \tag{1.1}$$

[1]Radio frequency (abbreviated RF, rf, or r.f.) is a term that refers to alternating current (AC) having characteristics such that, if the current is input to an antenna, an electromagnetic (EM) field is generated suitable for wireless broadcasting and/or communications. These frequencies cover a significant portion of the electromagnetic radiation spectrum, extending from nine kilohertz (9 kHz), the lowest allocated wireless communications frequency, to thousands of gigahertz (GHz) [*Radio Frequency* 2001].

where k is the Rent coefficient, which corresponds to the average number of ports, and p is the Rent exponent. A high value of p implies that the system has many global interconnections and hence more complex interconnections. The value of p ranges from 0.47 for regular structures such as RAM to 0.75 for complex modules such as full custom VLSI modules.

For example, a fully integrated digital radio has one RF interface pin and one analog output. The total number of interface pins is reduced, while the internal interconnection has increased dramatically. Hence, the amount of power dissipated in the input/output pins is greatly reduced as the number of interface pins are greatly reduced compared to a non-integrated system [Stroobandt 1999].

Mixed signal systems are designs that utilise both analog and digital representations with optimum partitioning of the system to use either of these representations to achieve the required performance specifications [Sanduleanu 1999, Reader *et al.* 2000, Gielen 1998]. Such a concept is referred to in the literature in a number of ways such as analog and mixed signal circuits [Hafed *et al.* 2002, Sajid *et al.* 2001], mixed analog-digital design [Sansen 1998, Choi & Bampi 1999] and sometimes as analog-digital mixed design [Nagata & Iwate 2000]. Even though in mixed signal systems the digital part usually dominates in size, the analog part dominates the interface side as the world we live in is *analog* in nature. To provide interfaces, analog circuits such as amplifiers, filters, analog-to-digital converters (ADC) and digital-to-analog converters (DAC) are commonly used. As demand for the digital part is increasing, fabrication foundries tend to optimise their process for digital circuit fabrication by scaling their fabrication processes. This has resulted in improvements in digital circuitry performance but with adverse effect on analog functionality. The aim of this research is to devise new design techniques for mixed signal circuits in standard complementary metal oxide semiconductor field effect transistor (CMOS) technology to provide improvements in the performance of portable systems in terms of cost, power consumption and reliability. The term 'standard CMOS technology' refers to a CMOS technology with no special elements, devices or fabrication steps.

CMOS technology is the most widely accepted microelectronic fabrication technology. This technology was accepted because it not only provides the low cost and simple fabrication processing steps compared to other technologies, such as GaAs and bipolar technologies, but also allows the integration of analog, digital and RF circuitries. More specifically CMOS technology provides (1) very high density integration of digital circuitry, (2) approximately zero static power dissipation, (3) integration of analog and digital circuitry, (4) integration of some RF circuitry, and (5) low fabrication cost. However, as CMOS was originally developed for digital circuitry (and not for analog or RF circuitry) design

techniques to address the potential integration of analog and RF circuitry become of critical importance in mixed signal systems. It has become a major research activity lately to develop new design techniques to integrate analog and RF circuitry using CMOS technology – this is highlighted in the review paper by Takagi [2001]. Takagi's paper, which surveyed more than 200 articles, reviews analog circuit research in the 1990's from an academic viewpoint with emphases on what will become important in the 21st century. The frequency range of interest from this research point of view extends from the audio frequency range up to hundreds of megahertz.

CMOS technology provides a number of basic components for system designers. Such components are nMOS and pMOS transistors, capacitors, resistors and inductors. The last two components are costly to integrate as they suffer from a wide spread in parameters in the case of resistors, while providing a very low quality factor Q in the case of inductors, in addition to the large area requirements of these elements. The application domain for this research is radio frequency identification systems, however the developed techniques are generic and can readily be applied to applications such as artificial vision, biomedical devices and neural networks.

1.2 Low Power Mixed Signal Technology

In mixed signal applications it is necessary to reduce the power dissipation, hence reducing thermal management problems, of both the analog and the digital parts of the system, even when the source of power is not a battery. In this research, the definition of low power is adopted from Sanduleanu [1999], which defines a low power analog circuit as "the design within the specifications with the minimum possible power consumption by using the most efficient architecture." Power reduction in mixed signal applications can be achieved at a number of levels [Lidsky & Rabaey 1994, Chandrakasan *et al.* 1992a]. These levels are

- ***Fabrication Process Level*:** This is achieved by the development of devices that have high driving current, multiple threshold voltages, small geometries and reduced parasitics. Power reduction at this level has led to the development of new devices such complementary GaAs and Silicon on Sapphire to reduce the power consumption level.

Table 1.1. The research contributions for low power mixed signal design techniques. The techniques are sorted according to the power reduction level they are targeting.

Mixed Signal Low Power Design Techniques			
Fabrication Process Level	**Circuit Level**	**Architecture Level**	**Algorithmic Level**
	Controlled Conductance Devices		
	New AC Coupling		
	Topology for Converting Grounded Resistors to Floating Equivalent		
	Controlled Current Bleeding		
	Digital Trimming Techniques for Opamps		
Mixed Signal Neuron MOS			
	Gray Code Generation		

- ***Circuit Level:*** This level involves the development of circuit techniques to minimise number of devices, switching activity and supply voltage. This is achieved through the development of new logic style in case of digital circuits such as complementary pass transistor logic CPL [Munteanu *et al.* 2000] and charge recycling clocking for adiabatic logic [Psilogeorgopoulos *et al.* 2000] and new circuits techniques for the analog part. This research focuses on power reduction by addressing mostly this level of power reduction.

- ***Architectural Level:*** This involves the use of architectures that utilise parallelism and/or pipelining [Badawy & Bayoumi 2002], power management techniques and the reduction of number of busses [Chandrakasan *et al.* 1992a]. This approach resulted in a trade-off between hardware size and power reduction level.

- ***Algorithmic Level:*** This involves the trade-off between hardware size and software coding, development of codes for minimum switching activity [Ramprasad *et al.* 1999] and critical path reduction [Rabaey *et al.* 1995].

The supply voltage for CMOS circuits is a critical parameter in power reduction of mixed analog-digital circuits. It has been demonstrated in [Stan 2001, Bhavnagarwata *et al.* 1998, Chandrakasan *et al.* 1992b] that a sub-one volt supply voltage can be used for digital circuits. However, the supply voltage for analog circuits should be sufficiently large to enable the operation of CMOS circuits at satisfactory speed with good dynamic range of operation. The minimum supply voltage for analog circuits should be greater than the sum of the input signal voltage swing V_{swing} and the MOS transistor threshold voltage V_{th} and the overdrive voltage for MOSFET [Bult 1999, Castello *et al.* 1995]. The supply voltage requirement depends on the circuit's (a) topology, (b) type and (c) specifications. For example, the reference voltage for the ADC reference circuits shown in Figure 1.1 is 3 times the drain saturation voltage $V_{d,sat}$ plus one V_{th} plus the input signal swing. However, if the circuit is a folded cascode operational amplifier the minimum supply voltage required is 4 times of $V_{d,sat}$ [Bult 1999]. In a basic current cell for a DAC, the minimum supply voltage is 3 times of $V_{d,sat}$. If the maximum input signal swing for these circuits is in the order of 1.25 Volt, $V_{d,sat}$ is in the order of 250 mV, and the threshold voltage is in the order of 750 mV, then the minimum supply voltage for the ADC reference circuit is 3 Volt, 2.25 Volt for the operational amplifier and 2.0 Volt for DAC basic cell.

The previous examples illustrate that the supply voltage is function of the circuit's topology, type and specifications. Accordingly, a 3 Volt supply is high enough to enable the integration of different types of analog circuit within a digital environment. Another

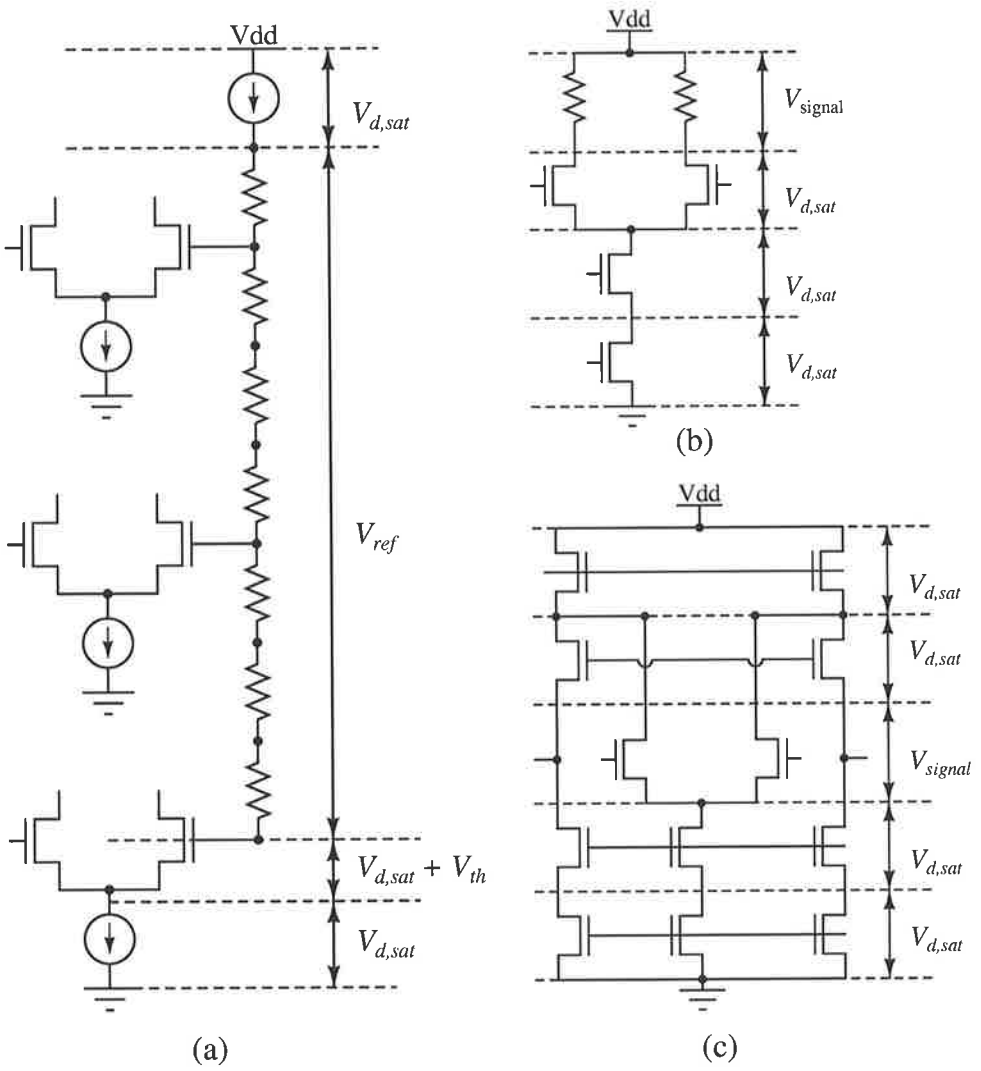

Figure 1.1. Voltage headroom for various analog circuits modules. The voltage headroom for the ADC reference circuit in (a) is $3V_{d,sat}$ plus V_{th}, for the folded cascode amplifier in (b) is $4V_{d,sat}$, while for the DAC basic current cell in (c) is $3V_{d,sat}$.

factor that has strengthened the argument for around a 3 Volt supply is the battery technology. As these devices come in primary cells with nominal voltages ranging from 1.2 to 3.6 Volts as shown in Table 1.2, so only specific values of voltage can be used. Consequently, analog designers find themselves obliged to design analog circuits operating at lower supply voltages to cope with the supply voltage scaling of digital circuits, allowing analog circuit integration with digital circuits on the same substrate using a unified supply voltage. In contrast to digital circuits, supply voltage reduction of analog circuits can result in further power dissipation. This is because lower supply voltage tends to decrease

Table 1.2. A list of nominal voltages for various chemical battery technologies. The list shows values of nominal voltage around 1.2 V, 2.3 V, and 3.3 V

Chemical Technology	Nominal voltage, Volt
LiIon	3.6
Li Metal 3.0	3.0
NiCAD	1.2
NiMH	1.2
Rechargeable Alkaline	1.4
NiZn	1.65
Supercapacitor	2.3

the performance of the analog circuits and in order to maintain the same speed, gain and linearity the trade-off is an unfortunate increase in power dissipation.

1.3 Problem Definition

Mixed analog-digital circuits specifications are a function of the targeted application and technology. Hence a unified design technique to implement such circuits is not possible, so the research question is "given a collection of commonly used mixed signal circuit modules, is it possible to come-up with new design techniques for mixed signal modules with emphasis on low power, small area and robustness against process variation?" The answer to this question involves a number of issues that include: What is the targeted application? What is the targeted technology? What are the common mixed signal modules that are commonly needed in mixed signal systems? What are these techniques and at what level they would reduce the system power? Is it possible to devise circuit techniques that are robust against process variation? And how?

In this research the targeted application is in the area of radio frequency identification systems (RFID) with emphasis on the transponder part. *RFID* is defined in [*RFID* 2002] as "a technology that incorporates the use of electromagnetic or electrostatic coupling in the radio frequency (RF) portion of the electromagnetic spectrum to uniquely identify an object, animal, or person. RFID is coming into increasing use in industry as an alternative to the bar code." The reason for concentrating on the transponder part is because it is portable and has to sustain its operation as long as possible using a low cost battery. This type is usually referred to as an *active transponder*. If the power source is a rectified signal from an RF source or a photocell, the transponder is referred to as *passive transponder*.

The common requirements of such systems are a fully integrated system with minimal or no external components connected to the transponder chip, requiring very small silicon area and operating at very low power levels. The targeted technology is CMOS.

The common modules that are needed in RFID systems are also common to other mixed signal applications. These modules are discussed in detail in the following section. Furthermore, new techniques to reduce power consumption at the process fabrication, circuit, architectural and algorithmic levels are discussed in this thesis. At the process fabrication level new device configurations that can be constructed in standard CMOS technology are utilised in the design of low power mixed analog circuits with high precision. At the circuit level the power dissipation is reduced for mixed signal applications through new techniques that reduce the short circuit current and the dynamic power consumptions. At the architectural level, new techniques for circuit real estate reduction and improvements that allow accurate circuit implementation, by exploiting capacitor or current ratios, are presented and discussed. Also the presented techniques can be used in building basic elements for building power management components that shut down parts of a mixed signal system, when these parts are inactive, leading to further power reduction. At the algorithmic level, new techniques to design counting circuits with minimum switching noise and activity are presented and discussed.

In order for the devised techniques to be less susceptible to process variations, the new techniques depend on the relative transistor parameters rather than on the absolute value of these parameters and should be insensitive to second order effects of the transistors such as channel length modulation, mobility reduction and velocity saturation. Furthermore, in some of techniques discussed in this research, the sub-threshold region of operation is utilised to achieve low power operation based on matched transistors.

1.4 Common Mixed Analog-Digital Components

The common digital components needed in mixed mode analog-digital systems are the basic logic functions such as AND, OR, NAND, NOR, XOR, etc. Other sub-modules such as latches, flip-flops, adders, multipliers and digital signal processors (DSP) can be either constructed from the basic digital modules or are provided as basic modules as it is the case with some *field programmable gate array* (FPGA) [Dent 2001, Semiconductor Design Solutions 2002] or *standard cell design* [Youngkou *et al.* 1999]. In order to identify the analog blocks or subsystems that are commonly needed in mixed analog and digital systems, a survey was conducted based on text books [Razavi 2001, Gray *et al.* 2000, Huijsing *et al.* 1997, Michael *et al.* 1994, Gray & Meyer 1993, Allen & Jolberg 1987,

Soclof 85], papers [Sanz *et al.* 2001, Johns *et al.* 1999, Kaminska *et al.* 1997, Chow 1994] and research monographs [The Center for Integrated Space Microsystems 2002, Integrated MicroSystems Laboratory 2002] on analog circuit design and common modules provided in commercial *field programmable analog array* (FPAA) such as Anadigm[2], SIDSA[3] and Lattice Semiconductor[4] – in addition to modules that are needed in the current application domain. These blocks and subsystems are:

- **Amplification Circuits:** These circuits are commonly designed using operational amplifiers and used as the basic generic component in designing most of the needed modules.

- **Data Converters:** Analog-to-digital and digital-to-analog data converters used as the interface between the analog and digital domains. The basic component in the ADC is a high precision comparator with low offset voltage, while high precision switched current mirrors are the basic components for the DAC.

- **Reference Bias Generators:** Various type of current and voltage generators are needed, specially bandgap reference circuits.

- **Phase Locked Loop:** PLLs are commonly used for clock recovery from streamed input data.

- **Oscillatory Circuits:** Stable clock and timing signals with low phase noise.

- **Analog Switches:** This component is used to multiplex and demultiplex analog signals between the different modules.

- **Analog Buffers:** This component is used to buffer analog signals and facilitate inter- and intra-chip communication.

The first two items in the above list are the most common blocks in field programmable analog arrays (FPAA) [Ganesan & Vemuri 1999] with an additional on-chip memory [Klingenbeck 2000] or filters elements [Pankiewicz *et al.* 2001].

Based on the survey, the following modules were identified as the basic modules that are required to design low power mixed analog-digital systems:

[2]http://www.anadigm.com
[3]http://www.sidsa.es/fipsoc.htm
[4]http://www.latticesemi.com

- **Amplifiers** with controlled gain are commonly needed in portable devices where the gain is either set by controlling transistor geometry or controlled as function of auxiliary digital controlling inputs. Both of these types are important because they allow accurate control of the amplifier gain and the control of this gain after the circuit fabrication. Chapter 2 of the thesis is dedicated to new design techniques for controlled gain amplifiers in which the gain is controlled by designing the transistor geometries used in the amplifier. A family of amplifier circuits is presented, with one of these circuits resembling a true low power amplifier. Measured results are also presented as part of that chapter.

- **High Precision Operational Amplifiers** with very low offset voltage are very important common modules. Chapter 3 is dedicated to new design techniques to digitally trim the offset voltage of an operational amplifier whether it is operating in the strong or sub-threshold region of operation. These techniques are applied to the design of high performance comparators with very low offset voltage. Measured results from fabricated test modules show the effectiveness of the techniques in trimming the offset voltage after the amplifier fabrication.

- **Schmitt Trigger Circuits** have been around since 1938 when Otto Schmitt implemented the first prototype. However, the problem of large current consumption of these circuits has not been addressed in the literature [Nagaraj & Satyam 1981, Steyaert & Sansen 1986, Dokic *et al.* 1988, Enning 1990, Pfister 1992, IBM 1986, Dokic 1996, Ramkumar & Nagaraj 1985, Bundalo & Dokic 1989, Ramkumar & Nagaraj 1985, Ramkumar & Satyam 1989]. As this circuit is one of the basic modules in many integrated oscillator designs, new design techniques for a number of families of Schmitt trigger circuits are presented and discussed in Chapter 4. Some members of these families represent true very low power Schmitt trigger circuits with a very small amount of current drawn from the power supply.

- **Mixed Signal Design using Neuron-MOS Transistor** is a new interesting research area [Shibata & Ohmi 1991, Shibata & Ohmi 1992a, Shibata & Ohmi 1993, Kosaka *et al.* 1995, Ohmi & Shibata 1994, Ishii *et al.* 1992, Weber *et al.* 1996, Shibata & Ohmi 1992b, Yang & Andreou 1994]. As transistor scaling is approaching the physical limit set by the atom size, the common trend is to move from VLSI to ultra large-scale integration (ULSI) technology, where the interest is to increase functional density rather than the transistor density per unit area. The neuron-MOS transistor or simply referred to as νMOS, is a possible step toward ULSI technology.

This transistor is more intelligent than the conventional MOS transistor in that the switching of νMOS is a result of a weighted sum of the capacitively coupled input signals to a floating gate. The structure of the device and its application in the design of precision analog circuits are discussed in Chapter 5.

- **Low Activity Counters** such as Gray code counters are preferred in applications in which only one transition occurs when moving from one state to another. In contrast to binary counters, the number of transitions for an n sequence, requires $\sum_{i=1}^{n} 2^i = 2^{n+1} - 2$ transitions. Therefore Gray code counters are preferred as they reduce the switching noise on the common power supply line. Techniques to design binary ripple counters are discussed in literature [McCalla 1992, Pucknell & Eshraghian 1986]. So far, the techniques used to design Gray code counters use either a state machine or simply converting the binary counting to Gray counting by using a group of XOR gates. In Chapter 6, new formulas for the generation of Gray code sequence are discussed in addition to the application of these formulas to the design of new static and dynamic ripple-through Gray code counters are also presented and discussed.

- **Active Floating Resistors** are very important modules in the design of filters and amplifiers. Chapter 7 presents and discusses a new topology to convert most types of grounded resistors into a floating one. The new floating resistor value is equal to the some of the two-grounded resistors. This topology is used in the design of very high value floating resistor in the order of GΩ by utilising the output conductance of the MOS transistors operating in either the sub-threshold or saturation regions of operation. Furthermore, the usefulness of the new topology is demonstrated through the design of very low-frequency band-pass filter for vision and pacemaker applications. High resistance values can be achieved using switched capacitor techniques, however, our floating resistor approach is superior due to the absence of switching noise.

- **Program Mode Detection (PMD) Circuit:** In remotely programmable RFID systems, a circuit that enables the transponder to start in either "program" or "reply" mode is needed [Cole & Grasso 1993]. This circuit is called program mode detection (PMD). The circuit has one input and one output. Under normal power up of the circuit, it starts in one state, however if the supply voltage is interrupted for a short period of time in the order of hundreds of microseconds, the circuit 'comes-up' in another state, which is referred to as program mode. A new method of bleeding

is developed and used in designing PMD circuits. The bleeding principle relies on using two dynamic analog memory cells. The first stores a predefined analog voltage across a capacitor, while the second cell stores the value of a discharge current that is used to bleed the capacitor charge during the supply voltage interruption. A description of the principle in details through designed circuits is presented and discussed in Chapter 8.

1.5 Original Contributions

The research in this thesis has led to a novel design methodology for low power mixed signal systems. The design techniques are applicable to standard CMOS technologies. Table 1.1 lists all of these techniques, classified according to the level of power reduction that they achieve. Furthermore, the research contributions are:-

- **Controlled Conductance Devices:** A new technique to control the conductance of MOS transistors has been devised. Three variants of this technique are:

  1. *Series Transistor Configuration (STC):* In this technique two transistors are connected in series with a feedback path to generate a controlled conductance device. The conductance can be linearised to obtain either a grounded active resistor or current-voltage characteristics similar to the MOS transistor. The characteristics are independent of second order effects such as the channel length modulation. The conductance can be controlled through relative transistor sizes.
  2. *Parallel Transistor Configuration (PTC):* This technique uses two transistors in parallel. The conductance value is also a function of relative transistor sizes ratio.
  3. *Current Mirror Transistor Configuration (CMC):* This technique is an extension of the parallel transistor configuration technique with current mirrors used to control the device conductance.

  The presented techniques are used in the design of controlled gain amplifier circuits where the amplifier gain is controlled by transistor ratios. The parallel transistor configuration technique was used to design a controlled gain amplifier with gain that can be set using auxiliary digital control signals. All the presented techniques have been verified using computer simulations and measurements from fabricated circuits.

- **A New AC Coupling Technique:** A new technique to design an AC coupled amplifier circuit with very high input impedance in the order of GΩ with quick recovery from overload has been devised. The technique provides a well-matched biasing circuit with the amplifier circuit and generates a well-defined operating point. The technique has been verified using computer simulations and circuit fabrication.

- **New Digital Trimming Techniques for Operational Amplifiers:** Three new techniques to digitally trim differential amplifiers have been devised. Some of these techniques require modification of the amplifier architecture to perform the trimming. One of the techniques does not require modification of the amplifier architecture; instead it can be applied through an input buffer circuit. A relation between the number of digital trimming bits and the achieved offset voltage cancellation is derived. All these techniques are verified through computer simulations and measurement from fabricated circuits.

- **A New Technique for Modulated Hysteresis Schmitt Trigger Circuits:** A simple and effective new technique to modulate the hysteresis width of Schmitt trigger circuits has been devised. This technique is presented through the design of a number of novel Schmitt trigger circuits. Some of these circuits have very small short circuit current and a wide hysteresis width using only 5 to 6 transistors. A comparative study between Schmitt trigger circuits presented in this research with those in the literature demonstrates that the proposed circuits offer low power feature, wide hysteresis with good fan-out. Measurement of the low power version is presented.

- **New Techniques for Analog Circuit Design using Neuron MOS Transistor:** New techniques for designing controlled gain amplifier and Schmitt trigger circuits using Neuron MOS transistors have been devised. The characteristics of these circuits are set as a function of capacitor ratios. In contrast to switched capacitor circuits where a circuit characteristics can also be set using capacitor ratios, the presented techniques result in continuous time circuits and do not require a controlling clock. All techniques were verified through simulations and measurements from circuit fabrication.

- **A New Technique for Gray Code Generation:** A novel technique that allows the generation of Gray and binary counting from a normal divide-by-2 circuit has been devised. New recurrent formulas that relate the generation of binary codes to Gray codes are presented. Based on these formulas, a new low power counting

circuits with reduced switching activity, which generate both binary and Gray codes were designed and fabricated.

- **A Novel Topology to Convert Grounded Resistors to a Floating Equivalent:** A novel topology has been devised to facilitate the conversion of any grounded resistor (to the author's knowledge) to an equivalent active floating resistor. The topology uses current mirrors connected in a special way in order to cancel unwanted second order effects to achieve the required cancellation. The topology is used in the design of a new current controlled floating CMOS resistor. This resistor is also used in the design of a very low frequency band-pass filter in the order of 100 Hz for image sensor applications.

- **A New Controlled Current Bleeding Technique:** A new current bleeding technique that relies on using two dynamic analog memory cells has been devised. The first analog cell stores a predefined analog voltage across a capacitor, while the second cell stores the value of a discharge current that is used to bleed the capacitor charge during a supply voltage interruption. This circuit was used in the design of an application specific integrated circuit (ASIC) for RFID systems to facilitate control and communication over a serial communication link. The new technique was verified through simulations and measurements from circuit fabrication.

1.6 Thesis Structure

The thesis is written in a modular structure. Hence each chapter can be read independently. However, there is occasional cross referencing between chapters for the purpose of illustration and comments. For this reason, each chapter has its own list of references. Possible areas of application of the new techniques are presented in each chapter. Chapter 9 summarises the research outcomes and presents suggestions for future research and recommendations. In the next chapter the controlled conductance device will be presented and its use in designing controlled gain amplifier circuit modules that target low power reduction at the circuit level is also presented. The amplifiers have gain in some cases controlled by transistor configuration and in other cases controlled as function of auxiliary digital inputs.

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Chapter 2

Controlled Gain Amplifiers

THIS chapter analyses the first of the new techniques to design mixed analog-digital circuits in CMOS technology. The focus of this chapter is on the design of *controlled gain amplifier* circuits that have gain that is either function of transistor geometry and set during the design process, or is function of a binary control inputs. The attractive features of the presented techniques are low power and small area in addition to the programmability. In addition, matched biasing circuits for the low power version with fast recovery from overload is also presented and discussed. Measurements from fabricated modules are also presented.

2.1 Introduction

In mixed signal analog-digital applications there is a need to amplify an input signal to a level that is sufficiently large either for later signal processing or to trigger a timing circuit. Hence, an amplifier circuit with moderate to high gain is needed in these applications. High gain amplification is readily available in mixed analog-digital circuits using a digital inverter by biasing it in the middle of its DC characteristic. This structure, shown in Figure 2.1, is referred to in [Baker *et al.* 1998] as a push-pull amplifier. This amplifier is attractive in mixed analog digital design because it offers the ability to source and sink equal amounts of current while also achieving rail-to-rail output swing. Hence, highly desirable as an output amplifier. The gain G of this amplifier is given as

$$G = \frac{g_{m_{mn1}} + g_{m_{mp1}}}{g_{d_{mn_1}} + g_{d_{mp_1}}}. \tag{2.1}$$

The above result is expect since mn_1 and mp_1 are common source amplifiers, each driven by the same input signal and both drive the same output. Hence, the transconductance of both transistors add up and the output resistance of the amplifier is determined by the parallel combination of the transistors' output conductances. However, obtaining a stable operating point is not possible due to the large gain of the amplifier (inverter). Even though a dynamic biasing technique is possible by using a control signal [Palmisano & Pennisi 2001, Harb *et al.* 1999, Garrity *et al.* 1991], this approach is not favoured in some applications as this approach does not provide continuous time operation and requires control signals. To continue to utilise the digital inverter as an amplifier, there is a need to reduce its gain. Reducing the width to length ratio of a normal inverter does not produce a considerable reduction in gain, which is very large because the output conductance is reduced at a greater rate than the forward transconductance. These considerations indicate that there is a need to reduce the gain of the inverter using predictable design techniques for controlled conductance devices in order to obtain a sufficiently well-defined gain and operating point amplifier circuits.

This chapter presents and discusses three variants of a new technique for controlled conductance devices, these devices are used in a complementary form to design the controlled gain amplifiers with stable operating point that is independent of second order effects such as *channel length modulation* λ. To achieve high gain while still maintaining a stable operating point, a cascade of AC coupled amplifiers can be used. A new technique to achieve AC coupling with very high input impedance is presented. The presented technique has important characteristics in accelerating recovery from *overload* [Jorges &

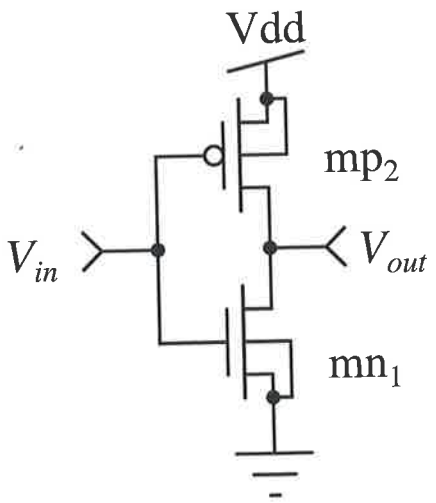

Figure 2.1. Digital inverter used as a push-pull amplifier. This structure uses a nMOS and pMOS devices to drive the output load.

Jummel 1997, Garrity *et al.* 1991], which is a problem in AC coupled amplifiers. The presented analysis is conducted using standard conduction equations. There are two reasons for this. Firstly, the circuit techniques are applicable through a wide conduction region range. Secondly, those parts of the circuit that may be operating in the sub-threshold region exhibits behaviour determined by relative geometry rather than by the conduction parameters particular to the sub-threshold region.

Even though there are a large number of techniques for amplifiers design that use operational amplifier [Razavi 2001, Baker *et al.* 1998] a different approach is adopted in this chapter for the following reasons. In using the operational amplifier there is a need to use either passive or active resistor to set the gain in addition to the need for either current or voltage bias circuits. Hence implementation of these circuits requires extra silicon area compared to the proposed techniques. Also the use of the switched capacitor (SC) approach is fully discarded from the current application point of view, as *SC amplifiers* require (a) large to moderate capacitors size to maintain good matching between the capacitors; (b) non-continuous time operation; and (c) a timing circuit to drive the SC circuits, hence large silicon area with more power dissipation. In addition, while it could be argued that it is possible to design low power circuits using switched capacitors, however, the area requirements of such circuits will be much larger than the area requirements for the proposed techniques given in this chapter.

This chapter is organised as follows: Sections 2.2, 2.3 and 2.4 present the three new variants of controlled conductance devices that can be used in designing controlled gain

amplifiers. Section 2.5 discusses a new technique to design a digitally programmable controlled gain amplifier based on the amplifier circuit discussed in Section 2.3. Section 2.6 discusses a new technique to design a matched voltage bias circuit that has a very high input impedance with a well defined operating point. Section 2.7 reports experimental results for the amplifier circuits discussed in Sections 2.2 and 2.3, while Section 2.8 provides a general discussion and a comparison between the different conductance reduction techniques.

2.2 Series Transistor Configuration

The first controlled conductance device uses *series transistor configuration (STC)* technique as shown in Figure 2.2. The operation conditions required to obtain a grounded conductance are that transistor m_1 should be operating in the saturation region, while transistor m_2 should operate in the linear region. Based on these conditions the current equation for m_1 and m_2, assuming that the corresponding source and the back-gate of each transistor are connected together for all transistors, can be written as

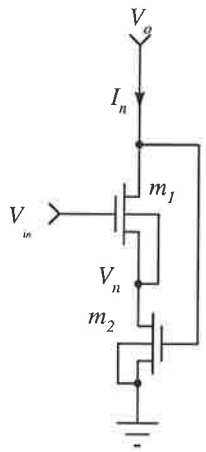

Figure 2.2. A schematic diagram of a voltage controlled grounded conductance. The conductance value of this structure can be controlled through the transistor sizes of m_1 and m_2 and the gate voltage of transistor m_1.

$$I_{m_1} = \frac{\beta_1}{2}(V_{in} - V_n - V_{th})^2 \tag{2.2}$$

$$I_{m_2} = \beta_2\left((V_o - V_{th})V_n - \frac{V_n^2}{2}\right), \tag{2.3}$$

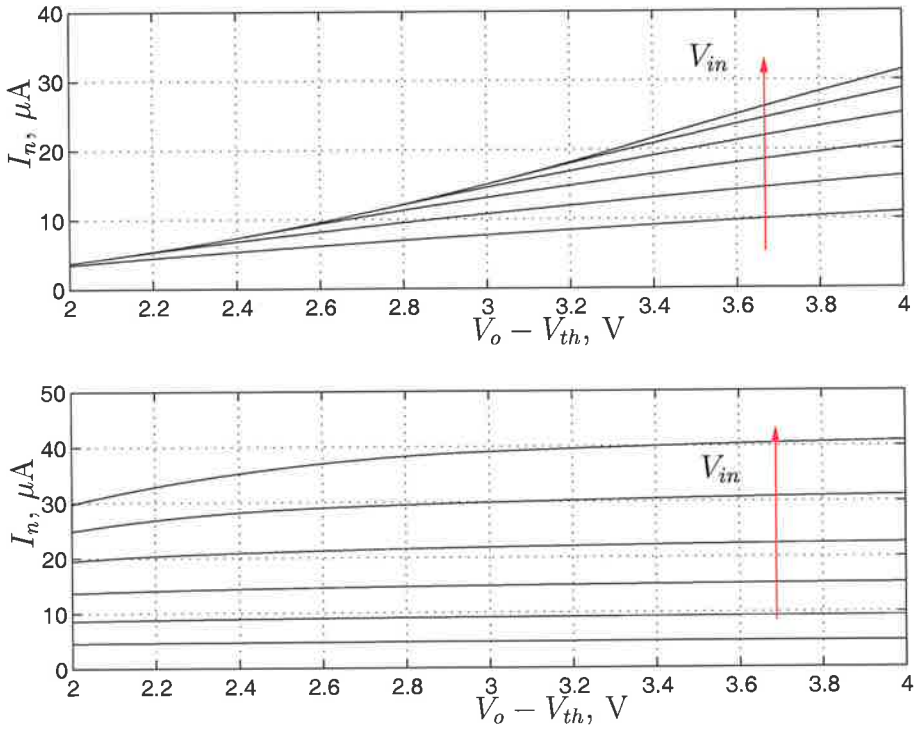

Figure 2.3. The simulation results of the grounded resistor. The upper simulation results were obtained using V_{th}= 1 V, $\beta = 20 \times 10^{-6}$ A/V^2, $S_1 = 10S_2$, while the lower simulation results were obtained using $S_2 = 10S_1$.

where β_i is the intrinsic transconductance parameter of transistor i, V_{th} is the threshold voltage, V_{in} is the input voltage, V_o is the output voltage, and V_n is the voltage of node V_n shown on Figure 2.2. The current passing through this configuration can be found by firstly calculating the voltage at node V_n, which can be calculated by equating Equations 2.2 and 2.3, then solving for V_n. Secondly, this value is substituted in either of Equation 2.2 or 2.3 to calculate the current passing through the configuration as function of V_{in} and V_o. As a simple analytical solution of the current passing through the configuration is not possible, hence the HSPICE circuit simulator is used. Level one was used for these simulations. The parameters used for the first simulation are $\beta = 20 \times 10^{-6}$ A/V^2, $\beta_1 = 5\beta$, $\beta_2 = 0.5\beta$ and V_{th}= 1 V. For the second simulation the parameters are $\beta_2 = 5\beta$ and $\beta_1 = 0.5\beta$. Both of these simulations are shown in Figure 2.3. In both of these simulations the channel length modulation was set to zero to prevent the simulator from calculating it using other available model parameters. These simulations show that the configuration behaves as a grounded conductance when S_1 is much larger than S_2. However, when S_2 is much larger than S_1 the configuration provides characteristics

similar to the MOS transistor characteristics in the saturation region with finite output conductance. This conductance is function of the transistor sizes and independent of the transistor's channel length modulation.

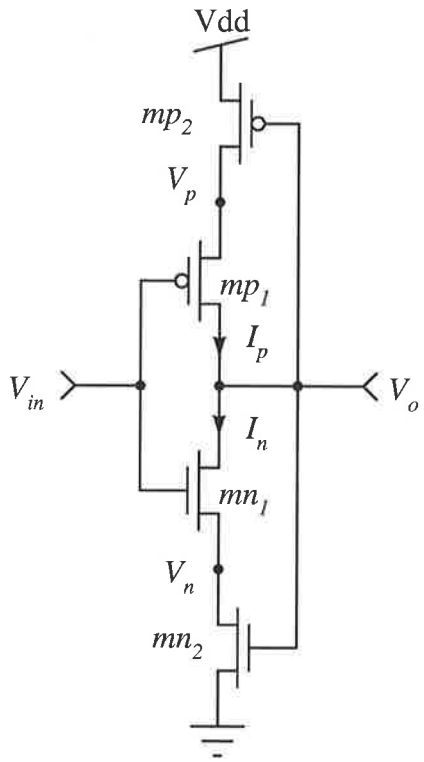

Figure 2.4. A controlled gain amplifier which uses a series transistor configuration (STC). The gain of this amplifier can be controlled by adjusting the transistor sizes of the n-type grounded conductance structures formed by mn_1 and mn_2 and the p-type grounded conductance formed by mp_1 and mp_2.

Based on the above analysis and simulations, if the series nMOS transistor configuration is combined with a complementary pMOS configuration, as shown in Figure 2.4, the resulting amplifier circuit has a controllable and finite output conductance in contrast to the push-pull amplifier discussed earlier. To use the STC in controlled gain amplifier design, the difference in mobility between nMOS and pMOS transistors should be compensated for by modifying the transistor geometries of the pMOS transistors. Then a relation between the amplifier gain and ratios of mn_1 to mn_2 and mp_1 to mp_2 is derived. So, to design a controlled gain amplifier that uses the STC, a chart that relates the amplifier gain to transistor ratios need to be generated. Such a chart is shown in Figure 2.5. This chart was generated using the HSPICE by increasing the width of transistor mn_2 (mp_2), while fixing the W/L of mn_1 (mp_1) and compensating for the difference in mobility between the

nMOS and pMOS type transistors. So, in total three specifications need to be defined to design this amplifier. These specifications are gain, maximum current drawn from power supply and the required bandwidth. All of these factors are interrelated, as reducing the drawn current requires increasing the transistors length of all the transistors resulting in reduced bandwidth. To show the relation between the transistor ratios, gain, current and bandwidth simulation were conducted using symmetrical Level 13 model parameters using HSPICE simulator. *Symmetrical model parameters* mean that the absolute value of the model parameters for the nMOS and pMOS transistors are the same. These parameters are listed in Appendix B. The simulation results that show the relation between the transistor ratios, gain and drawn current from the supply rail are shown in Figure 2.6. These data were obtained from DC simulations. While the AC simulation results that show the relation between transistor ratios, gain and bandwidth are shown in Figure 2.7. According to these simulations, the gain is directly proportional to the drawn current from the supply voltage. The second figure shows the trade-off between the amplifier gain and bandwidth.

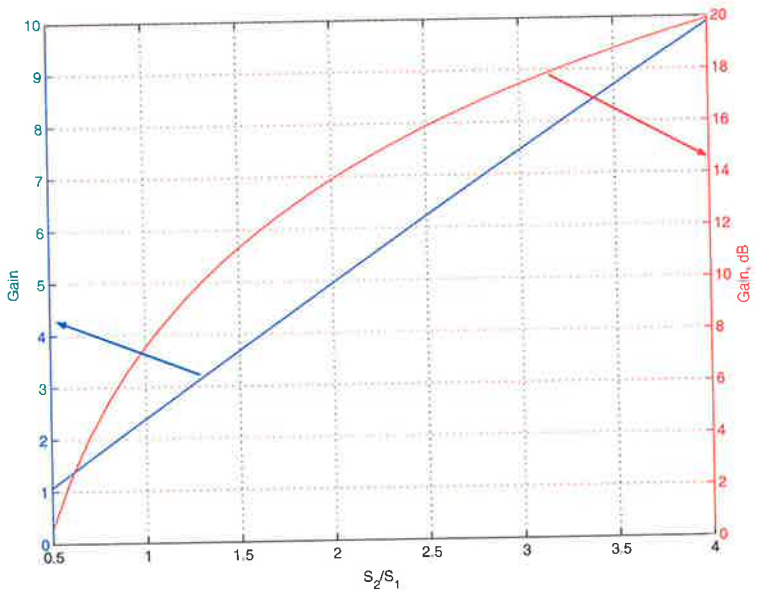

Figure 2.5. DC simulation results of the series transistor configuration amplifier. The x-axis is the width-to-length ratio of mn_2 - S_2 to mn_1 - S_1, while the width-to-length ratio of mp_2 to mp_1 were adjusted to compensate for the difference in mobility. The left hand side y-axis is the simulated amplifier gain, and the right hand side y-axis is the gain in dBs. The simulations show that the amplifier gain is directly proportional to the transistor size ratios.

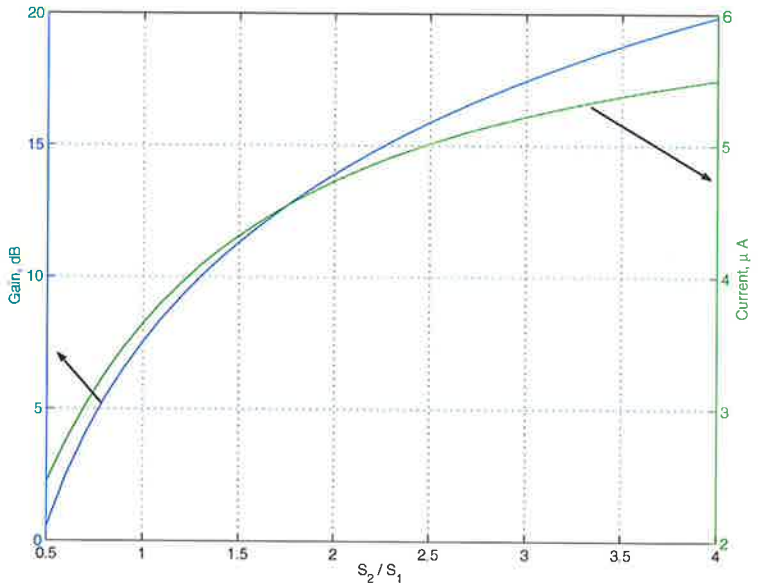

Figure 2.6. DC simulation results of current drawn from the supply rail for the controlled gain amplifier as function of transistor ratios. The x-axis is the width-to-length ratio of mn_2 - S_2 to mn_1 - S_1, while the width-to-length ratio of mp_2 to mp_1 were adjusted to compensate for the difference in mobility. The left hand side y-axis shows the simulated amplifier gain as function of the S_2 to S_1. The right hand side y-axis shows the current drawn from the power supply for STC amplifier. These simulations show that there is a logarithmic relationship between ratio of S_2 to S_1 and the drawn current. They also show that the drawn current from the power supply is directly proportional to the amplifier gain.

The STC amplifier robustness against process variation[5] was measured using available skew parameters for Taiwan Semiconductor Manufacturing Company (TSMC) double poly triple metal 3.3/5 Volt 0.35 μm CMOS technology [Taiwan Semiconductor Manufacturing Company Ltd. - TSMC 1998], which is provided by the MOSIS[6] production service. The simulation results of the STC amplifier using the TSMC skew parameters are shown in Figure 2.8 and the gains are listed in Table 2.1. The transistor sizes used for these simulations (in μm) are 4/20, 12/20, 12/4 and 4/4 for mn_1, mn_2, mp_1 and mp_2,

[5]Here and throughout this thesis we perform first-order variation analysis using the process spread in V_{th}. Typically, the spread in V_{th} values for a CMOS process represents the most dominant source of mismatch.

[6]MOSIS (http://www.mosis.org) is a low-cost prototyping and small-volume production service for VLSI circuit development. Since 1981, MOSIS has provided circuit fabrication for commercial firms, government agencies, and research and educational institutions around the world.

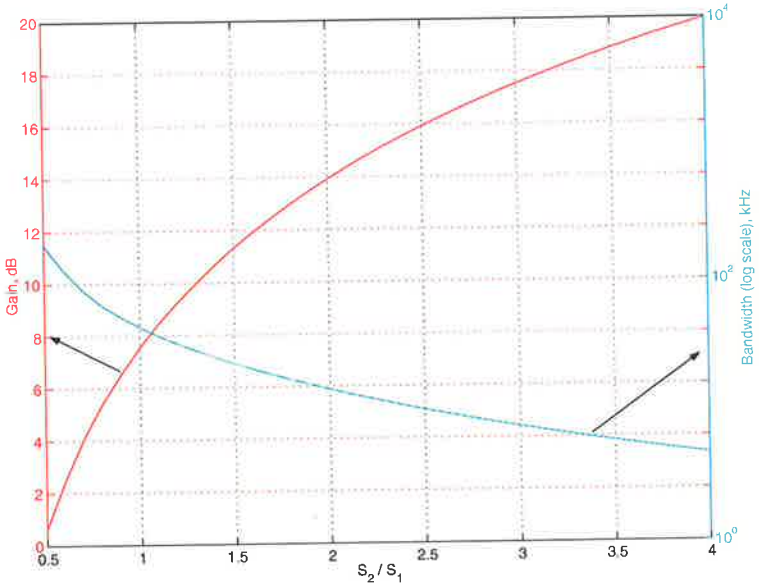

Figure 2.7. AC simulation results of the STC amplifier. The x-axis is the width-to-length ratio of mn_2 - S_2 to mn_1 - S_1, while the width-to-length ratio of mp_2 to mp_1 were adjusted to compensate for the difference in mobility. The left hand side y-axis is the amplifier gain in dBs. The right hand side y-axis is a logarithmic scale showing the amplifier bandwidth in kHz. These simulations show that the STC amplifier bandwidth is inversely proportional to the amplifier gain and the ratio of S_2 to S_1.

respectively. From Table 2.1, the gain variation as function of the skew parameters is less than 1.2%, which is less than 0.7% dB. However, the DC operating point of the amplifier is considerably shifted from half the supply voltage as function of the skew parameters, more on this matter will be discussed in the biasing circuit for this amplifier. Furthermore, the gain variation of the amplifier as function of temperature using the previously mentioned transistor sizes is also considered. Figure 2.9 shows that the amplifier gain varies by less than 0.4 dB for a temperature change from -50 to 100 °C.

2.3 Parallel Transistor Configuration

The second technique to produce a controlled conductance device is we call the *parallel transistor configuration (PTC)*. This technique relies on loading the drain of a MOS transistor with a similar type diode-connected transistor. Hence, the name parallel transistor configuration PTC. The output conductance of the device is a function of the transistor

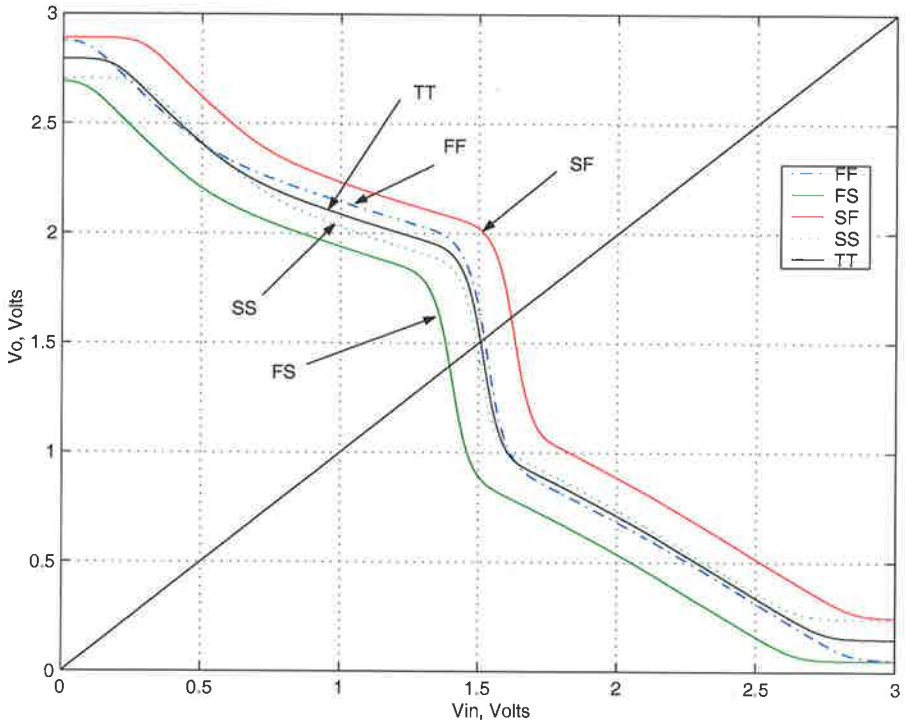

Figure 2.8. Simulation results of the STC amplifier using Taiwan Semiconductor Manufacturing Company (TSMC) skew parameters. These simulations show that the amplifier gain is robust against process variation, however, the process variation results in shifting the amplifier operating point from $V_{dd}/2$.

Table 2.1. The STC amplifier gain as function of the Taiwan Semiconductor Manufacturing Company (TSMC) process skew parameters. These gain values, obtained from simulation, show that the amplifier gain is independent of the global process variations.

Description	Gain	Gain in dB
Typical NMOS Typical PMOS model (TT)	-7.34	17.31
Slow NMOS Slow PMOS model (SS)	-7.25	17.21
Fast NMOS Fast PMOS model (FF)	-7.43	17.43
Slow NMOS Fast PMOS model (SF)	-7.33	17.31
Fast NMOS Slow PMOS model (FS)	-7.33	17.31

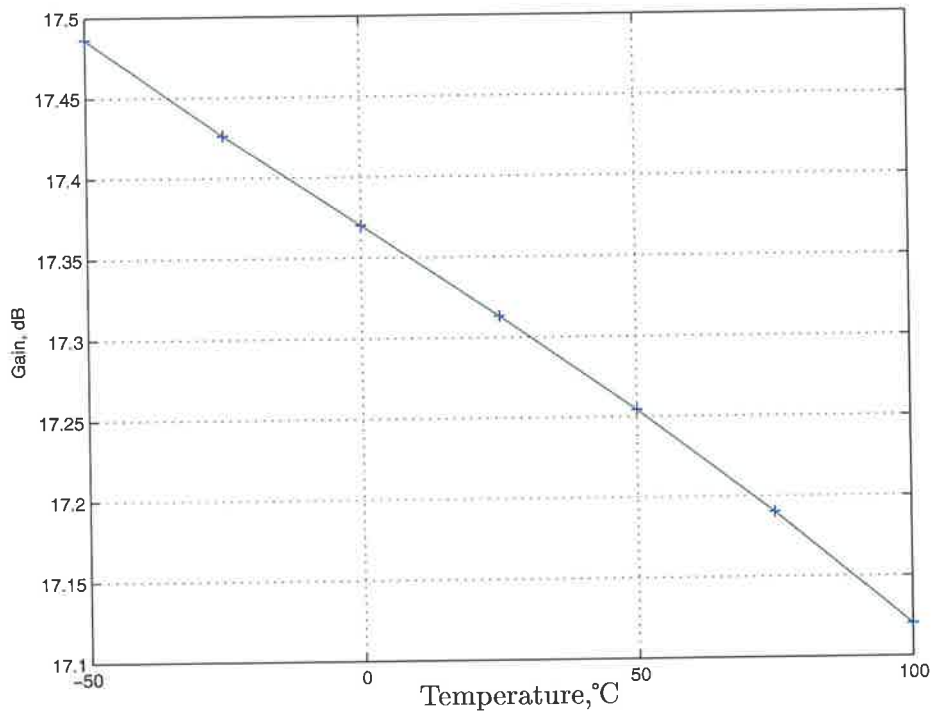

Figure 2.9. Simulation results of the STC amplifier as function of temperature. The temperature was varied from -50 to 100 °C in 25 °C steps. This illustrates that over a 150 °C temperature, the gain varied by less than 0.4 dB.

ratios as shown in Figure 2.10. Use of a complementary structure for this circuit results in a controlled gain amplifier, with gain primarily controlled through transistor ratios.

The low frequency gain of this amplifier can be found analytically by drawing the low frequency small signal equivalent circuit of the amplifier as shown in Figure 2.13. Then, applying KCL at node V_o results in

$$(g_{mmn_1} + g_{m_{mp_1}})v_{in} + (g_{m_{mn_2}} + g_{m_{mp_2}})v_o + \frac{v_o}{r_o} = 0. \tag{2.4}$$

Hence, the small signal gain G can be written as

$$\begin{aligned} G = \frac{v_o}{v_{in}} &= -\frac{(g_{m_{mn_1}} + g_{m_{mp_1}})}{(g_{m_{mn_2}} + g_{m_{mp_2}}) + \frac{1}{r_o}} \\ &\approx -\frac{(g_{m_{mn_1}} + g_{m_{mp_1}})}{(g_{m_{mn_2}} + g_{m_{mp_o}})}. \end{aligned} \tag{2.5}$$

If $g_{m_{m_i}} = g_{m_{mn_i}} = g_{m_{mp_i}}$ and $g_{m_{m_o}} = g_{m_{mn_o}} = g_{m_{mp_o}}$ are set in Equation 2.5, then the gain G can be written as

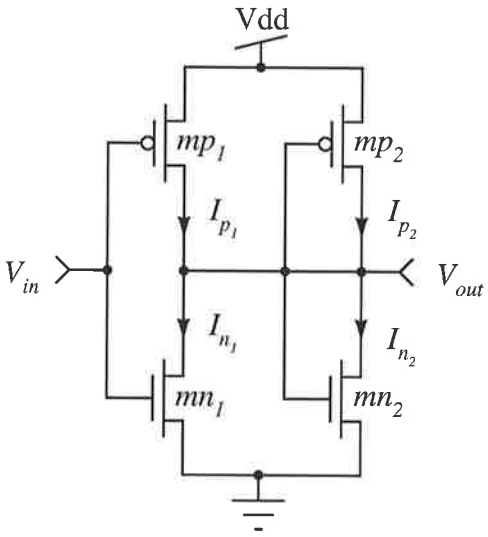

Figure 2.10. A parallel transistor configuration (PTC) controlled gain amplifier. The gain of this amplifier is set by the ratio of transistor mn_1 to mn_2. To have an operating point around $V_{dd}/2$ the width of the pMOS transistors have to be adjusted to compensate for the difference in the nMOS and pMOS mobility.

$$G = -\frac{g_{m_{m_i}}}{g_{m_{m_o}}} = -\frac{\beta_{mn_1}}{\beta_{mn_2}}. \tag{2.6}$$

As seen from Equation 2.6 the gain of the PTC amplifier is function of the transistor geometries and less dependent on process second order effects. This amplifier was simulated to show the DC transfer characteristics of the amplifier and the current drawn from the power supply as function of V_{in}, as shown in Figure 2.11. In these simulations, the lengths of mn_2 were obtained by multiplying 1, 2, 4, 8 and 16 times the length of mn_1, while keeping the ratio of β_n/β_p equal to 1, in order to maintain an operating point at $V_{dd}/2$. Furthermore, the simulated frequency response using the same parameters used for the DC simulation are shown in Figure 2.12. The AC simulation results show that the amplifier has a wide frequency response that extends to the megahertz frequency range, making the amplifier attractive for low to high frequency analog applications.

The robustness of the PTC amplifier against process variation was measured using the TSMC skew parameters. The simulation results of the amplifier are shown in Figure 2.14 and the amplifier gain is listed in Table 2.2. The transistor sizes (in μm) used for the simulation are $mn_1 = 8/2$, $mp_1 = 32.8/2$, $mn_2 = 2/2$ and $mp_2 = 8.2/2$. It is noticeable that the typical gain is less than the expected gain value of 4, predicted by Equation 2.6 by 4%. This is due to the approximation used in the amplifier analysis. Nevertheless,

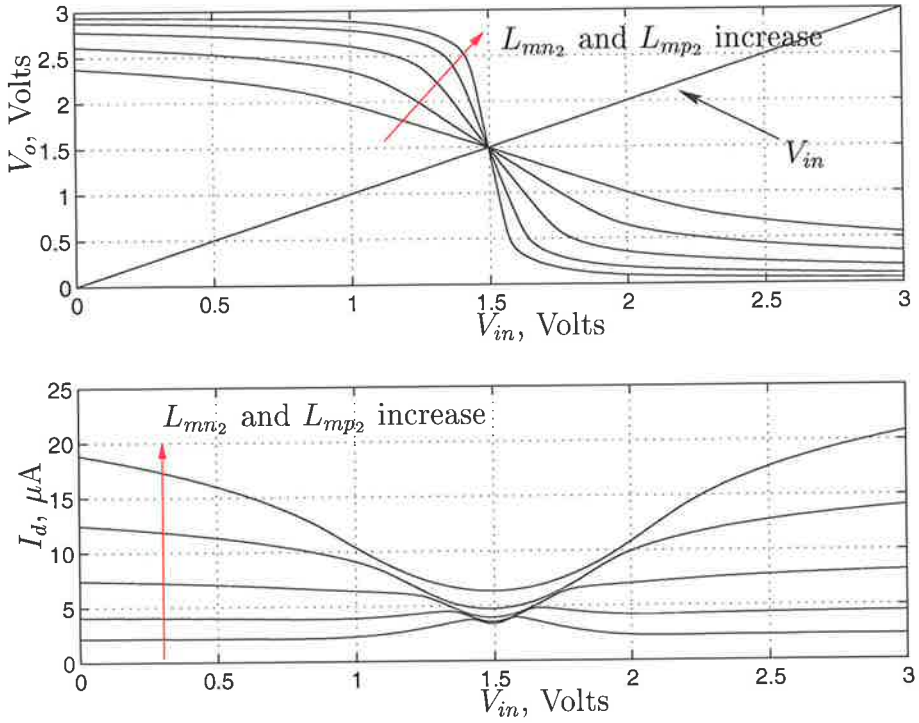

Figure 2.11. Simulation results of the PTC amplifier. The upper simulations show the input-output characteristics of the amplifier with the length L of the load transistors mn_2 set to 6.25 μm, 2 $\times$ 6.25 μm, 4 $\times$ 6.25 μm, 8 $\times$ 6.25 μm and 16 $\times$ 6.25 μm, while maintaining the ratio of β_{n_1}/β_{p_1} and β_{n_2}/β_{p_2} equal to 1. The lower simulations show the current drawn from the power supply as function of V_{in} for the corresponding transistor lengths.

4% is an acceptable error when comparing analytical results with simulation results. The simulations also show that there is a shift in the DC operating point. This shift has to be taken into consideration when designing a bias circuit for this amplifier. Furthermore, the simulation results show a less than 0.7% variation in the circuit gain as function of the skew parameters. In addition, the gain variation of the amplifier as function of temperature was also considered. Figure 2.15 shows the gain variation of the PTC using the previously mentioned transistor sizes. These simulations demonstrate that the gain variation was less than 0.09 dB. This indicates that the amplifier's gain is very robust against temperature and process variation.

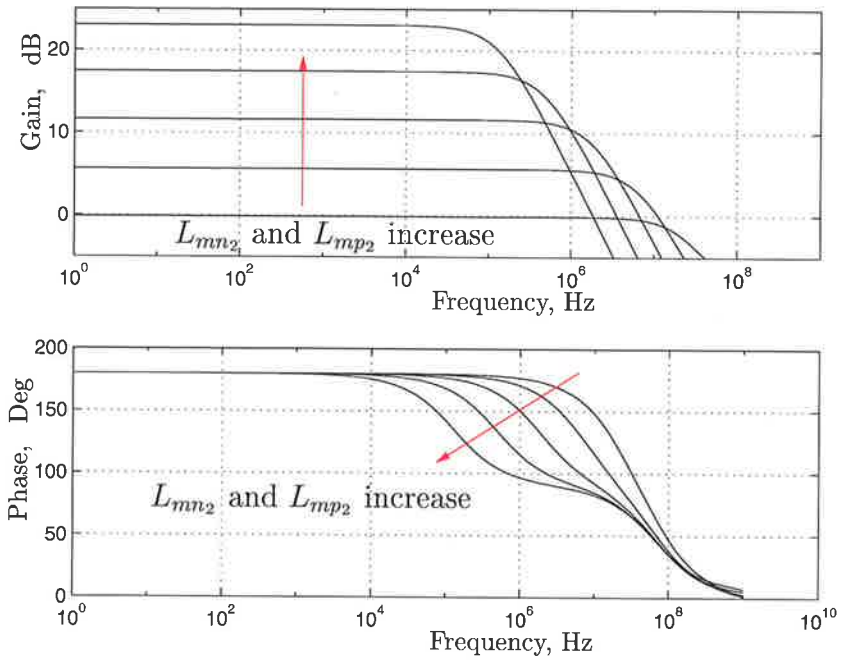

Figure 2.12. Frequency response of the PTC amplifier. The upper simulations magnitude response, while the lower simulations show the phase response simulated with the same sweep parameters used for the DC analysis shown in Figure 2.11.

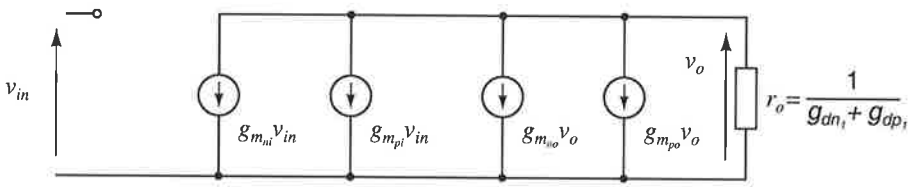

Figure 2.13. Small signal equivalent circuit of the PTC amplifier. In this circuit the output conductance of transistors mn_1 and mp_1 are combined into r_o.

Table 2.2. The PTC amplifier gain as function of the TSMC process skew parameters. These simulations results show that the gain of the amplifier is independent of the global process variations.

Description	Gain	Gain in dB
Typical NMOS Typical PMOS model (TT)	-3.86	11.74
Slow NMOS Slow PMOS model (SS)	-3.88	11.79
Fast NMOS Fast PMOS model (FF)	-3.84	11.68
Slow NMOS Fast PMOS model (SF)	-3.85	11.72
Fast NMOS Slow PMOS model (FS)	-3.87	11.75

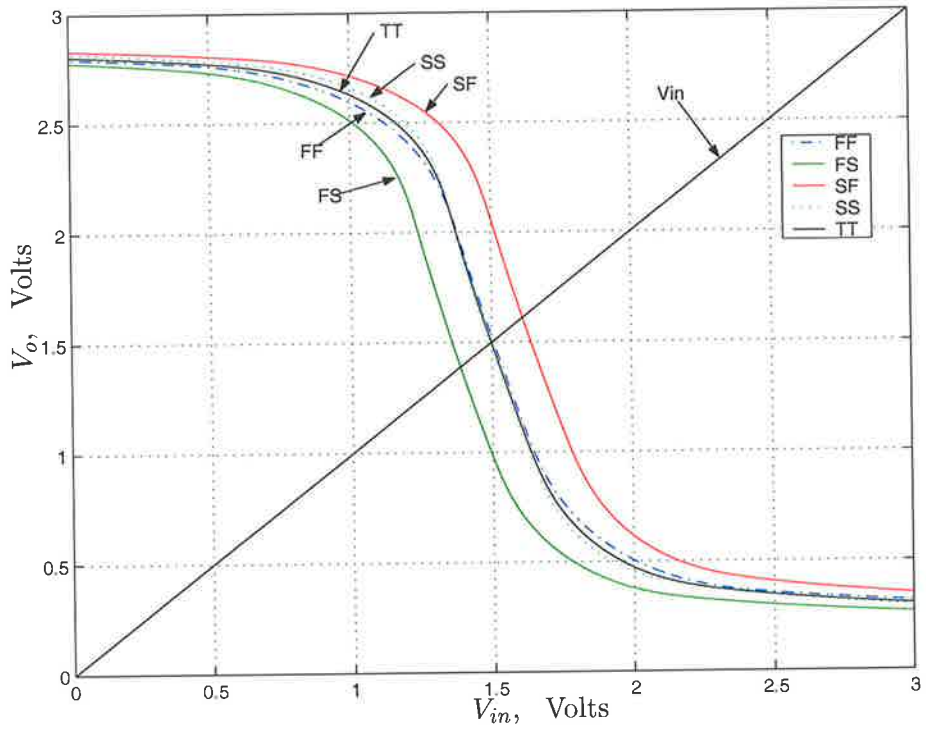

Figure 2.14. Simulation results of the PTC amplifier using the TSMC skew parameters. These simulations demonstrate that the PTC amplifier gain is very robust against process variations.

2.4 Current Mirror Configuration

The third technique to produce a controlled conductance device is similar to the PTC technique, but with current mirrors used to control the forward conductance of the load transistor instead of a direct connection. Hence, we refer to this structure as the *current mirror configuration (CMC)*. In this configuration two groups of current mirrors are needed to provide the correct phases at the gates of load transistor mn_6 to obtain a positive load conductance. The analysis for this device is presented as part of the controlled gain amplifier.

A controlled gain amplifier can be designed using a complementary structure of the controlled conductance device as shown in Figure 2.16. The gain of the amplifier can be found analytically by writing the current equations of all the transistors in terms of the forward conductance or intuitively from the analysis given in the previous section to give the result given in Equation 2.7, assuming that the operating point of the amplifier is at $V_{in} = V_o = V_{dd}/2$ and $\beta_{n_i} = \beta_{p_i}$, where i is the transistor number in Figure 2.16,

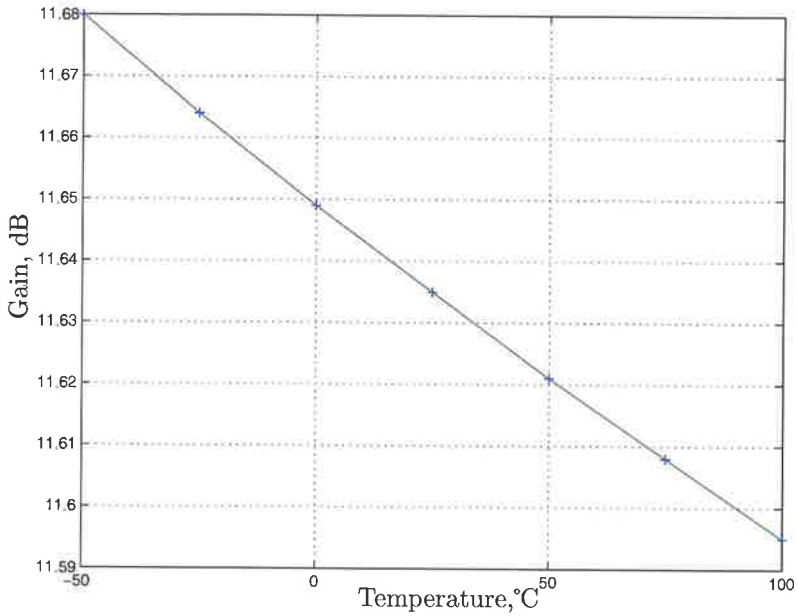

Figure 2.15. Simulation results of the PTC amplifier as function of temperature. The temperature was varied from -50 to 100 °C in 25 °C step. These simulations show that the amplifier gain is virtually independent of temperature over a wide temperature range.

$$G = -\frac{\beta_{mn_1}\,\beta_{mp_3}\,\beta_{mn_5}}{\beta_{mn_2}\,\beta_{mp_4}\,\beta_{mn_6}}. \tag{2.7}$$

The DC simulation results for the CMC amplifier are shown in Figure 2.17. The simulations show that the amplifier has a wide output dynamic range and its current consumption is larger than the PTC configuration. The AC simulation results shown in Figure 2.18 indicate that the amplifier exhibits gain peaking which can lead to instability problems. This is due to difference between the propagation delay through the first and second current mirror structures, and the output signal at V_o. Once the propagation delay becomes comparable to the reciprocal of the maximum frequency component in the input signal there is a potential for instability. The amplifier gain can be stabilised by using a feedback capacitor from the output to the input as shown by the solid line in the simulation results shown in Figure 2.18. Further analysis to prevent the instability is not presented as this circuit is not attractive for low power applications, has a higher current dissipation and uses larger silicon area compared to the previous amplifier circuits.

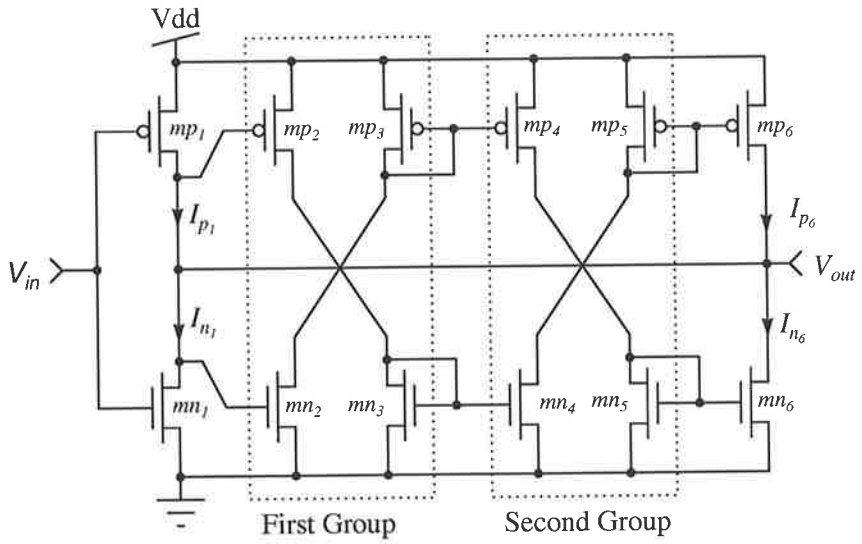

Figure 2.16. A current mirrors configuration (CMC) controlled gain amplifier amplifier. In this configuration two groups of current mirror are used to obtain the right phase at V_{out}. The gain of this amplifier is given by Equation 2.7.

Without performing any skew parameter simulation on the amplifier that uses the CMC technique, the robustness of this technique against process variation is very low at both local and global variations. For the local variation, mismatch in the transistor forming the current mirror will cause a shift in the amplifier characteristics. Furthermore, global variation represented through skew parameters will also cause a shift in the amplifier characteristics. As a result this amplifier will not find good use in most applications since (*i*) it is more susceptible to process variation compared to the STC and PTC amplifier circuits, (*ii*) requires larger silicon area and consumes more current than the other configurations due the increased number of transistors in parallel.

2.5 Digitally Programmable Conductance Configuration

As the conductance of all the previous circuits has to be fixed during the fabrication process, the ability to change the conductance value after its fabrication gives far more flexibility for the designer, especially when these conductances are used in amplifiers design. Such an amplifier is very attractive in a wide range of applications, especially when the gain can be controlled as function of digital control signals. However, not all the previously discussed controlled conductance techniques lend themselves to the concept of *digitally programmable devices*. The parallel transistor configuration and

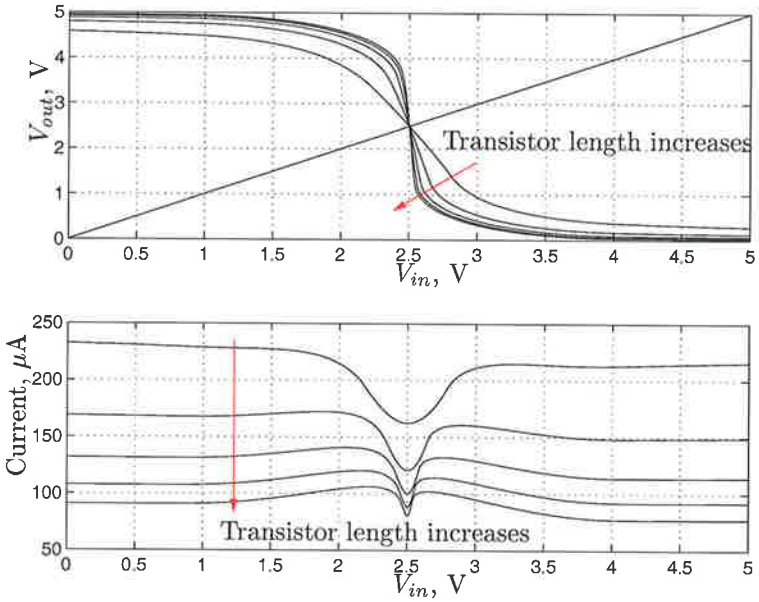

Figure 2.17. DC simulation results of the CMC amplifier. These simulations show the input-output characteristics of the CMC amplifier while sweeping the lengths of mn_2, mp_2, mp_4, mn_4, mn_6 and mp_6 from 27 μm to 54 μm in 9 μm steps, while the widths of all the load transistors are kept at 12 μm, and the W/L of the input transistors mn_1 and mp_2 are set to 12 μm/6.25 μm and 18 μm/18 μm, respectively.

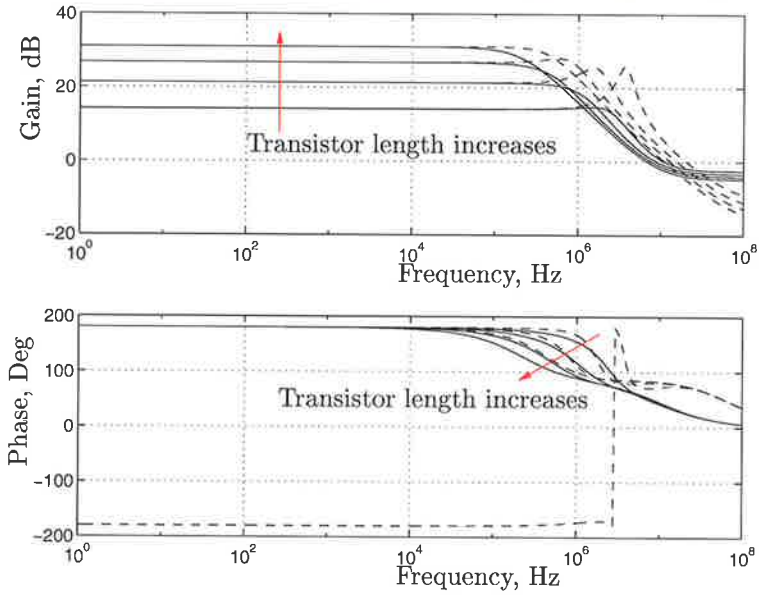

Figure 2.18. Frequency response of the CMC amplifier. This amplifier was simulated with the same sweep parameters used for the DC analysis shown in Figure 2.17. The upper simulations show the frequency response of the amplifier, while the lower simulations show phase response of the CMC amplifier circuit. The dashed line represents the simulation results with no compensation, while the solid one shows the simulation results after compensation.

Table 2.3. The gain of the digitally controlled amplifier as function of the digital input combinations. This table that the amplifier gain is function of the the auxiliary digital inputs B_0 and B_1.

B_1	B_0	Gain	Gain in dB
0	0	Very high	Very high (Inverter gain)
0	1	4	12
1	0	2	6
1	1	4/3	2.5

current mirror configuration techniques discussed in Sections 2.3 and 2.4 are best suited for such a concept[7]. This *digitally programmable PTC* concept is best illustrated through designing a controlled gain amplifier. This amplifier has digital control signals that are used to control the connection of a group of inverters as part of the amplifier load, as shown in Figure 2.19. The gain of this amplifier as function of the digital control signals, if a binary weighting scheme is used, can be written as

$$G = \frac{1}{\sum_{k=1}^{N} B_i \frac{1}{2^k}}, \tag{2.8}$$

where N is the number of parallel inverter structures and B_i represents the binary weight value, which is either 1, if the digital input is high, or zero if the digital input is low. It is assumed in Equation 2.8 that β_{n_i} and β_{p_i} are set to be equal to maintain an operating point at $V_{dd}/2$, and $\beta_{n_k} = \beta_0/2^k$. Also, in the above equation a binary weighted scheme is used. Note that the technique is still valid with any other weighting scheme. Based on Equation 2.8, the gain for a digitally programmable amplifier composed of two load inverters can be written as function of two digital inputs as given in Table 2.3. The amplifier circuit shown in Figure 2.19 was simulated using readily available parameters. Figure 2.20 shows that these simulation results are consistent with the those presented in Table 2.3. It should be mentioned that such configuration will have a large load capacitance as a result of including the gate capacitances of all the inverters whether they are part of the amplifier load or not. A better configuration would be to fully isolate the unselected loads from the output node as shown in Figure 2.21.

[7]The derivative of a digitally programmable technique from the CMC technique is not discussed here because of its high power dissipation and large silicon area.

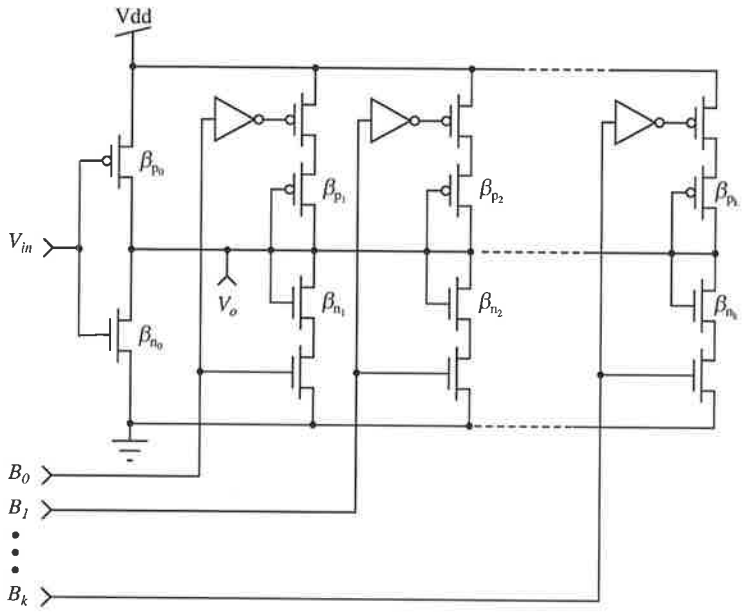

Figure 2.19. A schematic diagram of a digital soft-hardware controlled gain amplifier. The amplifier gain is controlled as function of the auxiliary digital input signals B_0 to B_k. The gain of this amplifier is given by Equation 2.8.

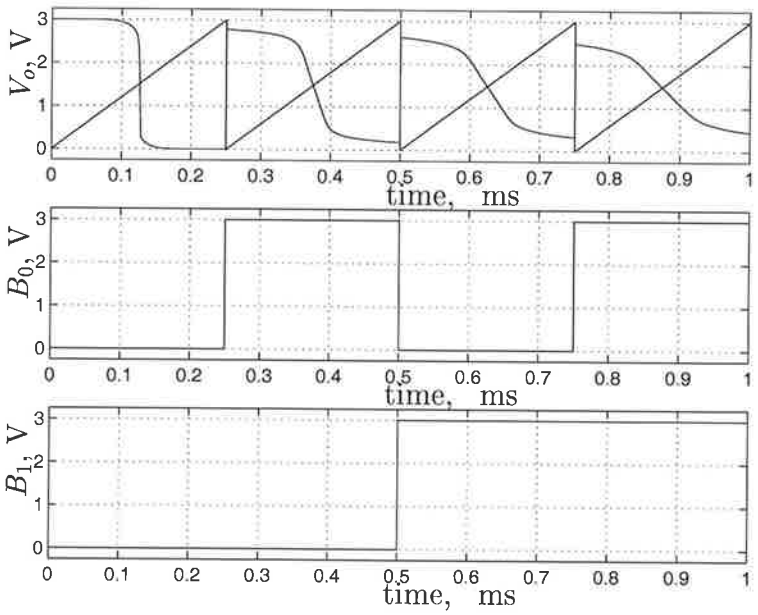

Figure 2.20. Simulation results of the digitally programmable controlled gain amplifier. These simulations show that the digitally programmable amplifier gain can be changed dynamically every 250 μs using the auxiliary digital inputs B_0 and B_1. For B_0=0 and B_1=0, the amplifier gain is equal to the inverter gain composed by β_{n_0} and β_{p_0} on Figure 2.19, when B_0=1 and B_1=0 the amplifier gain is set to 4, when B_0=0 and B_1=1 the amplifier gain is set to 2, and when B_0=0 and B_1=1 the amplifier gain is set to 4/3.

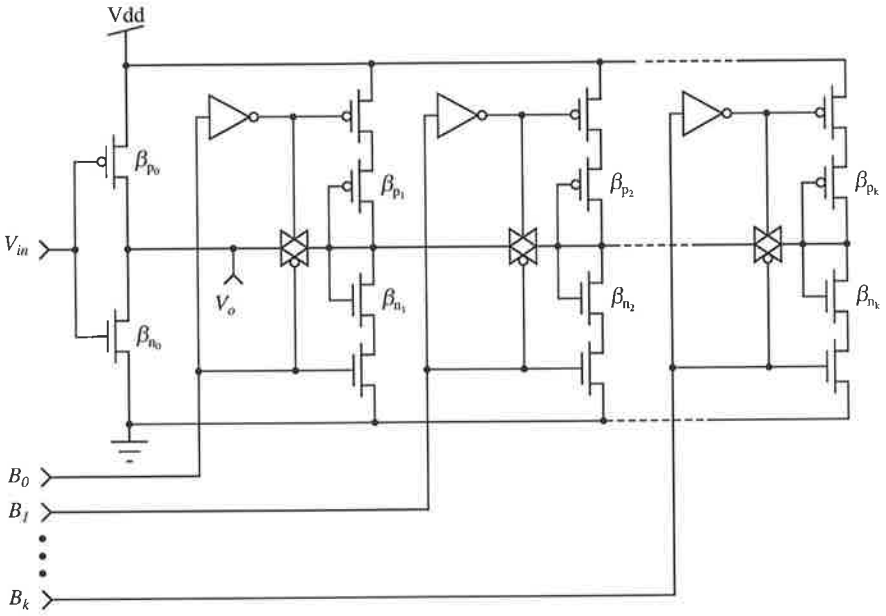

Figure 2.21. A schematic diagram of a digital soft-hardware controlled gain amplifier with less load capacitance. In this schematic extra transmission gate are used to isolate the unselected load inverters. This improves the AC performance of the amplifier by increasing its bandwidth of operation.

2.6 Biasing Circuits

To use the low power amplifier designed in Section 2.2 in an AC coupled application [Lobodzinski & Kuzminska 1998] with a small value of coupling capacitor, two similar biasing circuits were designed. The input signal to the amplifier is AC coupled to both the biasing circuit and STC amplifier. It is more convenient to firstly present the circuits and then explain the general principles on which they were designed.

The first circuit uses a *pn* junction while the second uses a diode-connected MOS transistor. The application requirements for these circuits are: (1) a well defined operating point, (2) a very high input impedance for positive voltage swing ($\gg$100 MΩ), (3) a lower path impedance for negative voltage swings to achieve fast recovery after large positive input transients, (4) to be matched with the STC amplifier, and (5) to consume a very small amount of current from the power supply.

The basic structure of the bias circuit consists of the same STC amplifier with two diodes and two current sources, as shown in Figure 2.22.a. The two diodes are connected back to back so that the voltage drop at D_1 will be cancelled by the voltage drop at D_2, while independent but equal current sources are used to establish the operating points of

the diodes. When there is no signal applied at V_{in}, the input impedance r_d at V_{ob} can be calculated as

$$r_d = \frac{1}{g_{d_{diode}} + g_{d_{mos}}} = \frac{1}{\frac{i_{ds}}{\eta U_t} + \lambda i_{ds}} \approx \frac{\eta U_t}{i_{ds}} \tag{2.9}$$

where

$g_{d_{diode}}$	is the output conductance of D_1;
$g_{d_{mos}}$	is the output conductance of mn_r;
I_{ds}	is the nMOS drain current which passes through the pn junction;
U_t	is the thermal voltage;
η	is the emission factor of the pn junction;
λ	is the MOS transistor channel length modulation parameter.

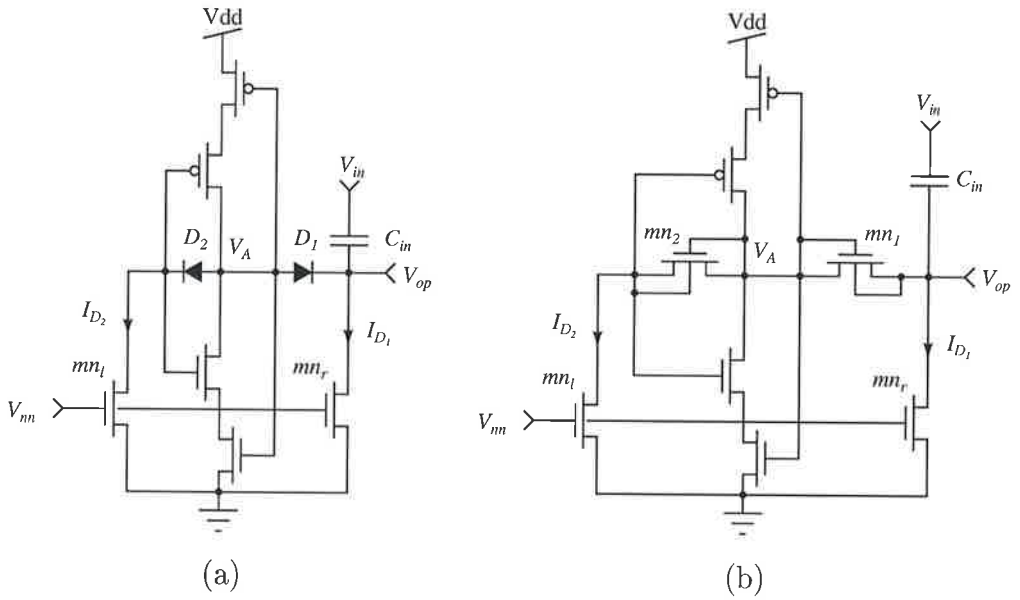

Figure 2.22. Biasing circuits for the STC amplifier. Two configuration can be used. The first (a) uses pn junctions, while the second (b) uses diode-connected MOS transistors. The pros and cons of each structure are discussed in the text.

For a 10 pA current source the input impedance is ~2.5 GΩ. However, when an input signal with a positive transient is applied at V_{in}, the diode D_1 with a 10 pF coupling capacitor provides a very large time constant in the order of 25 ms. The requirement for low bias current can be elevated while still maintaining very high output impedance by using other current mirror configurations such as Wilson, improved Wilson, cascode, etc.

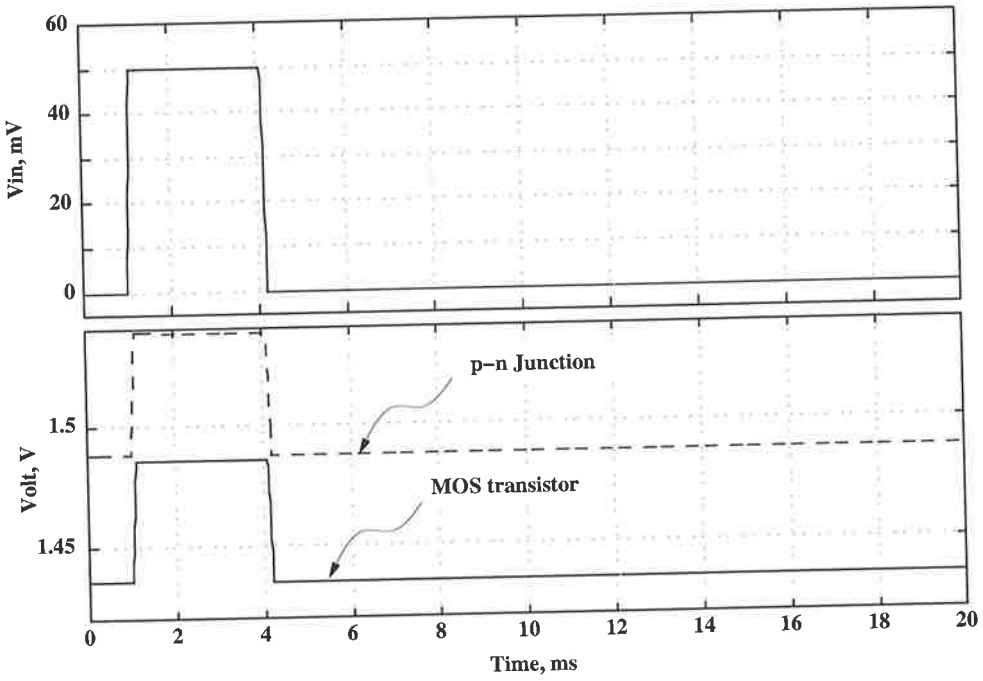

Figure 2.23. Simulation results of the pn and MOS transistors STC biasing circuits. The upper waveform shows a pulse of 50 mV amplitude and delayed by 1 ms. This pulse is used as an input for the two biasing circuits shown in Figure 2.22. The simulation results shown in the lower panel show two outputs. The dashed waveform correspond to the biasing circuit that uses pn junction, while the solid waveform correspond to the biasing circuit that used a diode-connected MOS transistor. These simulations show that the bias circuit with the diode-connected MOS transistor produces a larger offset from the bias circuit that uses the pn junction. This is due to the larger voltage drop across the diode-connected MOS transistor.

The third requirement is accomplished as follows. When a large negative transient is applied to the bias circuit, the recovery from an immediately preceding large positive transient will move diode D_1 more into the forward bias direction. Hence, the dynamic resistance will be momentarily reduced. Therefore the effective input resistance at V_A will be the input resistance at the anode of the diode D_1, which is in the range of 1.2 MΩ. As a result, the coupling capacitor discharges during the recovery from the transient with a desirably very small time constant (12 μs). The simulation results for this circuit are discussed later in this section.

A similar bias circuit was designed using diode-connected MOS transistors to replace the pn junction diodes in the previous circuit as shown in Figure 2.22.b. Still the same

principle of operation is applicable. For both circuits, the principles of optimum matching [Vittoz & Fellrath 1977] is employed by using the amplifier in the construction of the biasing circuit and using diode D_2 to cancel the voltage drop across D_1. The simulation results of the two biasing circuits with a 50 mV, 3 ms input pulse, delayed by 1 ms, are shown in Figure 2.23. The simulations show that the bias circuits have output offset voltages that are function of the voltage drop across the diode divided by the gain of the amplifier structure. The bias circuit that uses a *pn* junction has a very small voltage drop, while the biasing circuit that uses a diode-connected MOS transistor, exhibits a larger offset, which could drive the amplifier operating point off the amplifier dynamic range region of operation. Therefore the bias circuit which uses a *pn* junction is very much preferred. The recovery time from a negative transient for the circuit which uses diode-connected MOS transistors is faster than the one that uses *pn* junctions. The difference in time is traceable to the fact that when the nMOS transistor emerges from the sub-threshold region, its conductance initially increases more rapidly than that of an equivalent diode due to a large *subthreshold slope factor* n in weak inversion [Vittoz & Fellrath 1977] which is in the range of 1.3 to 2, compared to the *pn junction emission factor* η, which is in the range of 1.1 to 1.2 [Al-Sarawi 1991].

2.7 Experimental Work

2.7.1 Measurement of the STC Amplifier

As the prime interests of this research are techniques that result in low power circuits with small area, the amplifier circuit with bias circuit shown in Figure 2.24 were fabricated. The corresponding micro-photograph of the fabricated amplifier with its bias circuit, without the input coupling capacitor, is shown in Figure 2.26. The width to length ratio (in μm) of the transistors used in the fabricated amplifier are $mn_1 = 4.8/118.2$, $mn_2 = 12/25.2$, $mp_1 = 4.8/36$ and $mp_2 = 12/8.4$. The diodes in the bias circuit were implemented using a floating n-well as illustrated by Figure 2.25.

The measurements were conducted at 3 and 5 Volt supplies to investigate the variation of the amplifier gain and the bias circuit operating point as function of supply voltage. The first group of measurements performed on the amplifier were to measure the output characteristics of the amplifier as function of the input signal. The measurement at 3 Volt supply is shown in Figure 2.27, while the measurement at 5 Volt supply is shown in Figure 2.28. A number of comments can be made regarding the characteristics of the amplifier based on comparing these measurements with simulation results – shown in

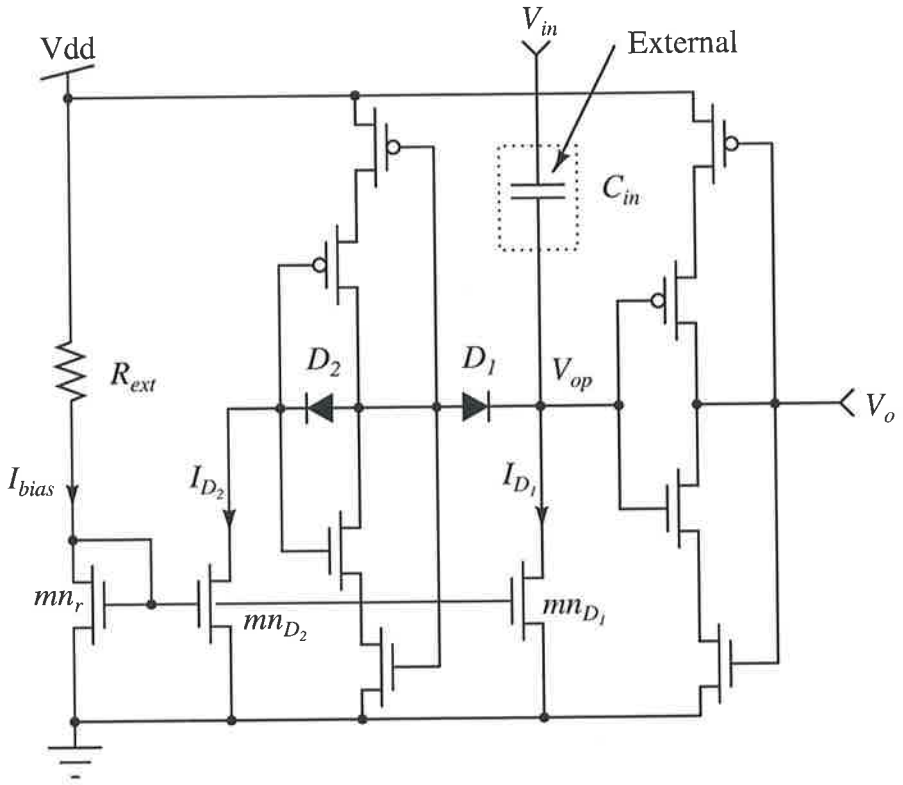

Figure 2.24. The schematic diagram of the fabricated pn junction STC bias and STC amplifier circuits. The micro-photograph of the fabricated amplifier with its bias circuit, without the input coupling capacitor, is shown in Figure 2.26.

Figures 2.29 and 2.30 – at the same supply voltages. Firstly, in contrast to the simulation results, the amplifier characteristics are shifted from the expected $V_{dd}/2$. This can be related to the position of the fabricated circuit on the wafer as demonstrated by the simulation shown in Figure 2.8. Secondly, the amplifier characteristics are not symmetrical across $V_{dd}/2$. This can be related to the ability to model transistor behaviour in the off and subthreshold regions of operation. However, the amplifier characteristics in the region of interest are consistent with the simulation. Thirdly, the simulated gain of the amplifier is 22.5 (or 27 dB) compared to the measured gain of 22 (or 26.8 dB). This shows that the amplifier gain is very robust against process variation. A difference of 0.2 dB is acceptable and is attributed to a measurement error rather than amplifier gain error. Fourthly, the simulated characteristics of the amplifier indicates that the amplifier exhibits a hysteresis outside the amplification range. This can be due to the second point discussed above, which is due the inability of the model to predict the transistor behaviour in the off

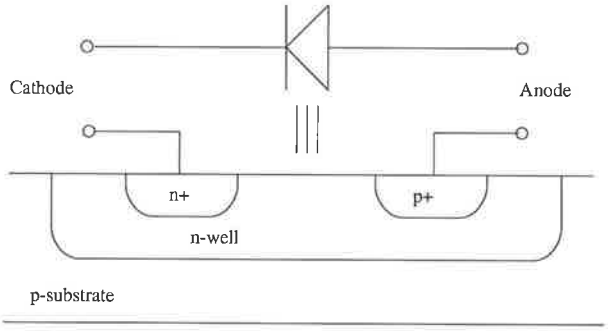

Figure 2.25. A implemented in an n-well process. This cross sectional diagram illustrates the implementation of pn diode using a floating n-well.

and subthreshold region of operations, as in some cases the simulator adds a very high conductance value between some nodes and ground to enable it to converge to a solution.

Also a number of comments can be made regarding the amplifier performance at different supply voltages. Firstly, comparing Figure 2.27 to Figure 2.28, the amplifier gain is slightly higher at higher supply voltages by 0.2 dB. This is due to the fact that mn_2 and mp_2 will have higher gate to source voltage at higher supply voltages, hence their dynamic resistance will be lower, leading to less feedback from the output to the input. Therefore the gain will slightly increase with an increase in the supply voltage. Nevertheless, this level of increase is acceptable and demonstrate the robustness of amplifier to process and supply voltage variation.

The second part of the measurement was to measure the bias circuits, shown in Figure 2.24. All the following DC measurements were taken using the Keithley 236 source measuring unit. The bias circuit was biased using a 19.82 MΩ external resistor, R_{ext} connected between V_{dd} and the diode-connected transistor mn_r, resulting in 115.7 nA and 214.8 nA at 3 and 5 Volt supplies, respectively. Transistor mn_r was designed using 4 parallel transistors with the W/L ratio of each at 21.6/4.8 (in μm), which is equivalent to a 86.4/4.8 (in μm) transistor. Moreover, mn_{D_1} and mn_{D_2} were long transistors with similar W/L ratio of 4.8/84.6 (in μm). Thus, the theoretical current passing through mn_{D_1} and mn_{D_2} at 3 and 5 Volt supplies were 76 pA and 141 pA, respectively. The measured bias voltage at V_{op} at 3 and 5 Volts supply voltages were 1.490 and 2.50 Volt, respectively, indicating that the relative operating point to the supply voltage is always fixed at $V_{dd}/2$.

The current drawn from the power supply by this amplifier circuit could not be measured as the V_{dd} terminal of the circuit under test is connected to the whole chip V_{dd} bus. On the other hand, the above measurements confirmed that the controlled conductance

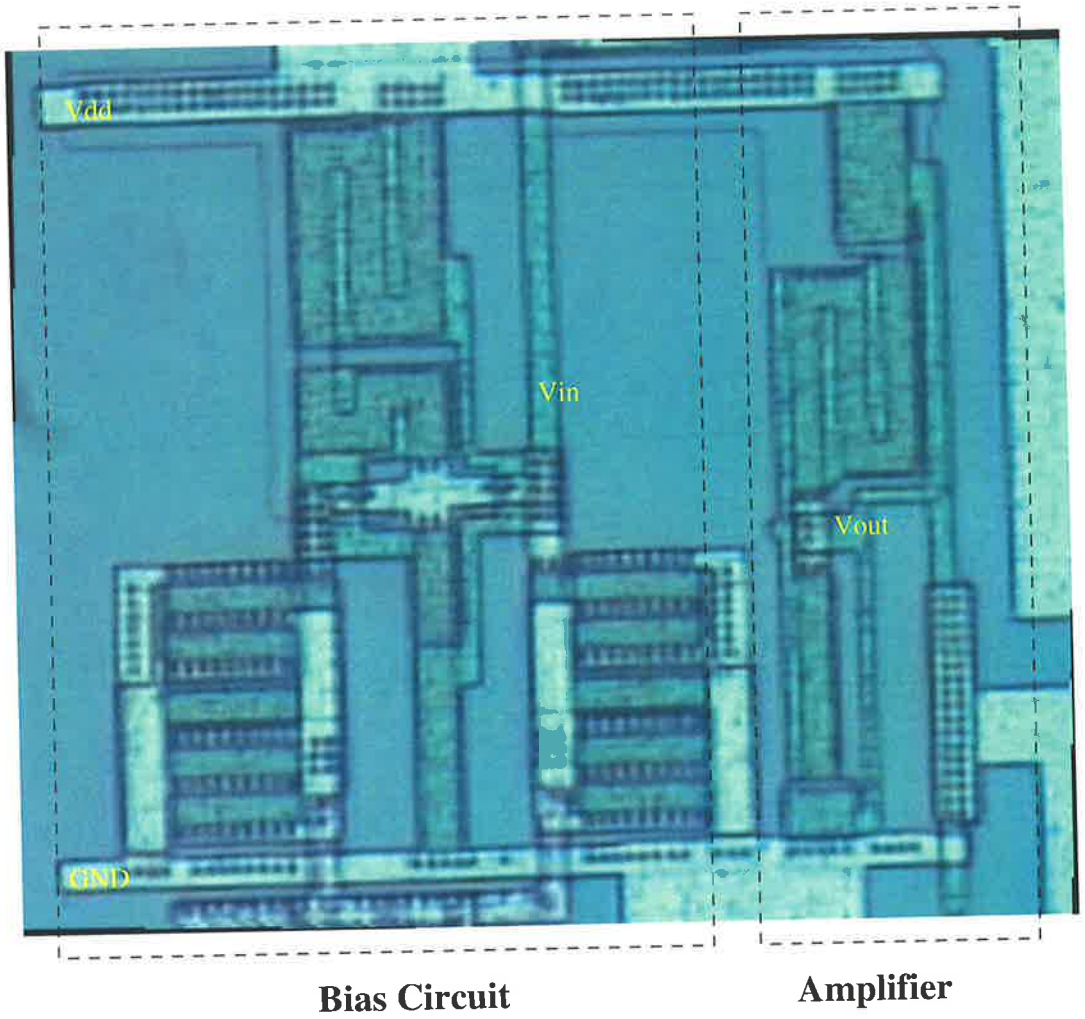

Figure 2.26. A micro-photograph of the fabricated STC amplifier. A micro-photograph of the fabricated STC amplifier circuit shown in Figure 2.4.

technique used in designing controlled gain amplifier is effective and the STC amplifier gain is independent of second order effects.

2.7.2 Measurement of the PTC Amplifier

Although the prime interest is in low power, the PTC amplifier has an interesting feature in which the gain can be accurately adjusted. The following measurements were conducted to verify that the gain can be accurately adjusted. The measurement for this amplifier was conducted using the Motorola MC74HCU04N [*MM74HCU04 Hex Inverter* 1993] logic IC which contains 6 inverters on a single chip. This IC was selected because the input protection circuit does not contain a transistor in series with its input terminal. Nevertheless,

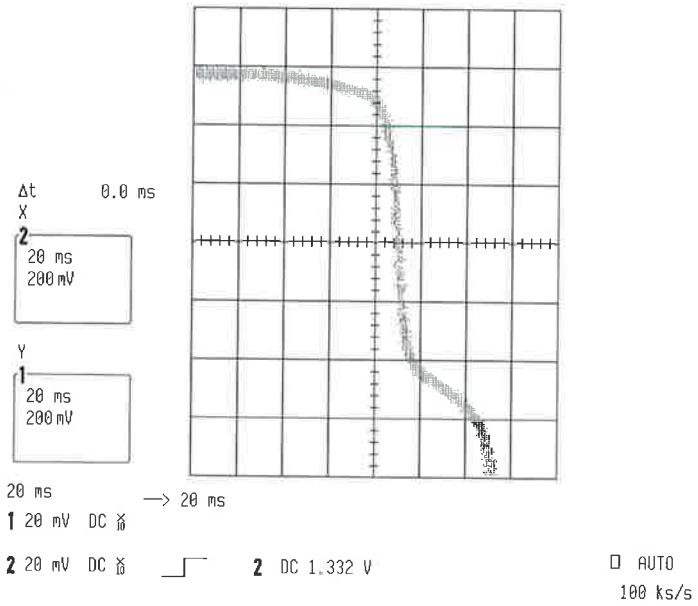

Figure 2.27. Measured input-output characteristics of the STC amplifier at 3 Volt supply. These measurements were obtained from feeding a slow sawtooth input with 3 Volts peak-to-peak signal to the STC amplifier and probing the amplifier output to an oscilloscope (Screen dump from the LeCroy 9360 Oscilloscope).

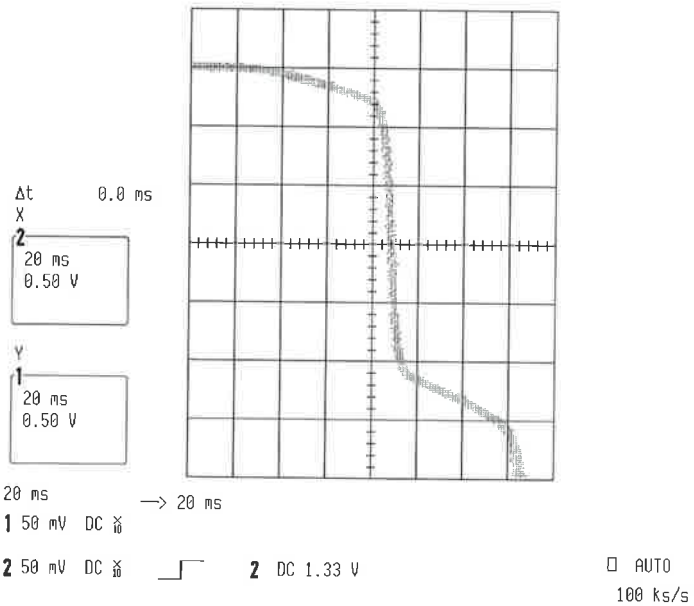

Figure 2.28. Measured input-output characteristics of the STC amplifier at 5 Volt supply. These measurements were obtained from feeding a slow sawtooth input with 5 Volts peak-to-peak signal to the STC amplifier and probing the amplifier output to an oscilloscope (Screen dump from the LeCroy 9360 Oscilloscope).

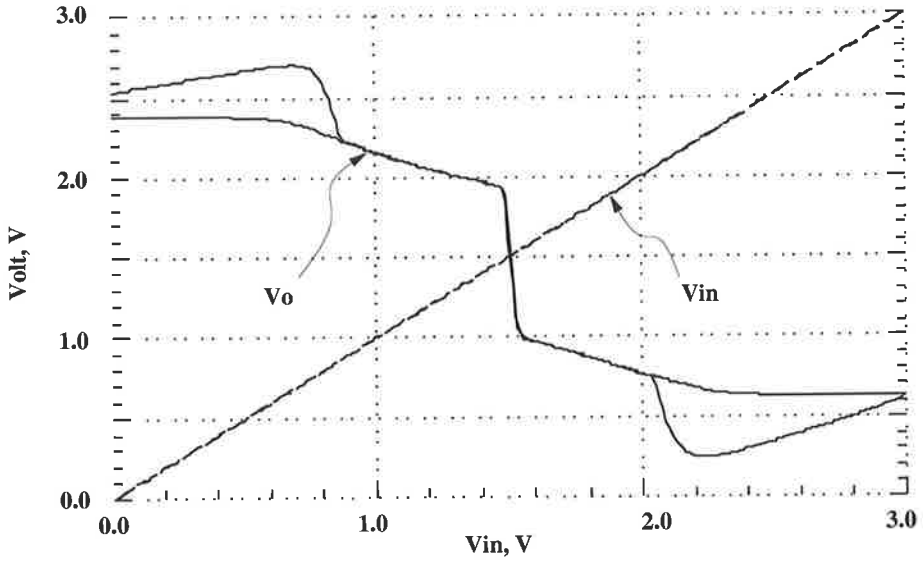

Figure 2.29. The simulation results of the fabricated STC amplifier at 3 Volt supply. These simulations show similar to the measured amplifier characteristics in the amplification region. However, it shows different characteristics below 1 V and about 2 V. This difference is due to the inability of the model parameters used to model the amplifier within 0 to 1 V and 2 to 3 V regions.

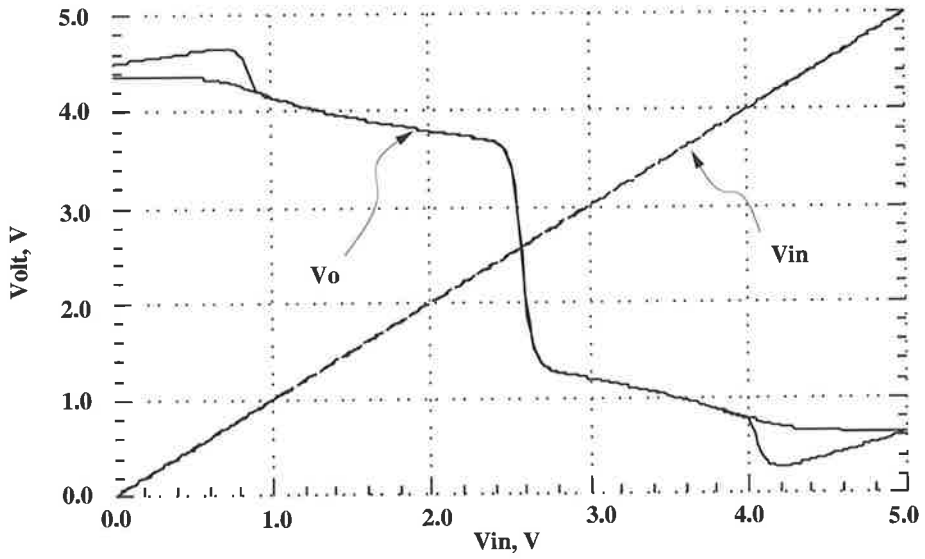

Figure 2.30. Simulation results of the fabricated STC amplifier at 5 Volt supply. These simulations show similar characteristics to the measured amplifier characteristics in the amplification region. However, it shows different characteristics below 1.5 V and about 3.5 V. This difference is also due to the inability of the model parameters used to model the amplifier within 0 to 1.5 V and 3.5 to 5 V regions.

it was found that the inverters in this IC have asymmetrical input-output characteristics around half the supply voltage, which causes the output operating point to deviate from $V_{dd}/2$ when the input is connected to the output.

The first experiment was to design a unity gain amplifier. This was accomplished firstly by connecting the input of one inverter to its output, then using it as a load for another inverter. Using this structure, the β's of the first and the second inverters are set to be equal. The measured input-output characteristics of the amplifier are shown in Figure 2.31. The figure shows that the amplifier has a gain of unity with its DC characteristics shifted from $V_{dd}/2$ for the reasons discussed before.

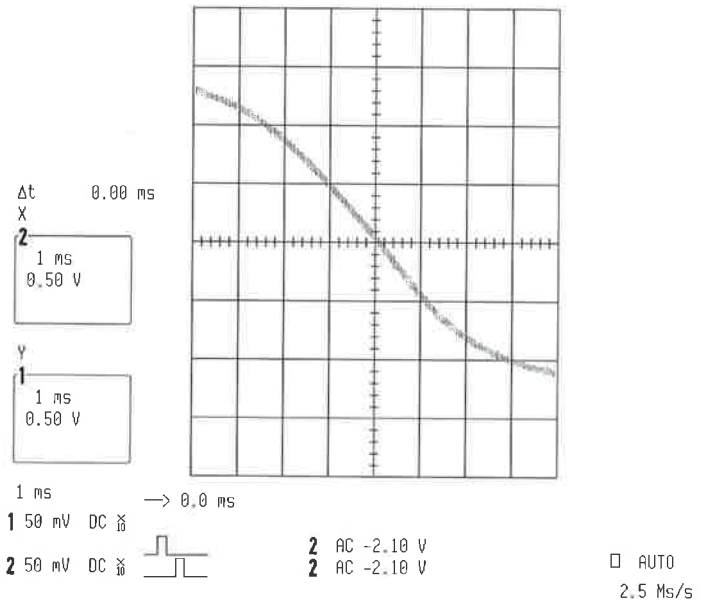

Figure 2.31. Measured characteristics of the unity gain PTC amplifier. These measurements were obtained by applying a sawtooth input signal with a 5 V peak-to-peak amplitude and output is recorded using an oscilloscope (Screen dump from the LeCroy 9360 Oscilloscope).

The second experiment was to use the MC74HCU04N IC logic in the design of a 6 dB gain amplifier. The structure of the amplifier is shown in Figure 2.32. In this structure, the ratio of the effective β's of the input inverters to the output load inverter is 2, resulting in a gain of 2 (6 dB). The measured output characteristic is shown in Figure 2.33 shows that the amplifier gain is 2 (6 dB).

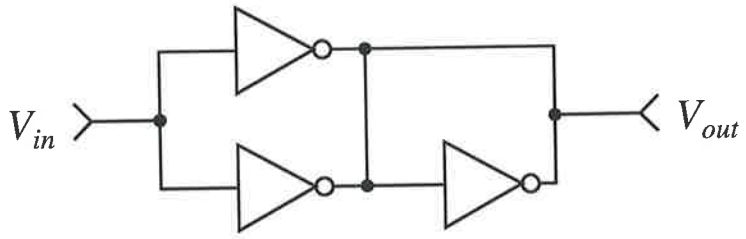

Figure 2.32. Circuit diagram of the implemented PTC amplifier with 6 dB gain. This amplifier was realised using MC74HCU04N IC logic.

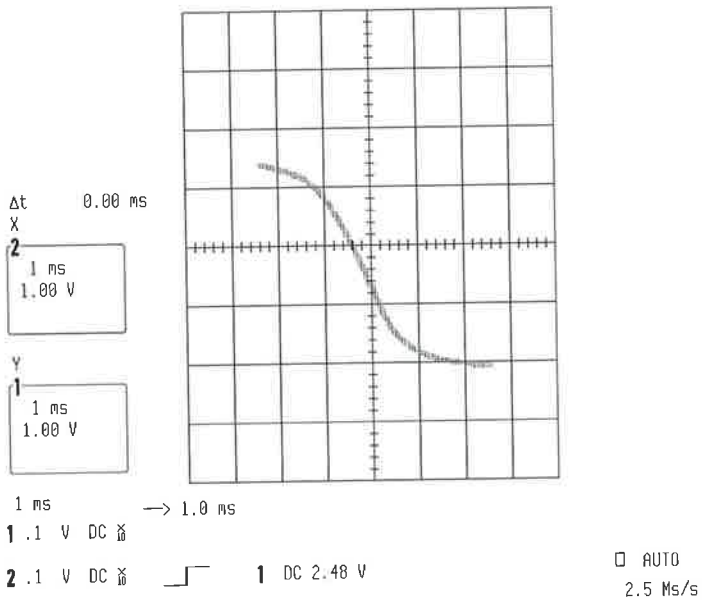

Figure 2.33. Measured input-output characteristics of the 6 dB gain PTC amplifier. These measurements were obtained by applying a sawtooth input signal with a 5 V peak-to-peak amplitude and output is recorded using an oscilloscope (Screen dump from the LeCroy 9360 Oscilloscope).

2.8 Summary

Three variants of new controlled conductance devices were designed, simulated, fabricated and verified. These devices were used successfully in designing controlled gain amplifiers, where the gain is controlled by transistor geometries. The STC technique uses voltage feedback mechanism to control the device conductance. The PTC techniques use the forward conductance of the MOS transistor as a load. The CMC device is a modified form of the PTC device, where the gain is controlled through a series of current mirrors

rather one transistor. When these devices are used in controlled gain amplifier designs the features of these amplifier circuits are

- the gain of all of these circuits is independent of supply voltage;
- the gain is function of the transistor geometries and does not depend on second order effects.
- the area consumption is fairly small compared to other amplifier configuration;
- all of these amplifiers can be configured to provide a unity gain inverting buffer.

A comparison between the three different amplifier circuits is presented in Table 2.4. The gain of these amplifier circuits is independent of the supply voltage. The amplifiers have a wide output dynamic range that extends from rail to rail except in the STC amplifier, the output dynamic range is restricted to $\sim V_{dd} - V_{t_n} - V_{t_p}$. An attractive feature of the PTC amplifier is that once the ratio of β_n/β_p for a process is obtained, the amplifier gain is function of transistor ratios rather than any second order effect that is not controllable by the fabrication foundry. As the structure of these amplifiers closely resembles the normal digital inverter, which has very high driving capability, they provide very high driving capability even with large capacitive load, except for the STC amplifier. This amplifier has a limited driving capability because of its low power nature.

In summary, four new controlled conductance devices are presented and discussed. One of these techniques provides digitally controlled conductance. These devices are used in designing four controlled amplifiers and two biasing circuits for the STC amplifier. The designed amplifiers (a) have infinite input impedance, (b) have fully symmetrical structure, (c) have moderate to wide dynamic range of operation, (d) have power consumption that ranges from low to moderate power levels, (e) can operate at low supply voltage, (f) have gains that can range between low to high gain based on the used configuration, and (h) are area efficient.

The STC controlled conductance technique was verified experimentally through a controlled gain amplifier design with good agreement between simulation and measurements. Also a bias circuit for the STC amplifier was fabricated and tested and proven to work as designed. Also the PTC technique was verified experimentally using IC components and proven to be effective. For AC amplifier applications, new diode based biasing techniques for very low frequency AC coupled amplifiers was presented and discussed. The first uses a *pn* junction, while the second uses a diode-connected MOS transistor. The former was

Table 2.4. A comparison between the three amplifier circuits. This table shows the trade-offs involved when choosing between the different amplifier circuits designed in this chapter in terms of power, silicon area, circuit complexity, bandwidth, power supply rejection, output dynamic range, robustness against process variation, and driving ability.

Comparison Category	STC	PTC	CMC
Power	low	moderate	high
Area	moderate	small	large
Complexity	complex	simple	moderate
Frequency Response	low – medium	low – high	low – medium
Operating Point-Supply dependency	moderate	very low	very low
Out Dynamic Range	small	wide	wide
Gain	mod-high	low-high	low-high
Process Dependency	moderate	independent	independent
Driving Capability	low	high	high

more economical for space and had an important feature in accelerating transient recovery from overload.

Having examined the first technique to reduce power consumption at the circuit level. In the next chapter we will show how design techniques to digitally trim the input offset voltage of differential amplifier at the circuit and the architectural levels used to reduce power consumption and improve mixed signal circuit performance.

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Chapter 3

Digital Trimming of Operational Amplifiers

OPERATIONAL amplifiers are very important basic building blocks in mixed analog-digital circuit design. The performance of these circuits is usually quoted in terms of input-referred offset voltage, power consumption, gain-bandwidth product, etc. The focus of this chapter is a new set of techniques to reduce the input referred offset voltage. In this chapter, two approaches to digitally trim the input referred offset voltage of the first stage gain of an operational amplifier are devised. Both approaches use a set of digitally programmed weighted current mirrors. The attractive features of the new techniques are: wide dynamic range, small silicon area, low power, and the ability to be adapted to provide auto-zero cancellation on the input-referred offset voltage.

3.1 Introduction

Operational amplifiers have always been a very important building block in linear and nonlinear integrated circuit modules. Some essential operational amplifier specifications are input offset voltage V_{os}, input offset current, differential gain, common-mode rejection ratio, etc. Of these specifications, the input offset voltage and differential gain are two parameters of interest when the amplifier is used as a comparator. The input offset current is not applicable as the used technology is CMOS. The offset voltage of the first stage of the amplifier dominates the offset voltage of the operational amplifier. Hence, the gain of the differential amplifier, which is usually the first stage of operational amplifier, is the focus of this chapter.

The gain of the differential amplifier can be increased in a number of ways such as using a small bias current to increase the transconductance of the input transistor or increase the output conductance of the ideally symmetrical input transistors, while the input offset voltage still presents a major problem. Hence a large number of techniques for input offset voltage cancellation have been described in the literature [Vittoz 1985b, Allstot 1982, DeGrauwe *et al.* 1989, Kung *et al.* 1993]. This offset is a result of the wide spread variation in process parameters [Shyu *et al.* 1984, Conroy *et al.* 1988, Pelgrom *et al.* 1989, Forti & Wright 1994, Pavasovic *et al.* 1994, Steyaert *et al.* 1994, Bastos *et al.* 1995, Bastos *et al.* 1997b, Bastos *et al.* 1997a, Kinget & Steyaert 1996], especially when the used fabrication process is not optimised for analog circuit implementation. Furthermore, most of the techniques to either reduce or cancel the input offset voltage in the literature require the use of either external components [Soclof 1985], switched capacitors [Yen & Gray 1982, Senderowicz & Huggins 1982] or floating gate devices [Gao & Snelgrove 1994, Sackinger & Guggenbuhl 1988, Carley 1989]. The first approach is not favoured in some applications as it defeats the integration objectives. The use of switches in the second approach will degrade the V_{os} cancellation due to parasitic capacitance and charge injection [Shieh *et al.* 1989, Chen *et al.* 1995]. Furthermore, some CMOS technologies may not offer such linear capacitors. The third approach requires extra hardware to generate the required programming voltage for the floating gate. Generating an accurate analog signal in the fourth approach can be problematic in a mixed-analog digital environment. Other techniques require increasing the size of the ideally symmetrical transistors, such approaches will minimise the the offset voltage, but will not cancel it.

In applications where the input signal level for the comparator is comparable to the input offset voltage, V_{os}, the effect of V_{os} becomes a serious problem. Therefore, there is a need to develop new techniques to either reduce or cancel it. Hence, there is a need

to estimate the order of magnitude of V_{os} and its statistical characteristics. This is the topic of Section 3.2. Section 3.3 discusses some of the techniques used to reduce V_{os}. Section 3.4 presents and discusses two new techniques. The new techniques are called weighted voltage and weighted-current digital trimming techniques. Section 3.5 presents experimental work of the weighted-voltage techniques. This technique was chosen because it provides trimming without modifying the differential amplifier structure.

3.2 Statistical Data on Input Offset Voltage

3.2.1 Components of V_{os}

The input offset voltage V_{os} can be divided into two components as follows:

1. *Systematic offset voltage:* this voltage is a result of circuit layout and it appears even when all of the matched devices in the circuit are indeed identical. This component can be reduced by using proper design and layout techniques.

2. *Random offset voltage:* this voltage is due to fabrication process variations, which result in threshold voltage mismatch of the supposedly identical devices. This component represents the ultimate limitation on the achievable accuracy.

The techniques devised in this chapter can be used to trim the offset voltage due to random offset variation as will be illustrated in Section 3.4.

3.2.2 Statistical Data on V_{os}

There is a need to have realistic and qualitative data on the input offset voltage V_{os} to devise effective techniques to reduce or cancel it. The targeted fabrication process was Orbit Semiconductor 2 μm, double poly, double metal n-well CMOS process. Since statistical data for this process was not available a literature review on the input offset voltage was done to estimate its order of magnitude.

Forti & Wright [1994] presented measured data for four different CMOS technologies for about 1400 transistors. The measured data are in terms of mismatch dependent on current density, device dimensions and substrate voltage without using any specific transistor model. The data are presented in a graphical form, which shows the current and voltage mismatch versus drawn device dimensions for both nMOS and pMOS devices for the four processes listed in Table 3.1. The results for nMOS transistors are shown in Figure 3.1.

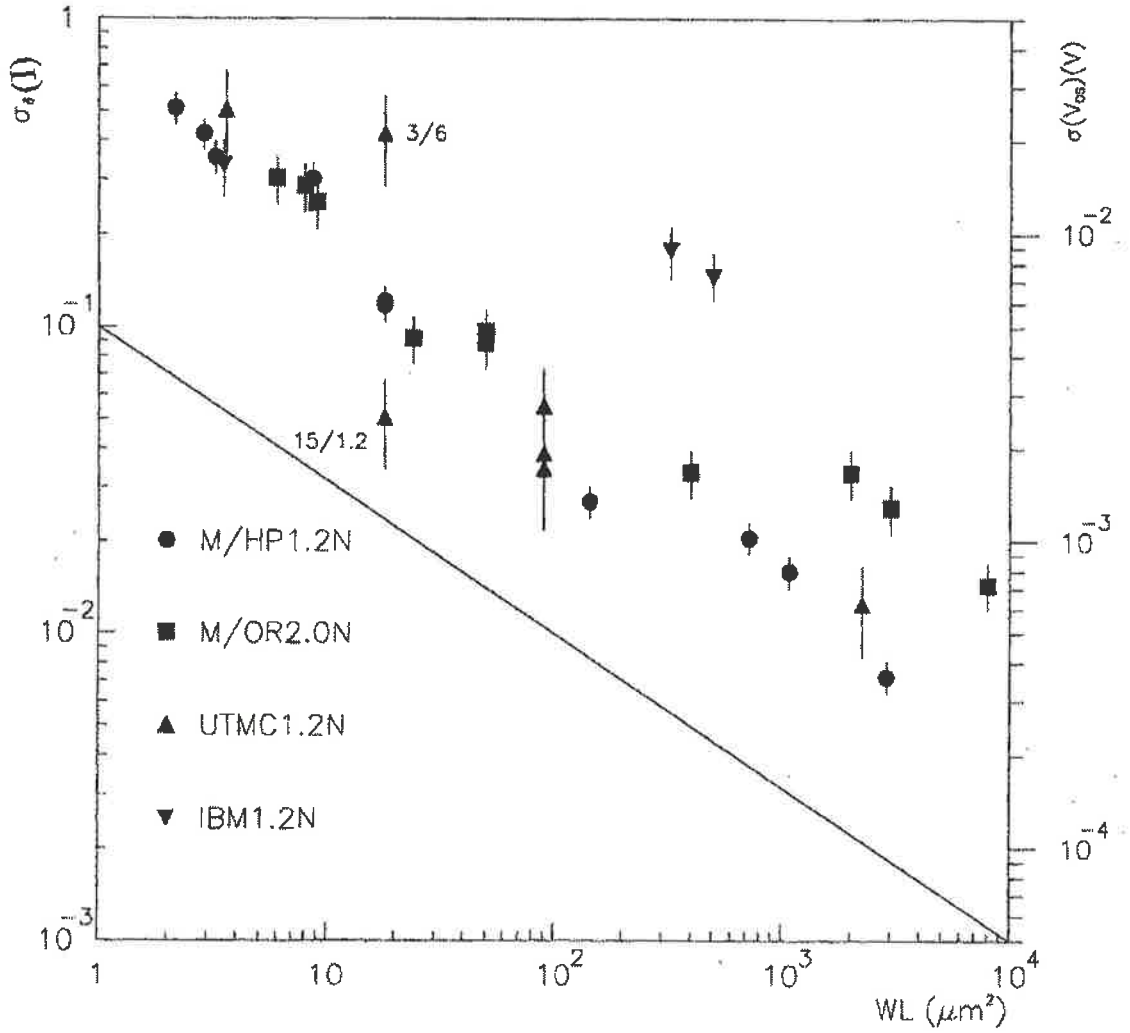

Figure 3.1. Current and voltage mismatch versus drawn device area. This graph shows the current and voltage mismatch versus drawn device area for all processes for nMOS transistors at drain current density $I_\square = 1$ nA/□. The straight line represents the slope of the expected $1/\sqrt{WL}$ dependence. The left hand side y-scale of the figure represents the standard current deviation, $\sigma_\delta(I)$ from the designed value in nA. The right hand side y-scale represents the standard deviation of the input offset voltage, $\sigma(V_{os})$, in Volts, after [Forti & Wright 1994].

Table 3.1. Characteristics of some standard low cost CMOS processes. The table shows the oxide thickness and well type for a number of CMOS technologies that are used to study the statistical characteristics of offset voltage and current mismatch in current mirrors by Forti & Wright [1994].

Process	Feature Size (μm)	Well Type	Gate Oxide (nm)
MOSIS/HP	1.2	N	20
MOSIS/Orbit	2.0	P	40
UTMC	1.2	P	20
IBM	1.2	N	20

As expected from the models reported in [Lakshmikumar *et al.* 1986, Conroy *et al.* 1988, Shyu *et al.* 1984, Yu & Geiger 1994], the dependence of both current mismatch and input offset voltage is proportional to $1/\sqrt{WL}$. However, in case of pMOS transistors (the graph is not shown) they do not quite follow the $1/\sqrt{WL}$ relation. This might be due to higher mobility variations or poorer gate oxide capacitance matching [Forti & Wright 1994]. Moreover, an interesting relationship between the oxide thickness and both the current mismatch and the input offset voltage can be observed from Figure 3.1. The thicker the oxide the smaller the input offset obtained. This conclusion is consistent with statistical analysis presented in Appendix C.

The conclusions of Forti & Wright [1994], Lakshmikumar *et al.* [1986], Conroy *et al.* [1988], Shyu *et al.* [1984] and Yu & Geiger [1994] that the input offset voltage in standard CMOS technologies is in the range of ± 15 mV depending on the transistors sizes of the ideally symmetrical transistors. For example, to obtain an offset voltage in range of 1 mV, the size of the ideally symmetrical transistors has to be in the range of 1000 μm^2 which is very large.

3.3 Input Offset Voltage Reduction and Cancellation

The following subsections discuss some of the common techniques used to reduce and cancel the input offset voltage V_{os}.

Table 3.2. Rules for Optimum Matching. These rules can be used to ensure optimum matching between adjacent components for CMOS technology [Vittoz 1985a].

No.	Rule
1.	Same structure
2.	Same temperature
3.	Same shape and size
4.	Minimum distance
5.	Common-centroid geometries
5.	Same orientation
6.	Same surroundings
7.	Non minimum size

3.3.1 Device Mismatch Reduction

According to an analytical study of V_{os} based on a statistical model in [Michael *et al.* 1994], threshold voltage mismatch in the ideally symmetrical input transistors has a dominant effect. Therefore a special effort should be devoted toward reducing the threshold voltage mismatch of the ideally symmetrical transistors. This is done by increasing the sizes of the ideally symmetrical transistors [Watanabe *et al.* 1994, Mohamedi *et al.* 1992] and following the rules listed in Table 3.2 [Vittoz 1985a] for optimum matching to achieve the best results. This approach is costly in terms of silicon area because of the dependence of V_{os} on $1/\sqrt{\text{transistor area}}$.

3.3.2 Off-Chip Offset Voltage Compensation

The off-chip offset voltage compensation technique is widely used in commercial op-amps [Soclof 1985] due to its simplicity and effectiveness. This method uses a potentiometer either at one of the inputs of the op-amp terminals as shown in Figure 3.2, or a potentiometer between the offset null terminals of the op-amp and a reference voltage as shown in Figure 3.3. This technique is used in precision op-amps to achieve an offset voltage of less than 100 μV.

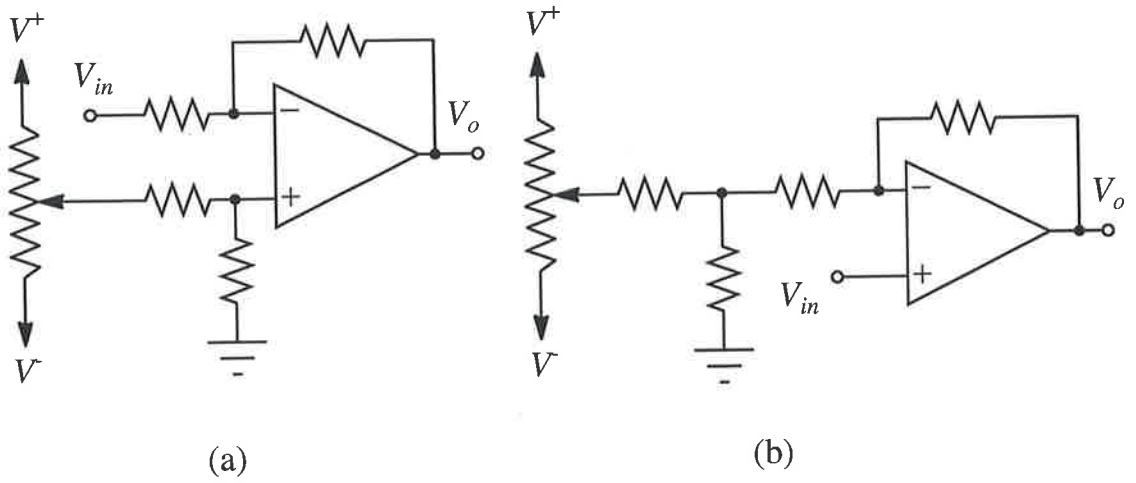

Figure 3.2. Two common techniques for offset voltage compensation. These conceptual drawing relies on using a variable resistor that is attached to one of the operational amplifier inputs to cancel the input offset voltage.

3.3.3 Auto-zero Cancellation Techniques

Another technique called auto-zero cancellation [Yen & Gray 1982, Senderowicz & Huggins 1982] can be used to reduce the offset voltage. This technique relies on providing hardware either on chip, off chip or both to automatically reduce the offset voltage. Most of the methods used in auto-zero cancellation rely on storing V_{os} at some of the circuit internal nodes and then cancelling V_{os} by various methods, as will be discussed later in this subsection. These methods have limited performance: Firstly due to the use of capacitors and analog switches to achieve the cancellation. These switches degrade the offset voltage cancellation due parasitic capacitance and charge injection [Shieh *et al.* 1989, Chen *et al.* 1995]. Secondly, most of these methods have a 50% duty cycle or less, making them unsuitable for continuous-time applications. Four common methods that are used in auto-zero cancellation of V_{os} are discussed below.

- The first method relies on storing V_{os} at a capacitor at the input of the op-amp, as shown in Figure 3.4.a. Assuming ideal conditions, the stored voltage across the capacitor is equal to V_{os}. However, due to charge injection of switch S1, the stored value will significantly change, resulting in a degraded offset cancellation [DeGrauwe *et al.* 1989]. The corresponding switches waveforms for these circuits are shown in Figure 3.4.d.

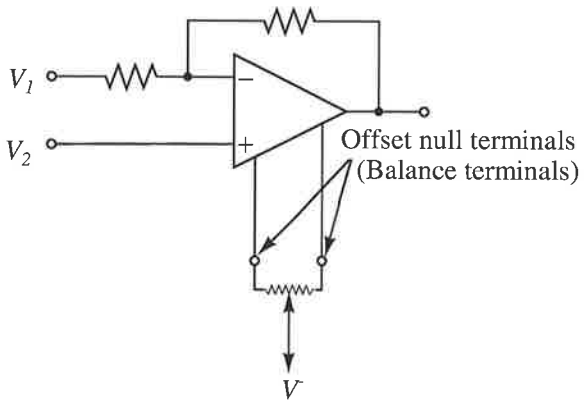

Figure 3.3. Offset voltage compensation using null terminals. In this technique a null potentiometer is used cancel the offset voltage through the current mirror structure of the differential stage in the operational amplifier.

- The second method uses two op-amps. In this method, V_{os} is amplified then stored at the output of the first stage op-amp, as shown in Figure 3.4.b. Even though, the charge injection of the switches S1 and S2 will not significantly degrade the offset cancellation, this method needs two op-amps which gives rise to potential stability problems [DeGrauwe *et al.* 1989, Poujois & Borel 1978].

- The basic idea of the third method is to store V_{os} at a low sensitivity auxiliary input and employ a feedback mechanism to reduce it, in addition to a buffer circuit for phase compensation acceleration, as shown in Figure 3.4.c. Using this technique it is possible to obtain a very small V_{os}, with a standard deviation in the order of 370 μV, however this technique has a 25% duty cycle and consumes large silicon area [DeGrauwe *et al.* 1989].

- The fourth method is a digitally controlled auto-zero cancellation [Yu & Geiger 1994, Kung *et al.* 1993, Opris & Kovacs 1996]. This method relies on using an analog programmable current mirror as a load for the differential amplifier, as shown in Figure 3.5. Despite the fact that the accuracy of this method is function of the digital-to-analog converter (DAC) and the comparator offset voltage, which are part of the offset tuning scheme Figure 3.6, it is claimed that it is possible to reduce an offset voltage in the range of $\pm$15 mV to a very small value in the range of 400-500 μV using a 7 bit digital to analog converters (DAC).

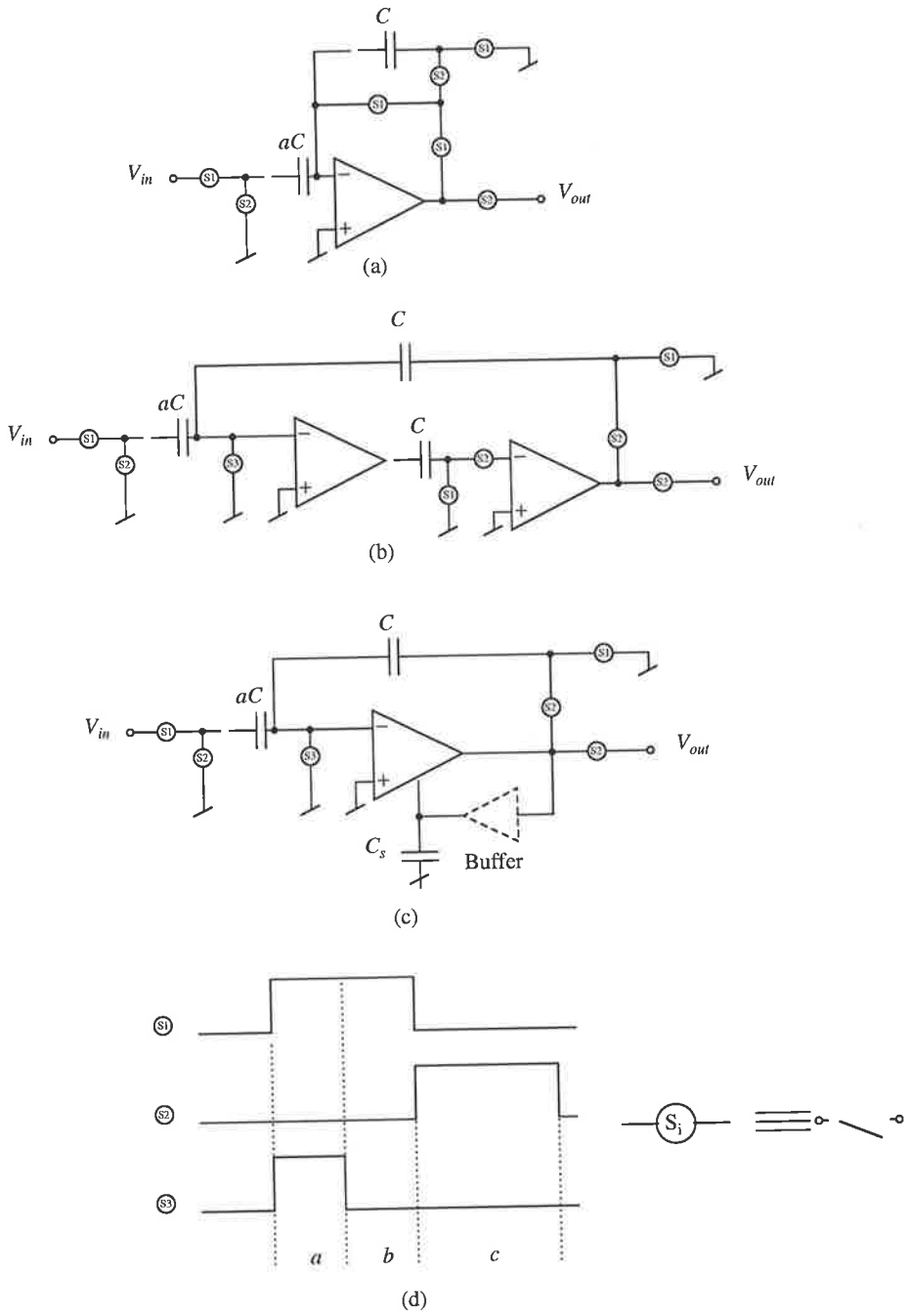

Figure 3.4. Auto-zero cancellation techniques. Three techniques for auto-zero cancellation are shown. In (a) the offset voltage is stored at the input then subtracted from input signal. In (b) offset voltage is amplified and stored after a first stage gain then subtracted from the amplified input signal. In (c) offset voltage is stored at a low sensitivity auxiliary input then subtracted in the operational amplifier from the input signal. Diagram (d) shows the the corresponding switch waveforms for each of the techniques.

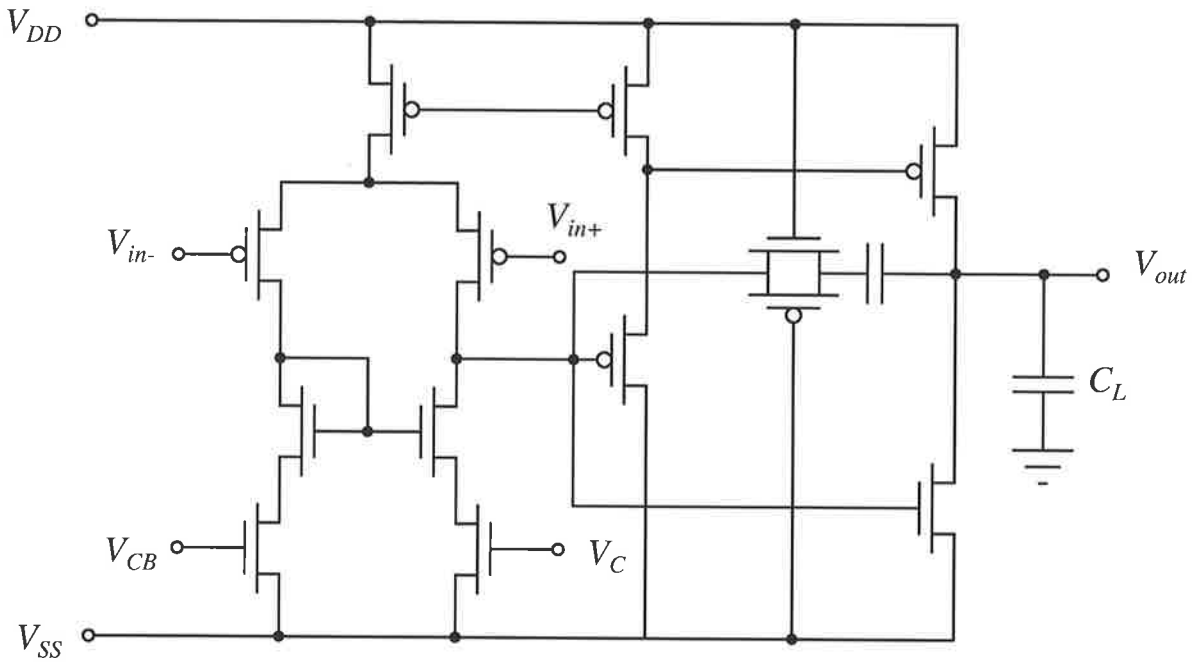

Figure 3.5. Offset adjustable two stage CMOS op-amp using a programmable current mirror. In this technique the offset is adjusted by applying a fixed voltage at V_{CB} and adjusting the voltage at V_C to obtain zero offset voltage at the differential amplifier output.

3.4 New Digital Trimming Techniques

Trimming techniques are widely used to enhance some aspects of analog circuit performance [Gray & Meyer 1992, Al-Sarawi & Cole 1995]. In this section two new approaches, we refer to as weighted-voltage and weighted-current techniques are proposed to achieve digitally trimmed offset voltage. Both techniques have a set of digitally programmable current mirrors as their controlling engine. The attractive features of the new techniques are:

- The trimming is performed digitally.
- They have a wide dynamic range.
- They do not consume large silicon area.
- They are applicable in both saturation and subthreshold regions of operation.
- They can be adapted, when a zero reference is available, to provide auto-zero cancellation of the input offset voltage similar to the one discussed in [Yu & Geiger 1994], without the need for a digital-to-analog converter (DAC).

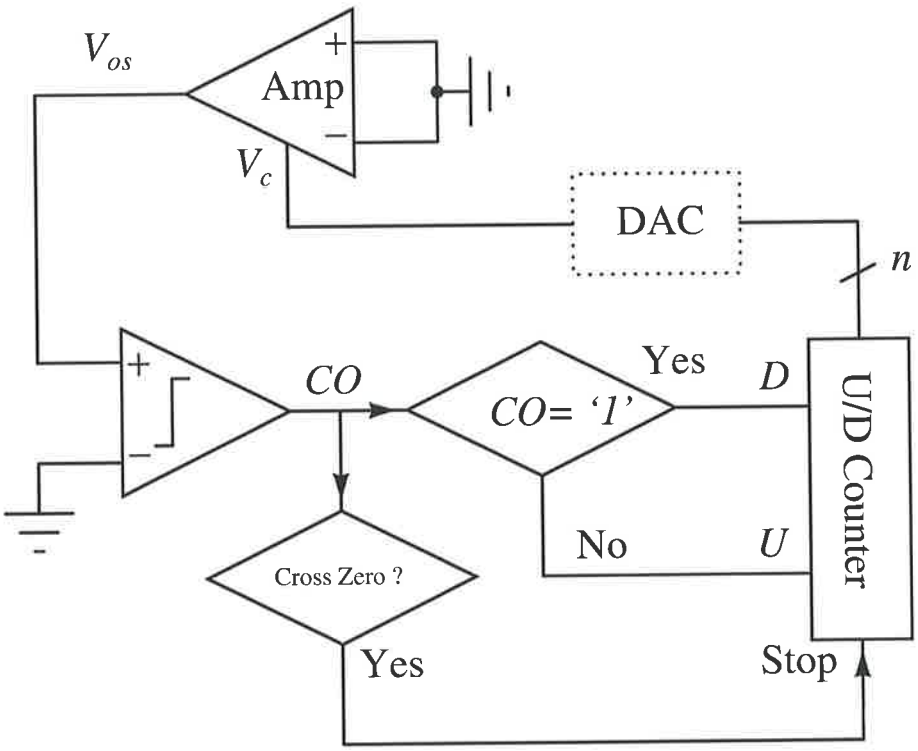

Figure 3.6. Concept of the offset tuning scheme. This is applied to the operational amplifier in Figure 3.5. CO is the output of the comparator, D is the down terminal of the counter to force the counter to count downward, U is the same as D except it forces the counter to count upwards, and DAC represents the digital-to-analog converter.

In the following analysis, it is assumed that the source and the backgate of the corresponding n and p MOS transistors are connected together, unless mentioned otherwise. In addition, a binary weighted scheme is used. Although other weighting schemes can be used.

3.4.1 Weighted-Voltage Trimming Technique

The name of this technique is derived from the way the trimming is achieved which is through biasing a *pn* junction diode (or a diode-connected MOS transistor) using digitally programmable binary weighted current mirrors. These currents are then used to produce a voltage drop across the diode, V_d. The relation between the diode voltage, the currents and the controlling switch states is given as

$$V_d = \eta U_t \ln\left(\frac{\sum_{i=0}^{N} B_i I_0/2^i}{I_s}\right) \tag{3.1}$$

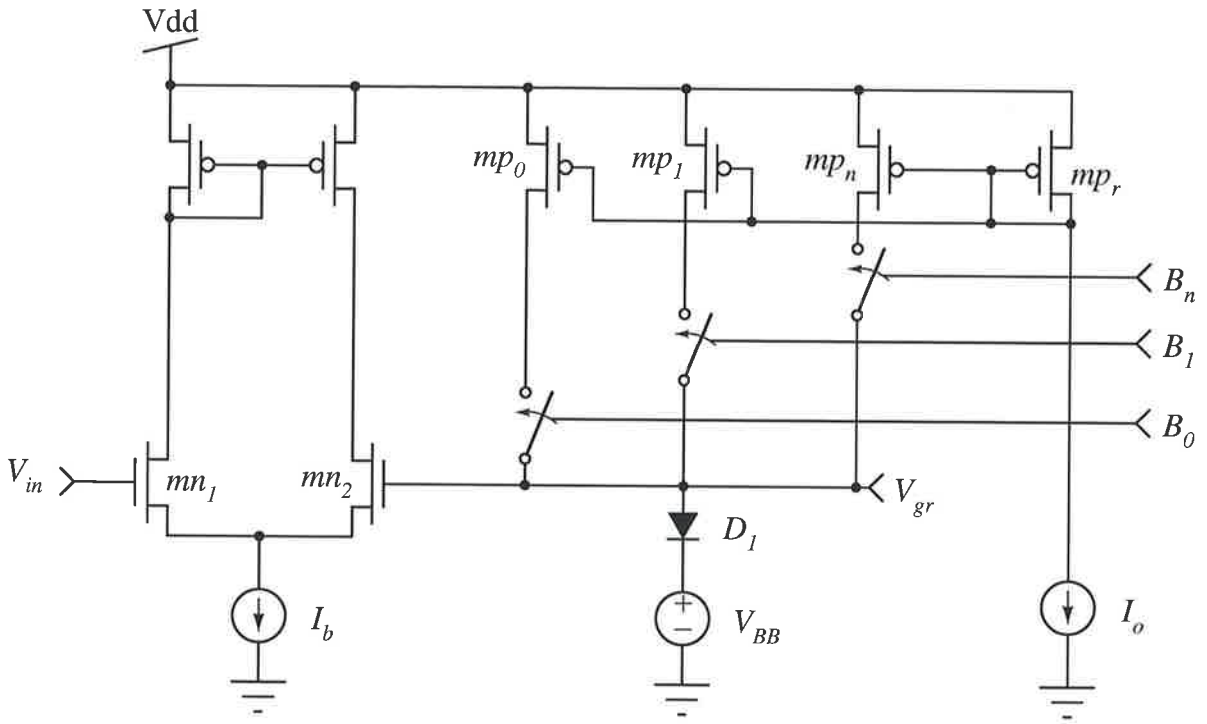

Figure 3.7. A single ended voltage comparator trimmed using a weighted-voltage trimming technique. The trimming for this circuit can be performed by digitally controlling the current through D_1, that current is translated into a voltage drop across D_1.

where

η	is the emission factor of the diode;
U_t	is the thermal voltage;
$N+1$	is the number of bits;
B_i	is the state of the ith switch, [0 for OFF or 1 for ON];
I_0	is the reference current value;
I_s	is the reverse saturation current.

The first method of using the weighted voltage technique, in offset voltage cancellation, is shown in Figure 3.7. The input gate of one of the input transistors of the differential amplifier, mn_2, is tied to a voltage source which has two DC components. The first component is a fixed bias voltage called V_{BB}, and is needed to provide the DC operating point for the differential amplifier, while the second component is the voltage drop across the diode. The resultant gate voltage at mn_2, V_{gr}, is given as

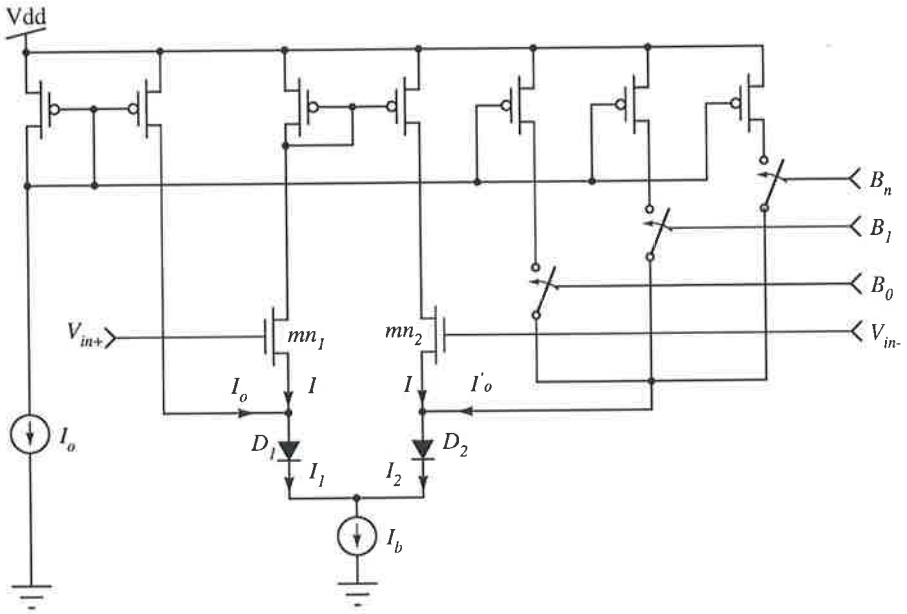

Figure 3.8. A digitally trimmed differential amplifier using the weighted-voltage technique. In this technique the source voltages of mn_1 and mn_2 are controlled by the digitally programmable current mirror. The summation of I'_o and I_o will be translated into a voltage drop across D_2. Hence, the difference between the source voltages of mn_1 and mn_2 are adjusted to cancel the input offset voltage.

$$V_{gr} = V_{BB} + \eta U_t \ln\left(\frac{\sum_{j=0}^{N} B_j I_0 / 2^j}{I_s}\right). \tag{3.2}$$

From Equation 3.2, the offset trimming depends on the absolute values of I_o, I_s and V_{BB}. The dependence on I_s and V_{BB} can be cancelled by using another diode biased by I_0 and placed in the other leg of the differential amplifier. To avoid presenting a low input impedance to the amplifier input, both diodes are moved to the source legs of the amplifier input transistors as shown in Figure 3.8. Such shift reduces the gain of the differential amplifier. The reduction, when subthreshold operation is considered, can be as much as half the original gain before the introduction of the diodes.

Figure 3.8 represents a second method to reduce the offset voltage using the weighted voltage technique. In this method, an *introduced offset voltage* V_{ios}, which is defined as the voltage difference between the sources of the input transistors of the differential amplifier, is calculated as in Equation 3.3. The full derivation of this equation is shown in Appendix E.

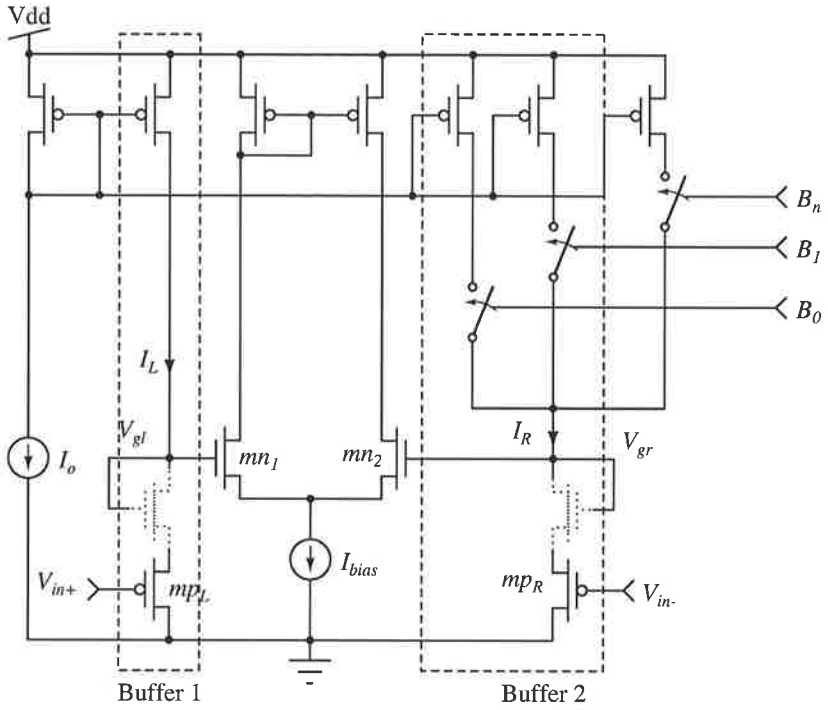

Figure 3.9. A digitally trimmed differential amplifier with extended common mode range using a weighted voltage technique. The trimming for this circuit is done through the input buffer circuits boxed by dashed line. These buffer perform two functions: first they introduce a level shift. This shift is function of the input pMOS transistor threshold and the bias current controlled by I_o. The second function to adjust the amount of voltage level shifting using the programmable current mirror. The resultant voltage at the output of these buffers can be used to cancel the input offset voltage. Furthermore, the two dashed diode-connected nMOS transistors can be introduced to the circuit if further level shifting is needed.

$$\begin{aligned} V_{ios} &= V_{d_1} - V_{d_2} \\ &= \eta U_t \ln \left[\frac{\frac{I_b}{I_o} + (1 - \sum_{i=0}^{N} \frac{B_i}{2^i})}{\frac{I_b}{I_o} - (1 - \sum_{i=0}^{N} \frac{B_i}{2^i})} \right] \end{aligned} \tag{3.3}$$

where

I_o is the reference current appearing in Figure 3.8;

I_b is the differential amplifier bias current.

Equation 3.3 shows the dependence of the introduced offset voltage V_{ios} on the ratio of I_b to I_o, and upon the switches state. In addition, the equation shows that V_{ios} is independent of I_s.

A third method of employing the weighted voltage technique to reduce the offset voltage is shown in Figure 3.9. The cancellation is performed through a buffering circuit at one of the input terminals of the differential amplifier. The buffer circuit uses at one terminal a common drain pMOS transistor biased by a digitally programmable current source, while buffering at the second input terminal uses a common drain pMOS transistor biased with a fixed bias current. An additional level shifting of the input signal can be achieved through using a diode-connected MOS transistor as shown by the dotted transistors in Figure 3.9.

The quiescent voltage at the gates of the inner differential pair is the sum of voltage drop across the diode-connected nMOS transistor and the drain to source voltage of the pMOS transistor. This voltage is sufficient for the operation of the differential amplifier with a single ended power supply. Additionally, the common drain pMOS transistors can operate at a quiescent gate voltage of zero. These two effects together allow the common mode input voltage of the circuit to extend to a negative supply voltage. The introduced input offset voltage V_{ios} to the differential amplifier structure is given by

$$\begin{aligned} V_{ios} &= V_{g_l} - V_{g_r} \\ &= \sqrt{\frac{2I_L}{\beta_L}}\left(1 - \sqrt{\frac{I_R\beta_L}{I_L\beta_R}}\right), \end{aligned} \tag{3.4}$$

where I_L and I_R are the current passing through mp_L and mp_R in Figure 3.9, respectively. In I_R is generated using a binary weighted digitally programmable current mirror that is described as

$$\begin{aligned} S_R &= \sum_{j=0}^{N} B_j S_L/2^j \\ \frac{I_R}{I_L} &= \frac{S_R}{S_L} = \sum_{j=0}^{N} B_j/2^j, \end{aligned} \tag{3.5}$$

then V_{ios} can be written as

$$V_{ios} = \sqrt{\frac{2I_L}{\beta_L}}\left(1 - \sqrt{\sum_{j=0}^{N} B_j/2^j}\right). \tag{3.6}$$

If mp_R is replaced by a group of binary weighted transistors (mp_{R_0} to mp_{R_n}) and biased by the same value of current as I_L as shown in Figure 3.10, the introduced input offset voltage relation with the weighted transistor sizes is similar to Equation 3.6.

3.4.2 Weighted-Current Trimming Technique

The name of this technique is also derived from the way the trimming is achieved, which is through the load transistors of the differential amplifier. This technique relies on compensating for current mismatch in the input transistors of the differential amplifier. The compensation is achieved by replacing the standard current mirror structure with a digitally programmable current mirror, as shown in Figure 3.11.

In the face of a threshold voltage variation, there is a need to have zero amplifier output current, so that no output current flows to the output terminal of the amplifier. Such output current, if present, could develop an output voltage across the combination of the output impedance of the amplifier and input impedance of any following load. Having a zero output current at the amplifier output can be achieved by firstly, calculating the difference in drain currents due to the threshold voltage variation and secondly, adjusting the amplifier current mirror structure so that output current of the amplifier is zero.

An equivalent threshold voltage mismatch ΔV for a current mismatch in the input transistors of the differential amplifier can be calculated in both the saturation and subthreshold regions by using the simple transistor [Haskard & May 1987] and Vittoz models [Vittoz 1985a], respectively. The result of these calculations are given in Equation 3.7.

$$\Delta V = \begin{cases} \sqrt{\frac{2I_L}{\beta}}\left(1 - \sqrt{\frac{I_R}{I_L}}\right) & \text{; saturation region} \\ -nU_t \ln\left(\frac{I_R}{I_L}\right) & \text{; subthreshold region} \end{cases} \tag{3.7}$$

where

I_L,I_R	are the currents through the mn_1 and mn_2 transistors, respectively;
β	is the intrinsic transconductance parameter, A/V^2;
n	is the subthreshold slope factor;
U_t	is the thermal voltage.

The relation between I_R and I_L in the digitally programmable current mirror is given as

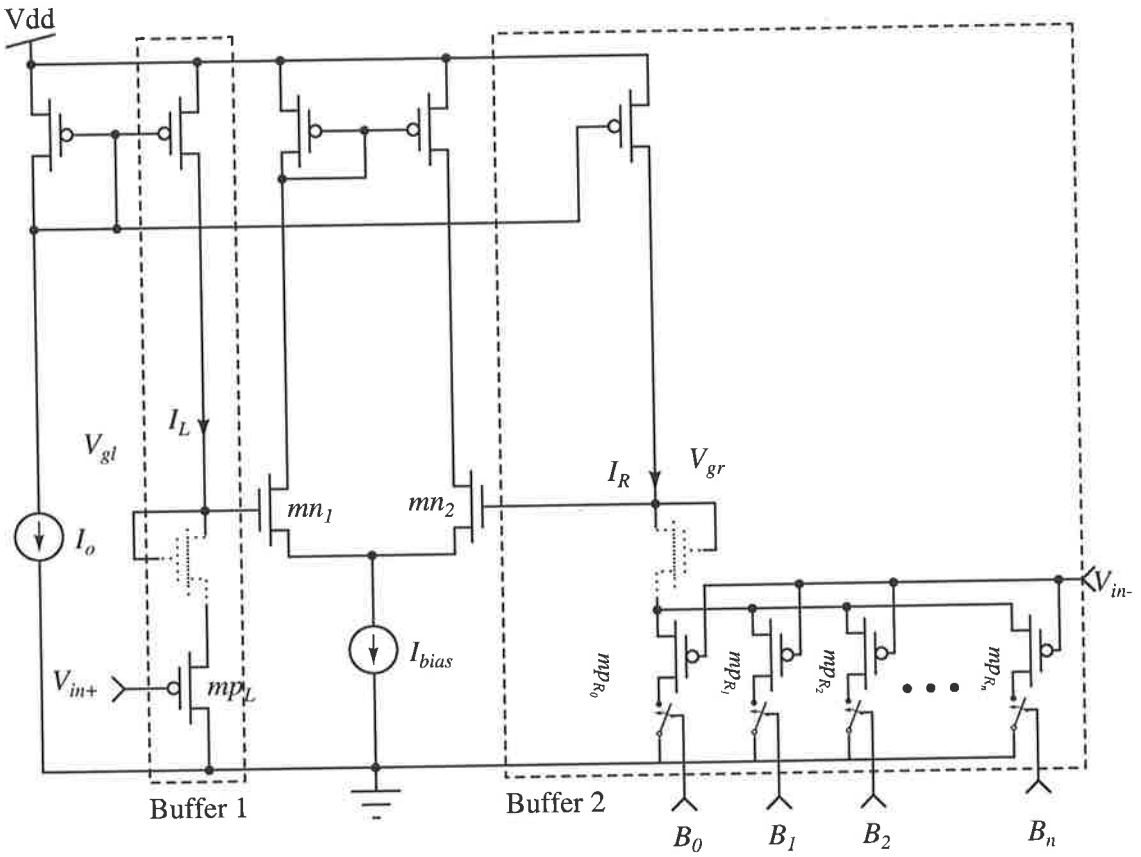

Figure 3.10. A digitally trimmed differential amplifier with extended common mode range using a weighted voltage technique at the input transistors. The trimming for this circuit is done through the input buffer circuits boxed by dashed line. These buffer perform two functions: first they introduce a level shift. This shift is function of the input pMOS transistor threshold and the bias current controlled by I_o. The second function to adjust the amount of voltage level shifting using the programmable current mirror. The resultant voltage at the output of these buffers can be used to cancel the input offset voltage. Furthermore, the two dashed diode-connected nMOS transistors can be introduced to the circuit if further level shifting is needed. In contrast to Figure 3.9, the bias current value for both buffer circuit is same and the weighting is done through resizing the input buffer transistors.

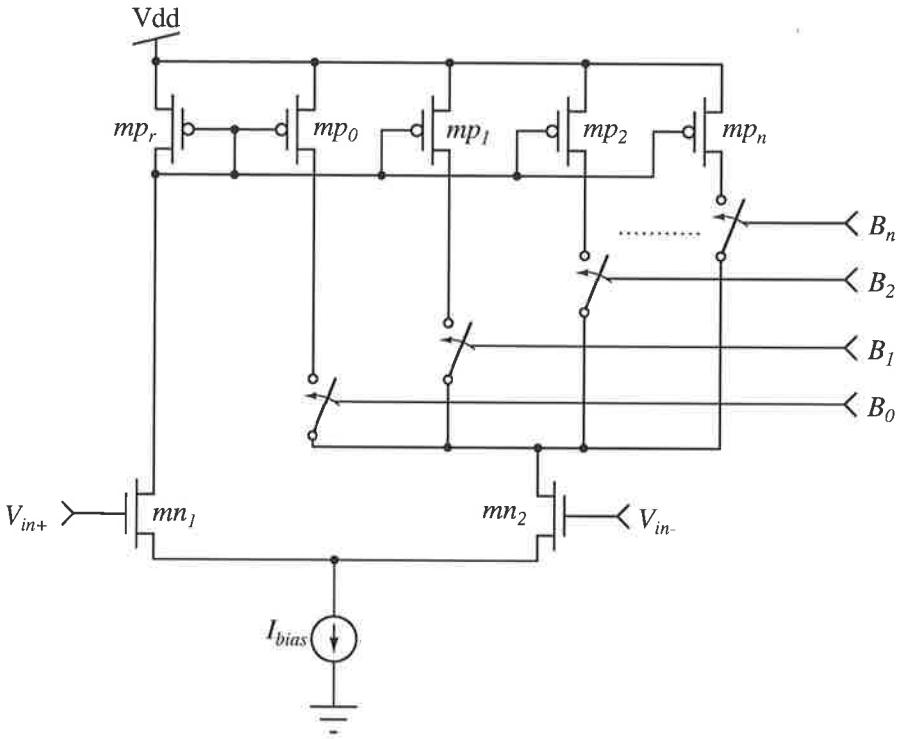

Figure 3.11. A digitally trimmed differential amplifier using a weighted-current technique. In this technique the mirror load current for transistor mn_2 is digitally controlled using switches B_0 to B_n.

$$\begin{aligned} S_R &= \sum_{j=0}^{N} B_j S_L / 2^j \\ \frac{I_R}{I_L} &= \frac{S_R}{S_L} = \sum_{j=0}^{N} B_j / 2^j, \end{aligned} \tag{3.8}$$

where

S_R	is the width to length ratio of the mp_0 to mp_n load transistors;
S_L	is the width to length ratio of the mp_r transistor;
B_j	is the state of the jth switch;
$N+1$	is the number of programming bits.

Substituting Equation 3.8 into 3.7, the equivalent threshold voltage mismatch ΔV can be written as

Table 3.3. Introduced offset voltage as function of the current mismatch. This table shows the minimum and maximum mismatch that can be cancelled when the current mirror structure either working in the saturation or subthreshold regions of operation. These measured simulation results show that the minimum mismatch can be cancelled is in the sub-millivolts, while the maximum mismatch current that can be cancelled depends on whether the current mismatch is in the diode-connected transistor or in the other transistor. The measured mismatch in both regions of operations is different. The difference is traceable to definition of ΔV given in Equation 3.9.

ΔV	Minimum Current Mismatch		Maximum Current Mismatch	
	+1.15%	-1.15%	+98.4%	-98.4%
Saturation	-719 μV	725 μV	-37.8 mV	80.9 mV
Subthreshold	-670 μV	660 μV	-177 mV	29.173 mV

$$\Delta V = \begin{cases} \sqrt{\frac{2I_L}{\beta}}\left(1 - \sqrt{\sum_{j=0}^{N} B_j/2^j}\right) & ; \text{saturation region} \\ -nU_t \ln\left(\sum_{j=0}^{N} B_j/2^j\right) & ; \text{subthreshold region.} \end{cases} \tag{3.9}$$

From Equation 3.9, the input offset voltage can be cancelled by compensating for the current mismatch of the input transistors of the differential amplifier. An interesting observation about ΔV, when subthreshold operation is considered, is that the trimming is independent of the bias current.

By using a 7-bit digitally programmable current source, it is possible to compensate for a current mismatch (I_R/I_L) in the input transistors of the differential amplifier from $\pm 1.15\%$ to $\pm 98.4\%$. The corresponding cancellations in the input offset voltages are given in Table 3.3. The values of I_L, β and S used for the saturation region calculation are 500 nA, 19.5 μA/V^2 and 6, respectively, while the value of n and U_t used for the subthreshold region are 1.65 and 25.8 mV, respectively.

From Table 3.3, this technique has a wide dynamic range in both regions of operation, and they can compensate for an offset voltage down to less than 1 mV. These calculations show that trimming using transistors operating in the subthreshold region of operation give better results than performing trimming using transistors operating in the strong region of operation. However, mismatch in the subthreshold region of operation is larger than the mismatch in the strong region of operation. The later comment should be taking into account by the designer to decide which region of operation to use for the trimming.

3.5 Experimental Work

From all of the above discussed trimming techniques, the weight-voltage technique discussed in Section 3.4.1 and shown in Figure 3.9 was selected for fabrication. Test structures were fabricated in a 2 μm double poly, double metal CMOS process at Orbit Semiconductor through MOSIS. The trimming technique shown in Figure 3.12 was selected for fabrication for three reasons. Firstly, it provides trimming without affecting the differential amplifier structure, so no restriction has to be imposed on the differential amplifier structure. Secondly, the trimming is performed without restricting the input terminals of the amplifier. Thirdly, the trimmer can be tested separately from the amplifier structure. A micro-photograph of the fabricated trimmer arms is shown in Figure 3.13. This micro-photograph corresponds to the schematic diagram shown in Figure 3.12. To improve the matching between the two arms of the trimmer a dummy transistor, mn_5, was connected between the source of mp_5 and ground with its gate connected to V_{dd}. This transistor can be removed as the trimmer is capable of compensating for the mismatch introduced by its structure.

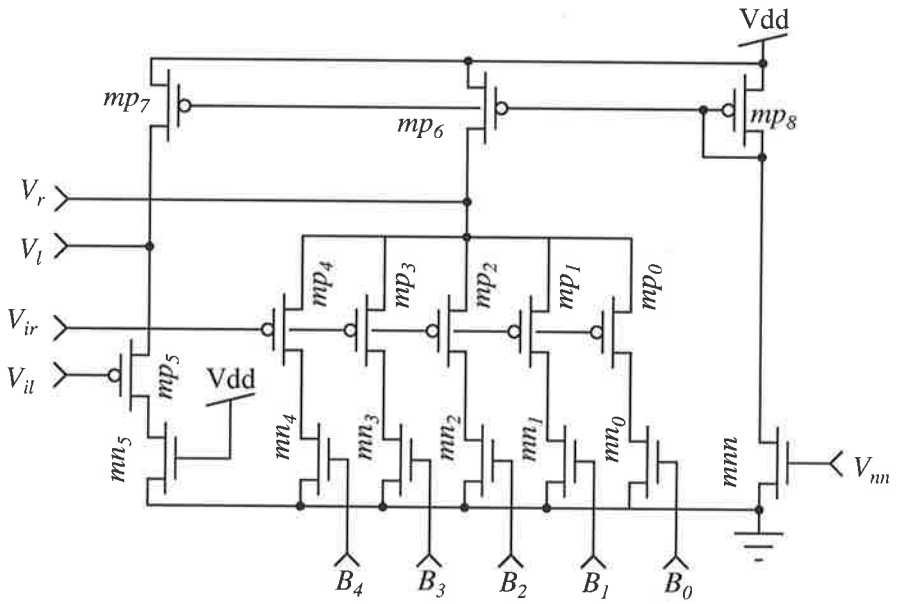

Figure 3.12. A schematic diagram of the digitally programmable arms. This structure was fabricated and used to measure the introduced input offset voltage between V_r and V_l. The transistor sizes of this circuit are listed in Table 3.4. During the measurements the ground was used as a reference point by connecting both of V_{ir} and V_{il} to ground.

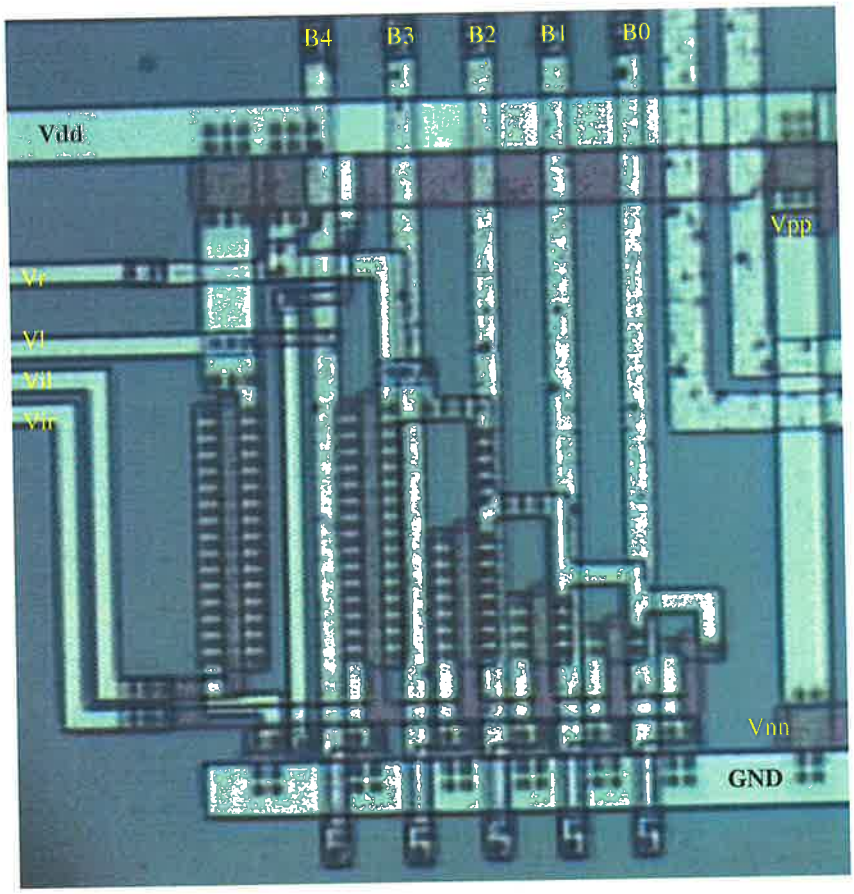

Figure 3.13. A micro-photograph of the fabricated of the digitally programmable trimmer arms. This corresponding schematic diagram of this micrograph is the schematic circuit diagram shown in Figure 3.12 with the transistor sizes listed in Table 3.4.

The bias current circuit used to bias the trimmer arms is the bandgap reference circuit discussed in [Tsividis & Ulmer 1978] and shown in Figure 3.14. The reference voltage measurements of this bias circuit from four fabricated chips as function the supply voltage using a 100 kΩ and 1 MΩ are shown in Figures 3.15 and 3.16, respectively. The measurements for the trimming arms from four fabricated chips were conducted at 3 and 5 Volt supplies to compare the results as shown in Figures 3.17 and Figure 3.18, respectively. The state at which all mn_0 to mn_4 are 'OFF' is not plotted to show the dynamic range of interest. With the aid of the data presented in Figures 3.17 and 3.18 or the raw data listed in Appendix F, the voltage difference ΔV_o between V_l and V_r after trimming at different supply voltages are presented in Table 3.5.

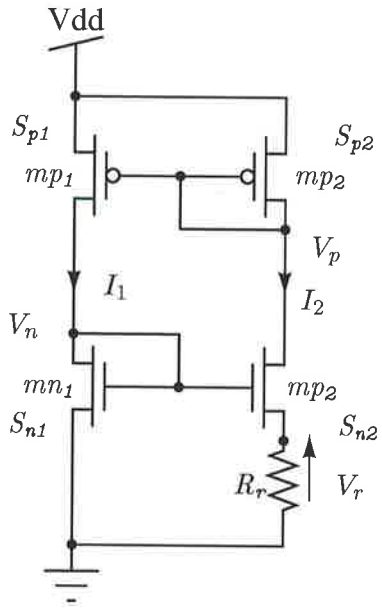

Figure 3.14. The bandgap voltage reference circuit. This circuit was used to generate the require low reference current to bias the programmable arms. The reference current is as function of the ration of transistors mn_2 and mn_1 and the resistor value of

3.6 Summary

In this chapter, two new techniques called the weighted voltage and weighted current techniques suitable for standard CMOS technologies were presented and discussed. These techniques provide: (1) a wide dynamic range for offset voltage cancellation; (2) an offset voltage cancellation independent of the absolute value of the process parameters; (3) possible compensation for mismatch in the introduced hardware; (4) moderate consumption of silicon area compared to other cancellation techniques. The proposed techniques are very attractive for use in the auto-zero technique discussed in Section 3.3.3 because they do not require a DAC for the offset tuning scheme shown in Figure 3.6.

The weighted-voltage technique provides a direct relation between the introduced input offset voltage and the input offset voltage, while the weighted current has an indirect relationship. Moreover, one of the weighted voltage techniques provides digital trimming of the input offset voltage without affecting the amplifier architecture. Making the technique attractive in trimming different amplifier architectures. For the weighted voltage technique, three methods to digitally trim the input offset voltage were discussed. The first method is most suited to the design of voltage comparators with a reference voltage above ground, while methods two and three provide input free terminals. In the third method,

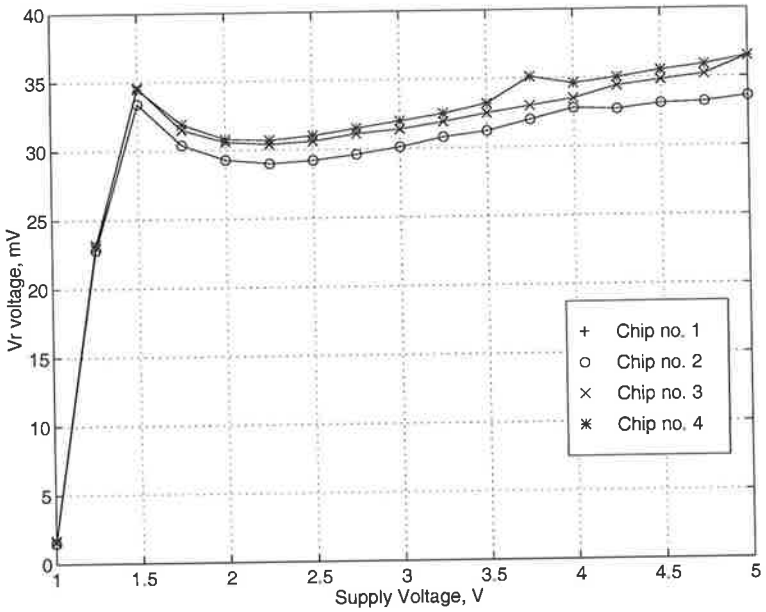

Figure 3.15. Measurements of the bandgap voltage reference circuit as function of the supply voltage using 100 kΩ resistor. These measurements show the dependence of the reference voltage V_R on the supply voltage for four fabricated chips.

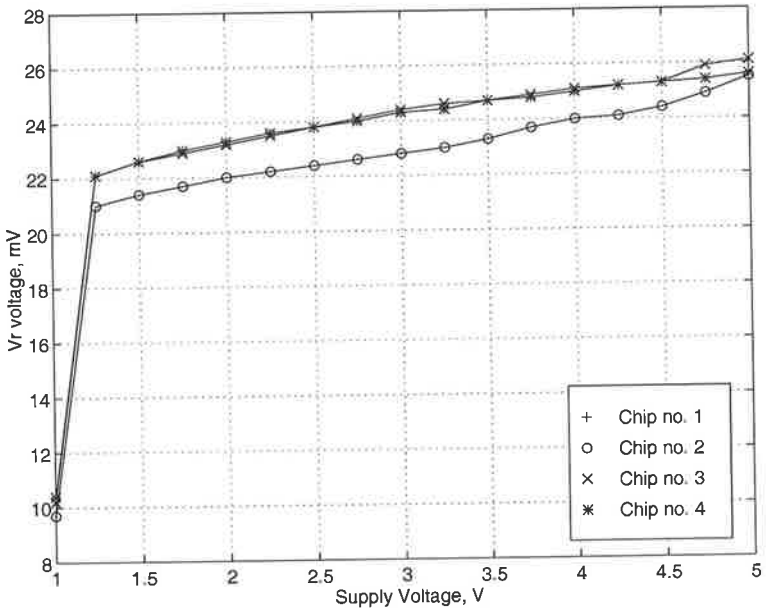

Figure 3.16. Measurements of the bandgap voltage reference circuit as function of the supply voltage using a 1 MΩ resistor. These measurements show the dependence of the reference voltage V_R on the supply voltage for four fabricated chips.

Table 3.4. The transistor sizes of the digitally programmable arms. These sizes are in terms of width to length ratio (in micrometers) for the schematic circuit diagram shown in Figure 3.12.

nMOS		pMOS	
$mn_0 = 4/2$	$mn_3 = 4/2$	$mp_0 = 4/4$	$mp_5 = 64/4$
$mn_1 = 4/2$	$mn_4 = 4/2$	$mp_1 = 8/4$	$mp_6 = 12/12$
$mn_2 = 4/2$	$mn_5 = 4/2$	$mp_2 = 16/4$	$mp_7 = 12/12$
		$mp_3 = 32/4$	$mp_8 = 12/12$
		$mp_4 = 64/4$	

as well as free input terminals, it provides buffering of input terminals and extension of the common mode range. Even though, the weighted-current technique does not provide a direct relation between the introduced input offset voltage and the amplifier V_{os}. The technique does provide offset voltage trimming without affecting the input terminals of the amplifier with small silicon area. One of the trimming techniques was verified experimentally through measuring the trimmer arms separately and through incorporating the trimming as part of a digitally programmable comparator, using ground as a reference voltage.

In this chapter it was demonstrated targeting circuit and algorithmic design levels can be used to reduced the area requirement and power consumption of mixed analog-digital circuits. The performance improvement at the circuit level is through the digitally programmable circuit structures, and at the architectural level through controlling the weighting scheme in the programmable structure and including the circuit module as part an automated offset voltage cancellation. In the next chapter we will show how targeting the circuit level design using new controlled conductances can be used to design low power circuits such as Schmitt triggers.

Table 3.5. Minimum voltage difference measured between the trimmer's arms from four fabricated chips. The minimum voltage difference measured for four fabricated chips at the trimmer output, ΔV_o, as function of the trimmer switches states at 3 and 5 Volt supplies. These measurements show the minimum voltage that can be trimmed using the weighted-voltage technique.

Supply	**Chip 4**		**Chip 3**	
Voltage	$S_4 \cdots S_0$	ΔV_o	$S_4 \cdots S_0$	ΔV_o
3 Volt	01110	-0.5 mV	10000	0.6 mV
5 Volt	01110	0.3 mV	10000	0.1 mV
Supply	**Chip 2**		**Chip 1**	
Voltage	$S_4 \cdots S_0$	ΔV_o	$S_4 \cdots S_0$	ΔV_o
3 Volt	10010	0.5 mV	10000	1.8 mV
5 Volt	10010	- 0.1 mV	10000	1.6 mV

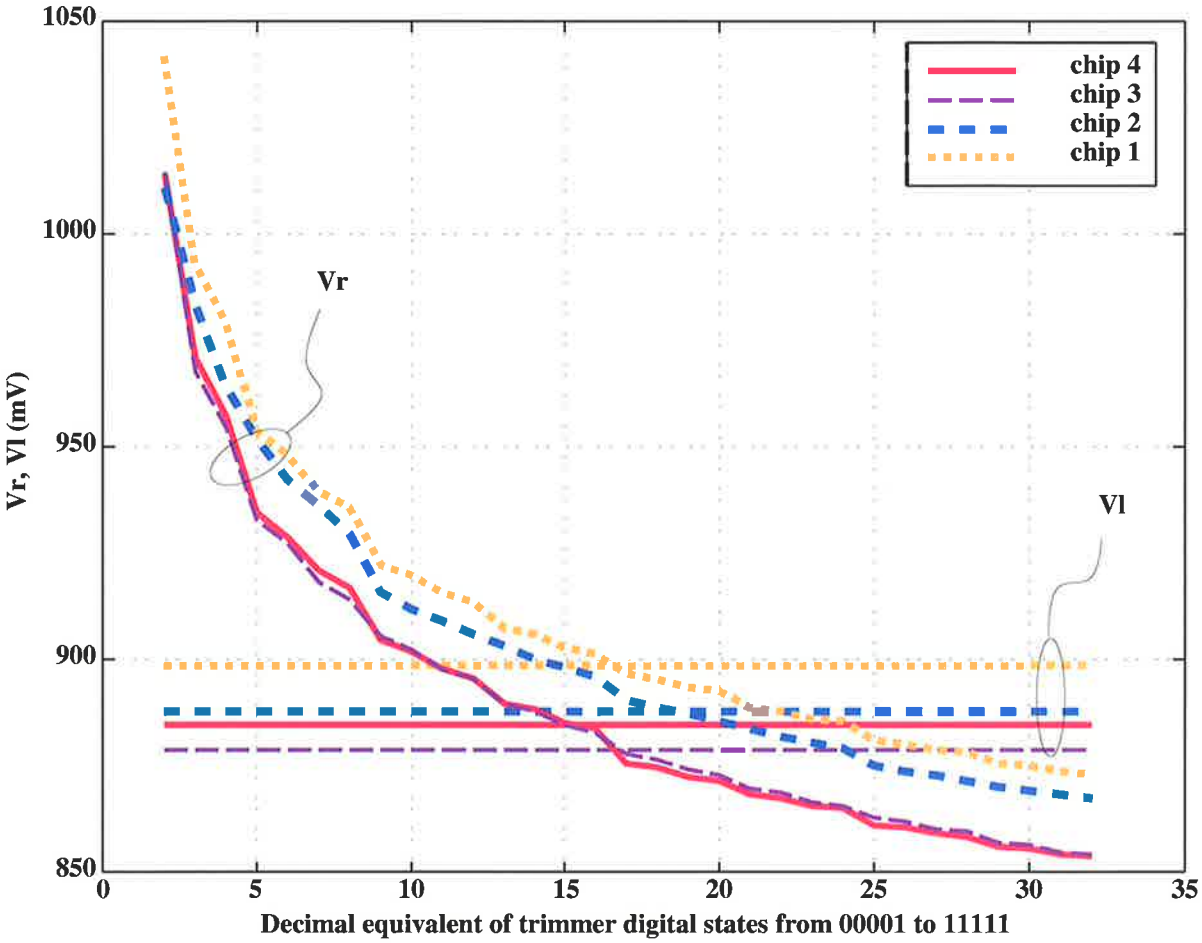

Figure 3.17. Measured voltage difference between the trimmer's arms as function of the state of digitally programmable switches. These measurements were conducted using a 3 Volt power supply and a 24 nA bias current. The measurements show that at states below $S_4 \cdots S_0 = 10000$ the voltage difference between state is large, while at state value larger than $S_4 \cdots S_0$, the difference voltage difference between state is small, hence better cancellation on the input offset voltage.

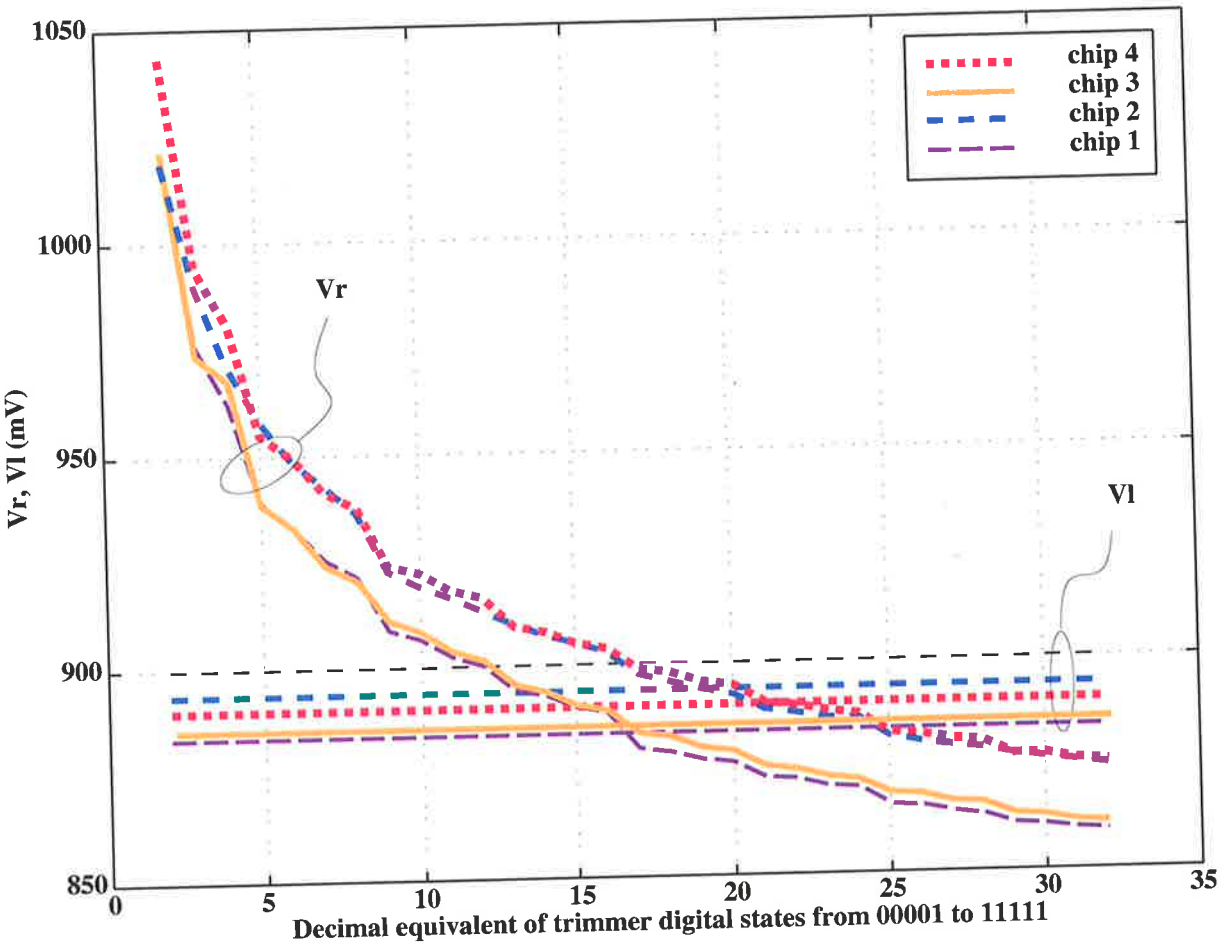

Figure 3.18. Measured voltage difference between the trimmer's arms as function of the state of digitally programmable switches. These measurements were conducted using a 5 Volt power supply and a 26 nA bias current. The measurements show similar characteristics as shown in Figure 3.17 in that at states below $S_4 \cdots S_0 = 10000$ the voltage difference between state is large, while at state value larger than $S_4 \cdots S_0$, the difference voltage difference between state is small, hence better cancellation on the input offset voltage.

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Chapter 4

New Schmitt Trigger Circuits

IN mixed signal systems, there is usually a need to digitise analog signals and sometimes a need to square up fast digital signals. The circuit that performs this function in both cases is called a comparator. In the case of a comparator with hysteresis, the transition of the comparator from one state to another can be governed by positive feedback and only relies on the input signal to trigger this positive feedback. Such a circuit is commonly referred to as a Schmitt trigger, because the functionality of the circuit mimics the vacuum-tube version invented by Schmitt in the 1930s. A formal definition of Schmitt trigger circuits will given in this chapter.

In this chapter new techniques to design Schmitt trigger circuits with wide hysteresis and low power are presented and discussed. This is achieved by using a voltage controlled resistor to modulate the hysteresis to increase its width and reduced the short circuit current of the circuits. A low power Schmitt trigger version is presented and compared to other circuits in the literature and showed very good performance in terms of power and drivability to a capacitive load.

4.1 Introduction

Schmitt trigger circuits are in a class of bistable circuits. These circuits "can exist indefinitely in either of two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation" [Millman & Taub 1965a]. It is possible to build these bistable circuits using two stage regenerative amplifiers as shown in Figure 4.1. Such a configuration is known by a wide variety of names, such as a *bistable multivibrator*, *Eccles Jordan circuit*, *trigger circuit*, *scale-of-2 toggle circuit*, *flip-flop*, and *binary* circuit. The difference between these circuits is related to the way the feedback mechanism from the input of the binary circuit to the output is provided. If the circuit shown in Figure 4.1 has unique feedback mechanism as shown in Figure 4.2 (in that the feedback is provided through connecting Z_1 and Z_2 to ground through a resistor called R_z and the coupling from the output Y_2 of the second stage amplifier A_2 to the input of the first stage amplifier A_1 is missing), such a circuit is referred to as *cathode-coupled binary* or *emitter-coupled binary*. Quite commonly, in the literature, either circuit is referred to as a Schmitt trigger, after the inventor of the vacuum-tube version in late 1930s [Millman & Taub 1965b, *Otto Schmitt's patents and publications* 2002].

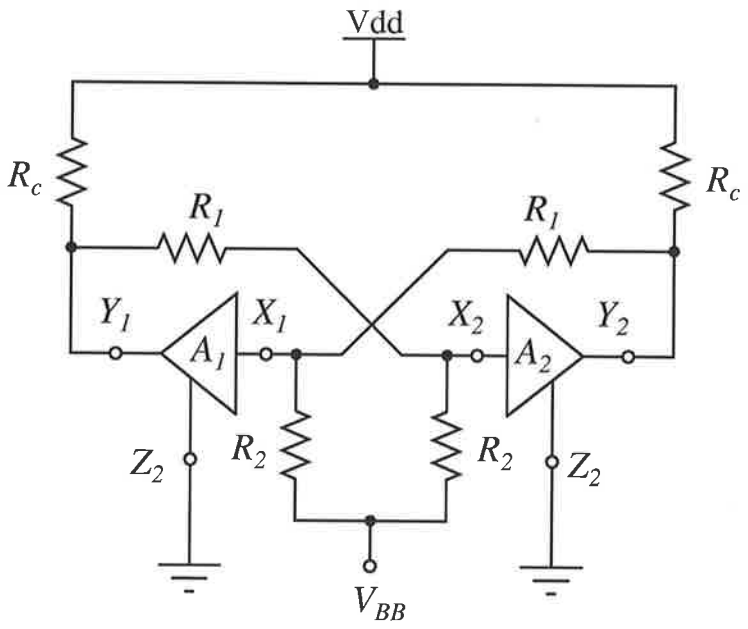


Figure 4.1. A binary circuit with two amplifying devices A_1 and A_2. These devices can be either vacuum tubes or transistors.

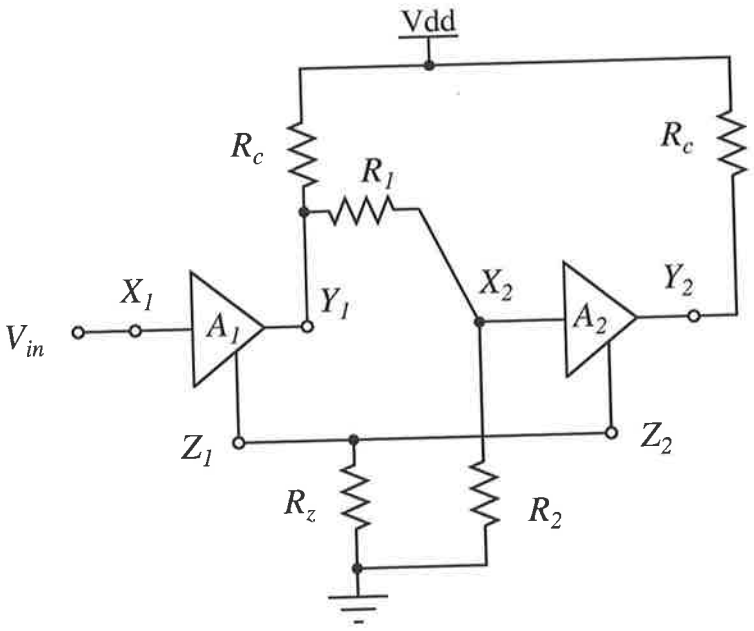


Figure 4.2. A Schmitt trigger circuit based on the binary circuit shown in Figure 4.1. This circuit shows the embedded feedback mechanism through R_z that distinguishes Schmitt trigger circuits. This feedback does not exist in the basic binary circuit shown in Figure 4.1.

The two main properties of bistable multivibrator circuits are: Firstly, the path from one state to the other is not the same, thus forming a hysteresis loop. Secondly, the transition from one state to another is carried out by a regenerative action within the circuit and not as a function of the circuit input signal. The role of the input signal is to trigger this regenerative action, which will force the circuit into another state. Even though the first circuit proposed by Schmitt was a bistable circuit, other ternary and tri-state circuits which have a regenerative action are also called Schmitt triggers [Ramkumar & Nagaraj 1985, Bundalo & Dokic 1989]. It has become common in the literature to denote any circuit that exhibits characteristics similar to Schmitt's valve circuit as a 'Schmitt trigger circuit.' These circuits are used (*i*) in mixed mode systems to convert a slowly varying analog signal to an almost discontinuous signal having abrupt jumps, (*ii*) in measurement systems to eliminate comparator chatter in signal shaping, (*iii*) for noise rejection in line receivers, (*iv*) in signal processing systems, (*v*) in ON-OFF control systems, (*vi*) in oscillators, and in neural networks [Di Cataldo & Palumbo 1990, Di Cataldo & Palumbo 1992b, Smith & Portmann 1989].

The importance of the Schmitt trigger is evident from the large number of publications that discuss the different approaches to analyse such circuits [Dokic 1984, Ahmad

et al. 1990, Dickes & Carlton 1982, Kennedy & Chua 1991, Ridders 1986, Ridders 1985, Abuelma'atti 1985, Smith 1988, Filanovsky & Baltes 1994] and the large number of circuits [Nagaraj & Satyam 1981, Steyaert & Sansen 1986, Dokic *et al.* 1988, Enning 1990, Pfister 1992, IBM 1986, Dokic 1996] designed to mimic the functionality of Schmitt's original prototype. There are other approaches to the implementation of Schmitt trigger circuits: Firstly through using special devices such as the *lambda diode* and *lambda transistor* [Ramkumar & Nagaraj 1985, Ramkumar & Satyam 1989] – the *lambda-diode* is a two terminal negative resistance device consisting of complementary depletion type FET transistors. Secondly through using a three terminal voltage-controlled negative resistance device consisting of a combination of an nMOS and a bipolar transistor. Schmitt trigger circuits based on these lambda devices are unattractive in standard CMOS technologies as they either require a specially characterised process or specially characterised devices that are not available in standard CMOS technologies, although an opamp with positive feedback can be used as a Schmitt trigger circuit. This approach requires using either passive or active feedback networks in addition to at least a 7-transistor differential amplifier and a bias circuit. Moreover, this takes up larger silicon area and consumes more power compared with the circuits presented in this chapter.

In most of the published Schmitt trigger circuits, the aspect of low power operation has not been considered – this sometimes being due to the methodology used in designing such circuits or due to the irrelevance of this aspect to the target application. Generally, these circuits are suitable for medium power applications. The requirement for low power Schmitt circuits has prompted the development of new techniques to reduce both power and area requirements of these circuits. In this research, the later is achieved by new techniques to modulate the hysteresis of Schmitt trigger circuits, which resulted in both area and power reduction of new families of Schmitt trigger circuits that are compatible with standard CMOS technologies. The techniques are presented through the discussion of the new Schmitt trigger circuits families in the following sections. Also, techniques to obtain adjustable hysteresis Schmitt trigger circuits are presented and discussed. These circuits can find use in communications applications [Di Cataldo & Palumbo 1992b] and neural networks [El-Leithy *et al.* 1989].

Schmitt triggers can be classified into two groups. The first group is called the voltage mode Schmitt trigger in which the input signal is a voltage, and which may be accompanied by insignificant amount of current. This group is usually referred to as 'Schmitt triggers' without reference to the input signal type. The second group is the current mode Schmitt [Wang & Guggenbuhl 1988, Wang & Guggenbuhl 1989, Di Cataldo &

Palumbo 1992a, Chavez 1995]. These circuits are associated with a low or a non-linear incremental input resistance and usually driven by current.

In this chapter two new families of Schmitt trigger circuits are discussed. The prototype circuit of the first family is considered to be a truly low power circuit, and is discussed in Section 4.2. The second prototype circuit, which exhibits a finite input impedance, is discussed in Section 4.3. Section 4.4 presents experimental results for one of the circuits discussed in Section 4.2. Section 4.5 provides a discussion on the performance of the new low power Schmitt trigger circuits in comparison with other Schmitt trigger circuits presented in the literature, while Section 4.6 draws conclusions on the suitability of the different Schmitt trigger circuits presented in this research for various applications. Appendix D discusses the context were the developed circuits are used in designing oscillators that can be used in a wide range of applications.

4.2 Low Power Prototype CMOS Schmitt Trigger Circuit

After investigating the different types of Schmitt trigger circuits, in particular the bipolar version discussed in [Millman & Taub 1965b] and the CMOS versions discussed in [Dokic 1984, Steyaert & Sansen 1986], it was found that a Schmitt trigger circuit with large hysteresis can be designed by using two methods: firstly by designing a switching circuit that has a regenerative action from the output to the input, secondly by modulating the switching points in the switching circuit by its output to increase the hysteresis width. Based on these findings a conceptual circuit using bipolar transistors is shown in Figure 4.3. This circuit operates as a Schmitt trigger circuit even without modulating the value of resistor R_e. However, the hysteresis is small. A detailed analysis of this circuit without the voltage controlled resistor is presented in [Millman & Taub 1965b]. The switching points of this circuit are not given as they do not serve a significant purpose. However, analysis of the CMOS version will be presented.

4.2.1 An nMOS Schmitt Trigger

A corresponding CMOS version of the circuit shown in Figure 4.3 can be obtained by replacing all the npn transistors in Figure 4.3 with nMOS transistors. Secondly, replacing the load resistors R_{c_1} and R_{c_2} by pMOS transistors. Thirdly, replacing the emitter resistor R_e with a voltage controlled resistor, which can be simply implemented as an nMOS transistor operating in the triode region. The resultant circuit after all of these changes

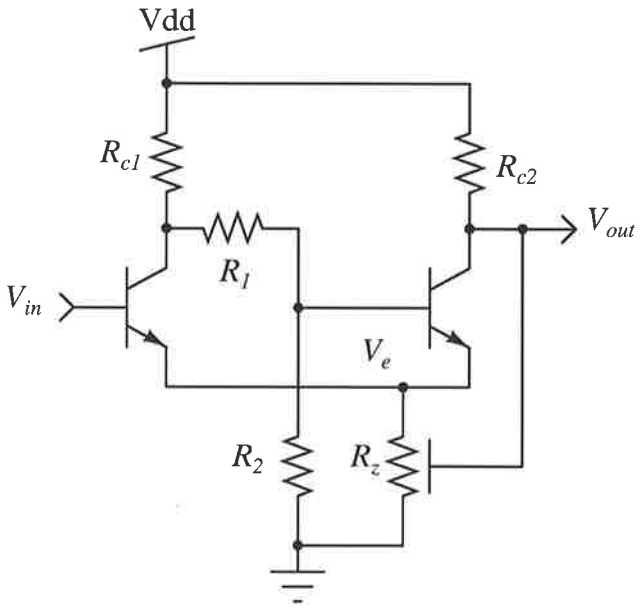


Figure 4.3. A conceptual Schmitt trigger circuit with large hysteresis in bipolar technology. This circuit shows how the value of the feedback resistor R_z can be modulated to increase the hysteresis width of the Schmitt trigger circuit.

is shown in Figure 4.4. The switching points of this circuit are derived analytically in the next paragraph.

The input voltage at which V_{out} switches from low to high, V_{LH} can be derived by finding the state of the circuit when the input voltage, V_{in}, is low. In this case, V_m is high and V_{out} is at V_n, because mn_3 is fully on. The Schmitt trigger circuit can be simplified as shown in Figure 4.5. The input signal at which V_{out} switches from low to high, V_{LH}, is given by

$$V_{LH} = V_n + \frac{V_{dd} + V_{th}(\kappa - 1) - V_n}{\kappa + 1}. \tag{4.1}$$

where $\kappa = \sqrt{\frac{\beta_{mn_2}}{\beta_{mp_2}}}$, β_i is the transconductance parameter for the transistor i on the Figure 4.5, V_{dd} is the supply voltage and $V_{th} = V_{tn} = |V_{tp}|$ are assumed, to simplify the analysis.

The relation between V_{in} and V_n can be found by considering the fact that both mn_1 and mn_2 are operating in the saturation region, just before switching, as long as V_{in} is larger than the sum of V_n and the threshold voltage of mn_2. Hence, the current equations for mn_1 and mn_2 can be written as

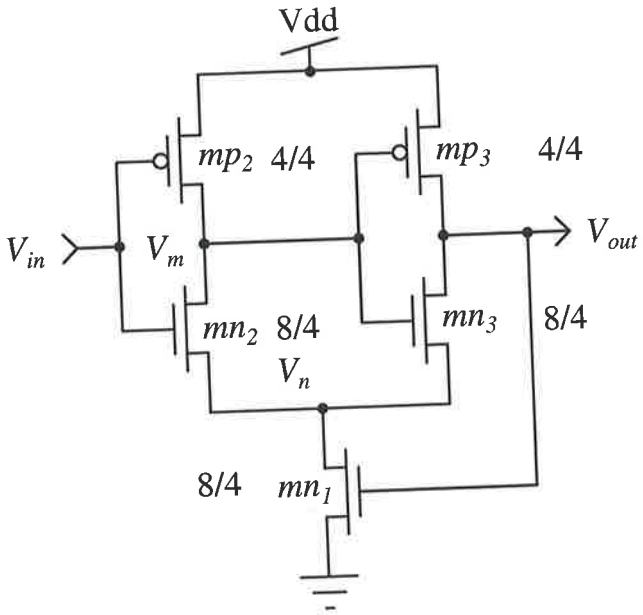


Figure 4.4. A wide hysteresis CMOS Schmitt trigger derived from the bipolar version. This version was derived from the bipolar version with load resistors R_{c1} and R_{c2} replaced by pMOS transistors, and the voltage controlled resistor, R_z, replaced by an nMOS transistor operating as a voltage controlled resistor.

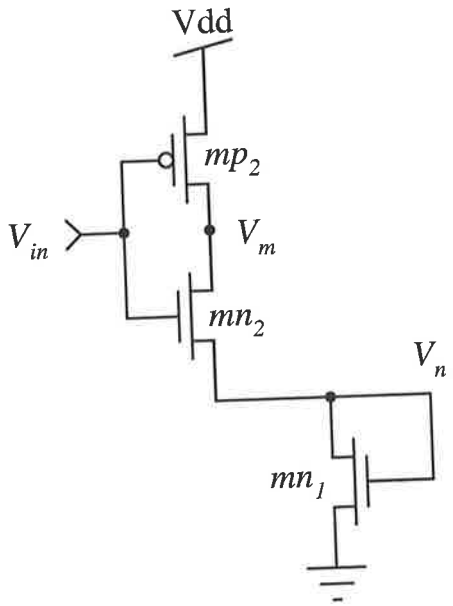


Figure 4.5. A simplified Schmitt trigger circuit with its input signal is low. This circuit will be used to drive the switching point of the Schmitt trigger circuit when the output switches from high to low.

$$I_{mn_1} = \frac{\beta_{mn_1}}{2}(V_n - V_{th})^2 \tag{4.2}$$

$$I_{mn_2} = \frac{\beta_{mn_2}}{2}(V_{in} - V_n - V_{th})^2. \tag{4.3}$$

Solving Equations 4.2 and 4.3 for V_n, then substituting $\kappa_n = \sqrt{\frac{\beta_{mn_1}}{\beta_{mn_2}}}$ results in

$$V_n = \frac{V_{in}}{1+\kappa_n} - V_{th}\frac{(1-\kappa_n)}{(1+\kappa_n)}. \tag{4.4}$$

Substituting Equation 4.4 in 4.1 at $V_{in} = V_{LH}$, Equation 4.1 can be written as

$$V_{LH} = V_{dd}\frac{(\kappa_n+1)}{\kappa_n(\kappa+1)+1} + V_{th}\frac{(\kappa_n\kappa-1)}{(1+\kappa_n)(1+\kappa)}. \tag{4.5}$$

The input voltage at which V_{out} switches from high to low, V_{HL}, can be calculated by finding the switching point of the inverter structure formed by mn_2 and mp_2, taking into account the dynamic resistance of mn_1 in the linear region of operation. The current equations for mn_2 and mp_2 can be written as

$$I_{mp_2} = \frac{\beta_{mp}}{2}(V_{in} - V_{dd} - V_{tp})^2 \tag{4.6}$$

$$I_{mn_2} = \frac{\beta_{mn}}{2}(V_{in} - I_{mn_2}R_{dym} - V_{tn})^2. \tag{4.7}$$

We can now solve these equations with $I_{mp_2} = -I_{mn_2}$ for V_{in} at $V_{in} = V_{HL}$, where I_{mp_2} and I_{mn_2} represent the currents passing through mp_2 and mn_2, respectively. R_{dym} is the dynamic resistance of mn_1 which can be approximated as $1/(\beta_{mn_1}(V_{dd} - V_{tn}))$. Based on the above equations, V_{HL} switching point can be written as

$$V_{HL} = \frac{V_{dd} - V_n + V_{th}(\kappa-1)}{\kappa+1} + V_n. \tag{4.8}$$

As the voltage swing at V_{out} does not fully go to ground potential, the output of the above Schmitt trigger circuit can be either taken from V_{out} after using a special circuit that switches from rail-to-rail or by taking the output from node V_m. The voltage at this node is the complement of V_{out} with a rail-to-rail voltage swing. Care should be taken to avoid loading V_m, as the load capacitance at this node limits the switching speed of the Schmitt trigger circuit.

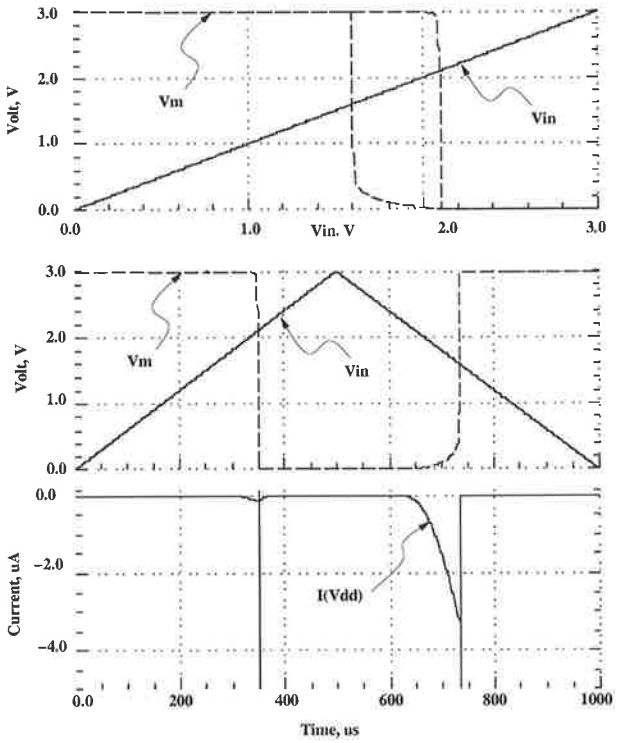


Figure 4.6. Simulation results of the Schmitt trigger circuit shown in Figure 4.4. The upper panel shows the output characteristics of the circuit at node V_m as function of the input signal, the middle panel shows the the input-output characteristics of the Schmitt trigger circuit as function of time, the lower panel shows the current drawn from the power supply as function of the input signal in the time domain.

The Schmitt trigger circuit shown in Figure 4.4 was simulated using HSPICE with Level 13 model parameters as shown in Figure 4.6. The input signal is a piecewise linear function with the input voltage increasing from ground to V_{dd} in 500 μs, then decreasing to ground at the same rate. As expected from the previous analysis, the switching point from high to low, V_{HL}, is shifted from $V_{dd}/2$ by $\sim$ 100 mV, which is equal to the voltage at V_n (not shown). Secondly, the current drawn from the power supply in case of switching from high to low, V_{HL}, is much larger than the current drawn when the circuit switches from low to high, V_{LH}, as shown by the bottom waveform in Figure 4.6.

4.2.2 A pMOS Schmitt Trigger

Another Schmitt trigger circuit can be obtained by replacing the nMOS transistors with pMOS transistors and vice versa in Figure 4.4, in addition to switching the supply voltage terminals, resulting in the circuit shown in Figure 4.7. The switching points, V_{HL} and V_{LH}

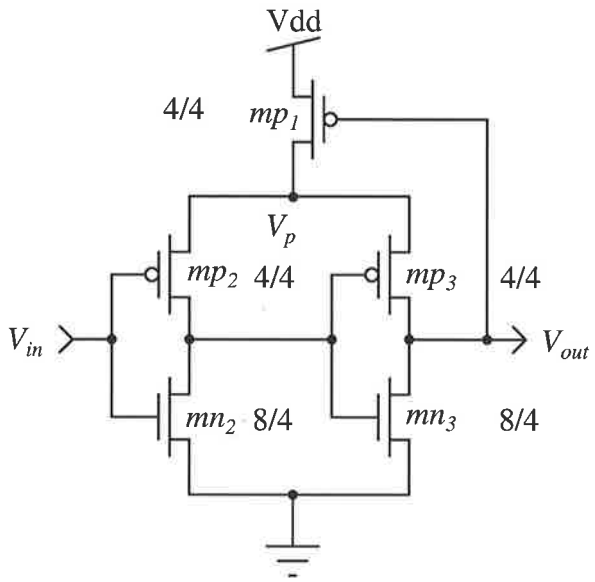


Figure 4.7. A pMOS Schmitt trigger derived from the nMOS Schmitt trigger circuit shown in Figure 4.4. This circuit can be derived from the nMOS by intuition from Schmitt trigger circuit shown in Figure 4.4 by changing the MOS transistor mn_1 to mp_1 and switching the power supply terminals.

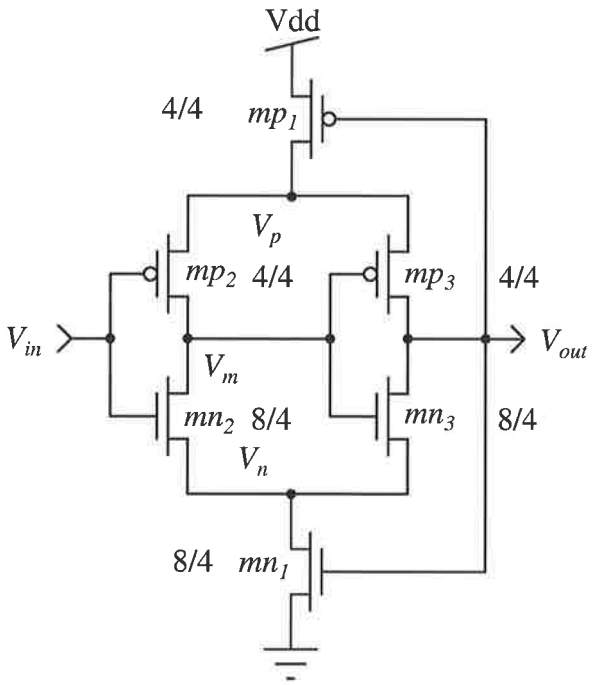


Figure 4.8. A new CMOS Schmitt trigger circuit. This circuit was obtained by merging the circuits shown in Figures 4.4 and 4.7 into a complementary structure.

can be found by following the same analytical procedures used in deriving these switching points for the circuit shown in Figure 4.4, or by benefiting from the similarity between the two Schmitt trigger structures. The later is achieved by subtracting Equations 4.5 and 4.8 from V_{dd} and replacing V_n by V_p and κ_n by κ_p, where κ_p is defined as $\sqrt{\frac{\beta_{mp_1}}{\beta_{mp_2}}}$, resulting in

$$V_p = \frac{V_{in}}{(1+\kappa_p)} - V_{th}\frac{(1-\kappa_p)}{(1+\kappa_p)} - V_{dd}\frac{\kappa_p}{(1+\kappa_p)}, \tag{4.9}$$

$$V_{LH} = V_{dd}\frac{\kappa}{(\kappa+1)} + V_{th} - V_p\frac{(\kappa-1)}{(\kappa+1)}, \tag{4.10}$$

$$V_{HL} = V_{dd}\frac{\kappa_p\kappa}{\kappa_p(\kappa+1)+1} + V_{th}\frac{(\kappa_p\kappa-1)}{(1+\kappa_p)(1+\kappa)}. \tag{4.11}$$

The simulation results for the pMOS Schmitt trigger are not presented, because they are similar to the simulation results of the nMOS version shown in Figure 4.4 with different switching points. However, this structure was presented to assess the presentation of the complementary structure Schmitt trigger circuit presented in the next subsection.

4.2.3 Fully Symmetrical CMOS Schmitt Trigger

As the switching point from low to high of the nMOS version and the switching point from high to low in the pMOS version drains a very small amount of current from the power supply, merging the nMOS and pMOS version in one circuit will produce a Schmitt trigger circuit that firstly has a very wide hysteresis width and more importantly draws a very small amount of current from the power supply during switching. The resultant circuit is shown in Figure 4.8. The switching points of this circuit can be found as follows. When the input signal increases from low to high, this circuit can be approximated to the Schmitt trigger circuit shown in Figure 4.4. The input voltage at which V_{out} switches from low to high, V_{LH}, and from high to low, V_{HL}, are given by Equations 4.5 and 4.11, respectively. The hysteresis width of the fully symmetrical, low power Schmitt trigger circuit can be calculated by subtracting Equation 4.11 from 4.5 and assuming that $\kappa_n = \kappa_p$, resulting in

$$V_{HW} = V_{dd}\frac{\kappa_n(1-\kappa)+1}{\kappa_n(1+\kappa)+1}. \tag{4.12}$$

Equation 4.12 shows that the hysteresis width is independent of the MOS transistors threshold voltage assuming that their absolute threshold voltage values are equal, and $\kappa_p = \kappa_n$. To check the consistency of the above equations, let us assume that κ, κ_n and

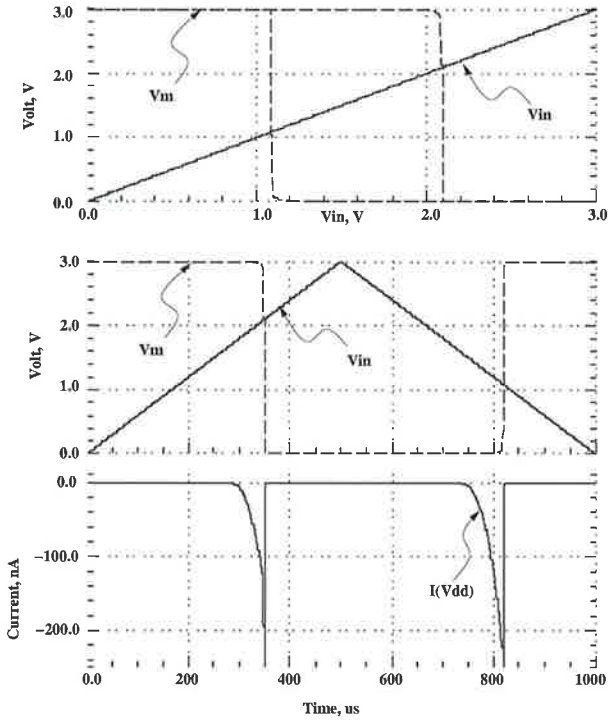


Figure 4.9. Simulation results of the complementary Schmitt trigger circuit shown in Figure 4.8. The upper panel shows the output characteristics of the circuit at V_m as function of the input signal, the middle panel shows the input-output characteristics of the circuit as function of time, the lower panel shows the current drawn from the power supply as function of the input signal in the time domain.

κ_p are all equal to 1, while V_{dd} is set to 5 V. According to Equations 4.5, 4.11 and 4.12, the numerical values for the V_{LH}, V_{HL} and V_{HW} of the low power Schmitt trigger circuit are 10/3, 5/3 and 5/3 Volts, respectively.

The circuit shown in Figure 4.8 was simulated with the same transistor sizes shown on the schematic, as shown in Figure 4.9. A number of observations can be drawn from the simulation results: Firstly, the Schmitt trigger has a large hysteresis width that is equal to $V_{dd}/3$. Secondly, the maximum current drawn from the power supply at 3 V is less than 250 nA. Thirdly, the hysteresis and the switching point for the Schmitt trigger circuit are all shifted by ~100 mV. This is equal to the difference in the threshold voltages between the n and p MOS transistors.

To investigate the switching point variation of the Schmitt trigger as function of process variation, for the circuit shown in Figure 4.8, a 100 iteration Monte Carlo analysis was conducted. These simulations were conducted by adding a zero mean Gaussian distribution voltage with a 10 mV standard deviation to the threshold voltages of the MOS

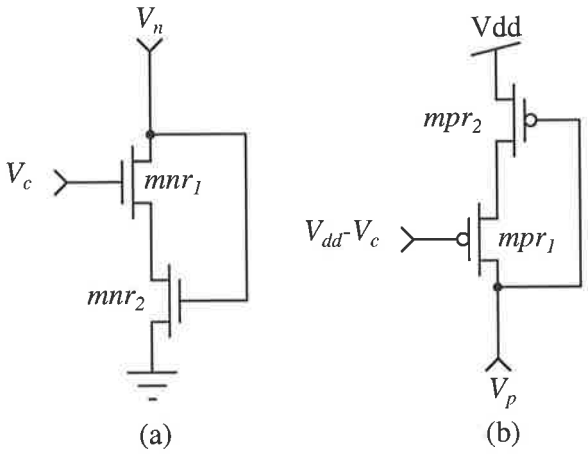


Figure 4.10. An nMOS and pMOS complementary voltage controlled grounded resistors. The value of these resistors can be controlled by either the transistor sizes of through the controlling voltage V_c.

transistors in the circuit. The results are given in Table 4.1. The simulations show that the switching points vary by less than 4%. Also the variation of the switching points as function temperature were also considered as shown in Figure 4.11. The simulations show that the switching points of the Schmitt trigger have a slight dependence on temperature resulting in less than 0.3% increase in the switching points for each °C. Both the Monte Carlo and temperature simulations show that the Schmitt trigger is robust against process and temperature variations.

4.2.4 Fully Adjustable Hysteresis CMOS Schmitt Trigger

The circuit shown in Figure 4.8 can be exploited further to give a low power, voltage controlled hysteresis Schmitt trigger circuit, or in short an adjustable hysteresis Schmitt trigger circuit. This can be achieved by a number of approaches. The first is to replace mn_1 and mp_1 by the voltage controlled resistors shown in Figures 4.10.a and b (for a detailed analysis of the nMOS structure refer to Section 2.2 in Chapter 2), resulting in the circuit shown in Figure 4.12.a. Other voltage controlled grounded resistors can be used, as long as the their value can be modulated through the Schmitt trigger output voltage and through an external voltage. The second approach is to introduce an nMOS transistor between the source of mn_2 and V_n, and a pMOS transistor between the source of mp_2 and V_p, as shown in Figure 4.12.b. The third approach is to shunt mn_1 and mp_1 with voltage controlled resistors. Such resistors can be simply a MOS transistor operating

Table 4.1. Statistical results of the low power Schmitt trigger circuit shown in Figure 4.8. These simulations show that the process variations have a small effect on the Schmitt trigger switching points. This variation is less than 4% for a zero mean Gaussian distribution voltage with a 10 mV standard deviation that was added randomly the MOS transistors threshold voltages.

	V_{LH}, V	V_{HL}, V
Mean	1.86	0.96
Max	1.87	0.98
Min	1.83	0.94
Sigma	8.2 m	9.2 m

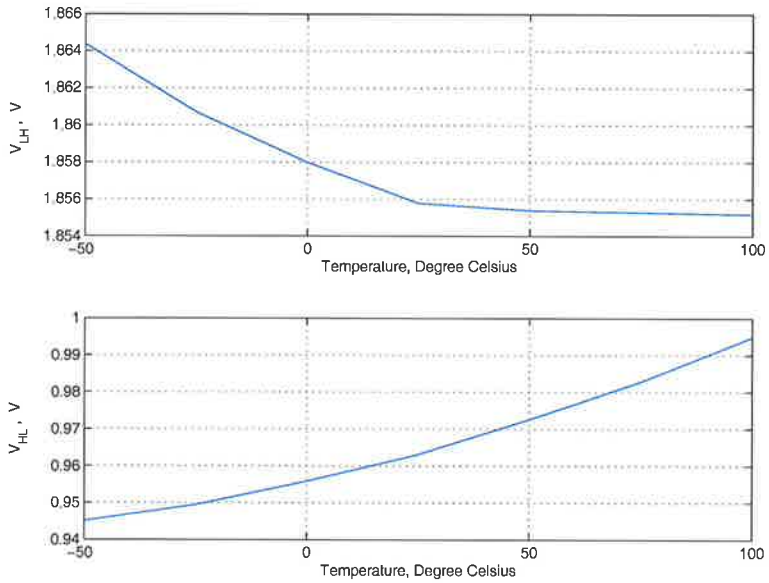


Figure 4.11. Temperature simulation results of the low power Schmitt trigger circuits. The upper panel shows V_{LH} variation vs temperature, the lower panel shows V_{HL} variation vs temperature. Both simulations show a slight variation of the switching points as function of temperature.

in the linear region as shown in Figure 4.12.c. The first two approaches can be used to increase the hysteresis width of the Schmitt trigger, while the third approach can be used to decrease the hysteresis width. The second approach is more effective than the first in increasing the hysteresis width. Because the first approach increases the voltage needed to switch both mn_4 and mp_4. The reason why the first approach is not very effective can

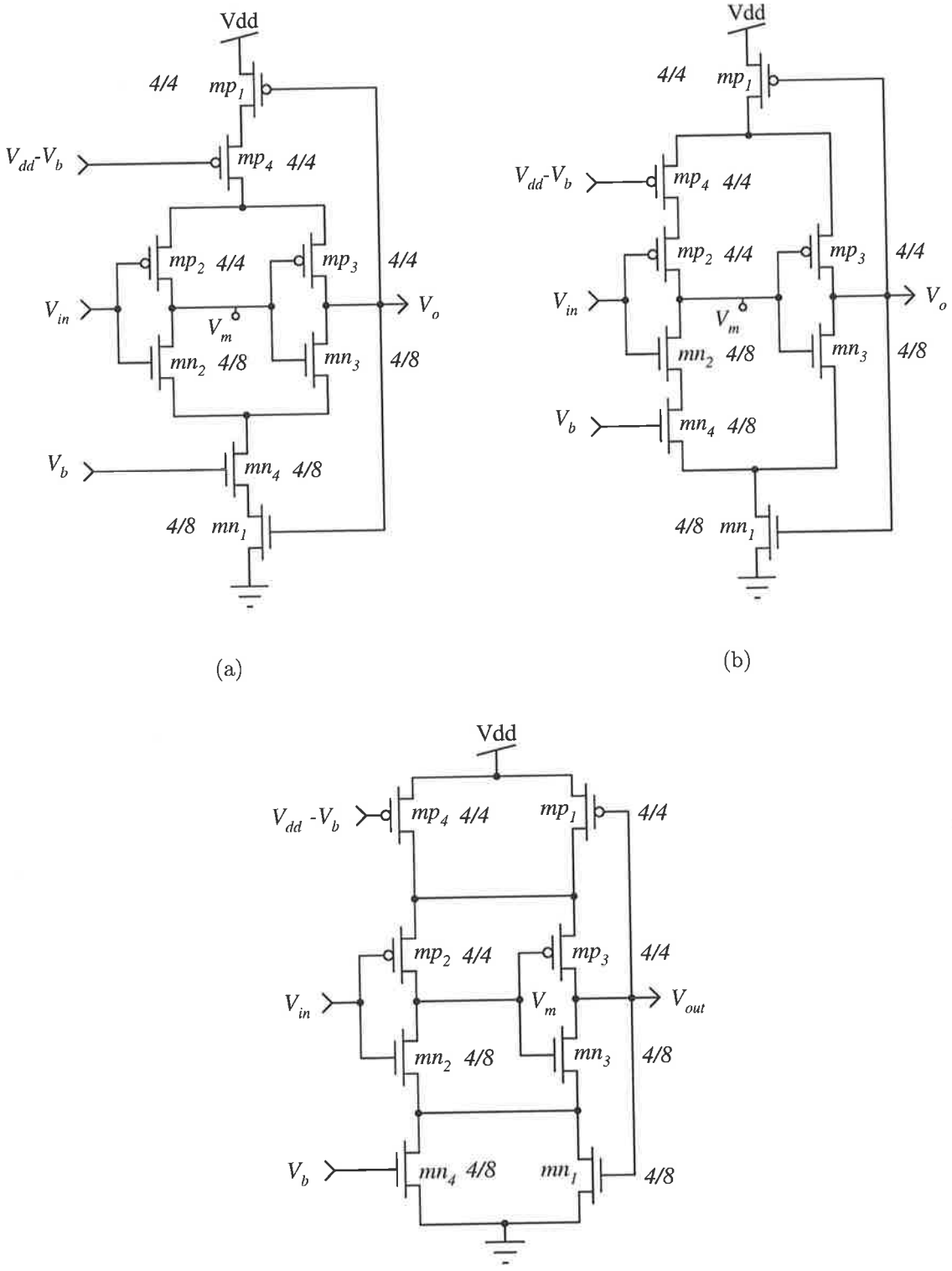


Figure 4.12. Three approaches to adjust the hysteresis width of the Schmitt trigger circuit shown in Figure 4.8. These approaches allow control of the hysteresis width as function of the controlling voltage V_b.

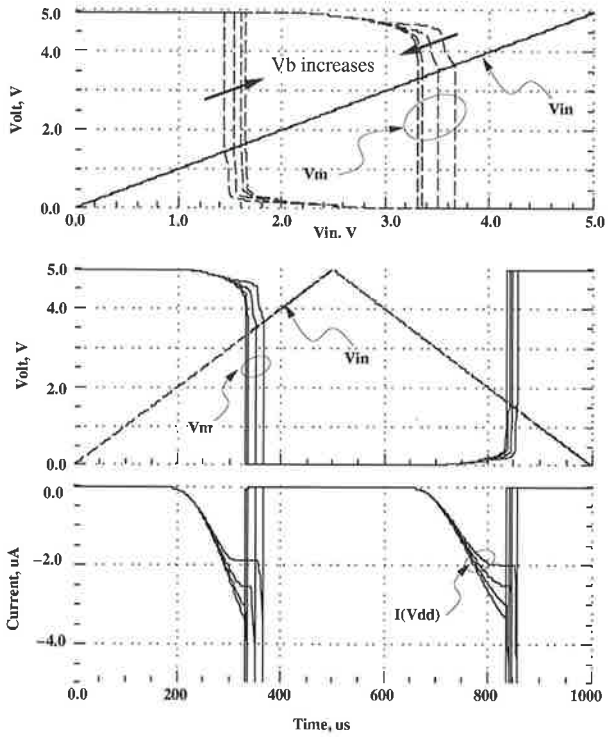


Figure 4.13. Simulation results of the adjustable hysteresis Schmitt trigger circuit shown in Figure 4.12.b. The upper panel shows the input-output characteristics with output taken at V_m, the middle panel shows the input-output characteristics of the circuit as function of time, the lower panel shows the current drawn from power supply as function of the input signal.

be related to the small dynamic range of the voltage controlled resistor as function of the bias voltage.

As the same analytical procedures used in the analysis of the low power version can be applied directly for the adjustable hysteresis circuits, the hand analysis for these circuits is not presented, instead the circuit simulator is used. The circuit shown in Figure 4.12.b was simulated with the gates of mn_4 and mp_4 tied to V_b and $V_{dd} - V_b$, respectively. Then, V_p was swept from 2.8 to 3.25 V in 0.15 V steps as shown in Figure 4.13. The simulation results for the circuit shown in Figure 4.12.c with V_p was swept from 1 to 3 V in 0.5 V steps are shown in Figure 4.14. From Figures 4.13 and 4.14, it can be seen that the hysteresis width for the above Schmitt trigger circuits is adjustable as function of an external bias voltage.

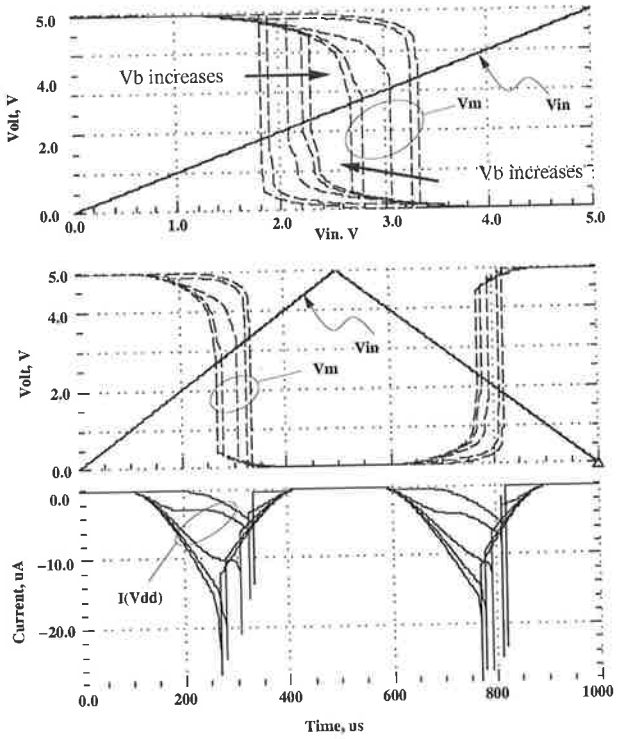


Figure 4.14. Simulation results of the adjustable hysteresis Schmitt trigger circuit shown in Figure 4.12.c. The upper panel shows the input-output characteristics with output taken at V_m, the middle panel shows the input-output characteristics of the circuit as function of time, the lower panel shows the current drawn from power supply as function of the input signal.

4.3 Finite Input Impedance (FII) Schmitt Trigger

One of the common circuits in digital electronics is the static latch, which is simply a pair of cross coupled inverters as shown in Figure 4.15 – where V_{in} and V_{out} are connected together to close the feedback loop. The latch has three operating points as shown by the graphical solution in Figure 4.16. Only two of these operating points are stable as long as the gains of the cross coupled inverters are large enough to satisfy the stability condition described in [Glasser & Dobberpuhl 1985]. The gains of cross coupled CMOS inverters are large enough to satisfy the stability conditions. Therefore the latch can be referred to as a Schmitt trigger circuit because firstly, it has a regenerative action from the output to the input. Secondly, the output does not rely on the input signal except for triggering the regenerative action. Thirdly, the circuit has two stable states only. As the input signal to the Schmitt trigger circuit is associated with a finite input impedance, the following techniques are referred to as finite input impedance (FII) Schmitt trigger circuits.

In the following subsections, simple but effective techniques to move the switching points of the static latch circuit away from the supply terminals are presented and discussed. Two techniques are presented. The first technique uses passive resistors, while the second uses active resistors as discussed in Sections 4.3.1 and 4.3.2, respectively. Section 4.3.3 presents a possible method to self bias the active resistor approach presented in Section 4.3.2.

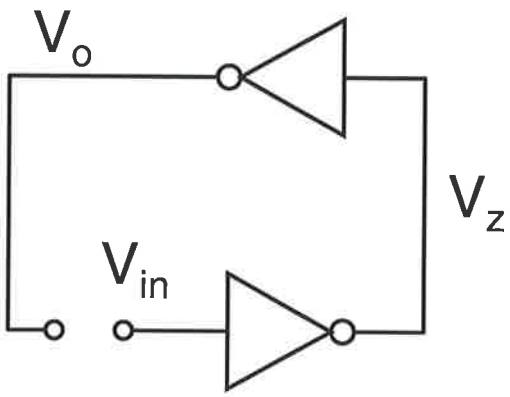


Figure 4.15. A CMOS bistable circuit. This circuit shows a simple bistable circuit that uses CMOS inverters.

4.3.1 Resistive FII Schmitt Trigger

The problem with using the latch as a Schmitt trigger is that the switching points of the latch circuit are very close to the power supply terminals' potential. The switching points can be shifted from the supply voltage rail by reducing the supply voltage of the cross coupled inverters to allow the input signal to go beyond the cross coupled inverters' supply terminals. This is accomplished by connecting the ground terminal of the latch to ground through a passive resistor as shown in Figure 4.17. The operation of the circuit can be described as follows. When the input signal V_{in} increases from ground to V_{dd}, V_{out} stays high as long as

$$V_{in} < \frac{(V_{dd} - V_{R_g}) + V_{tp} + \kappa V_{tn}}{1 + \kappa} + V_{R_g}, \tag{4.13}$$

where V_{R_g} is the voltage across R_g.

Once the above inequality becomes an equality, the input voltage at which V_{out} switches from high to low is referred to as V_{HL}. The above equation can be solved at $V_{in} = V_{HL}$

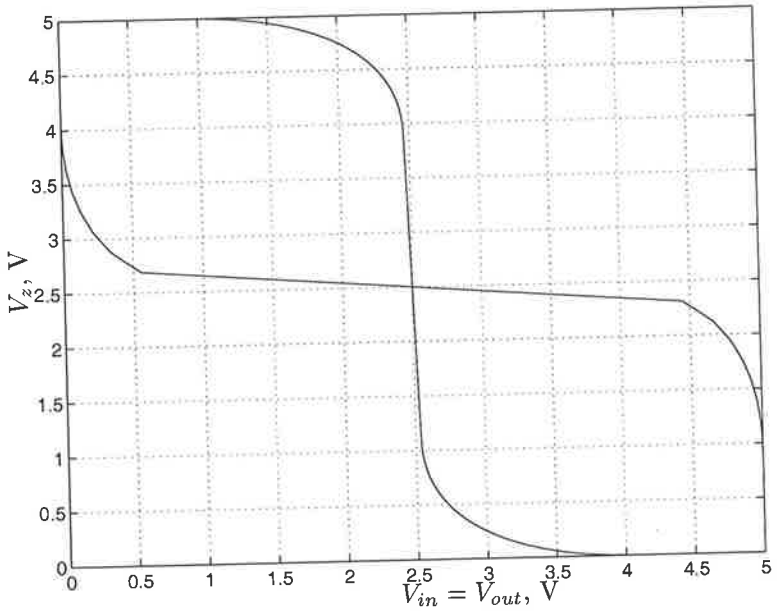


Figure 4.16. The simulated input-output characteristics of the bistable circuit shown in 4.15. These simulations show the output from input V_{out} was feed to V_{in} and the output is observed at V_z. These simulations show that there are three operating point for this structure and only of these two points are stable. The switching points are at $V_{in} = 0$ and $V_{in} = 5$ V.

by simplifying Figure 4.17 when V_{out} is high as shown in Figure 4.18. Then, writing the current equation for mn_1, which is operating in the linear region, and the voltage drop across R_g, V_{Rg}, as

$$I_{mn_1} = \beta_n[(V_{dd} - V_{Rg} - V_{tn})(V_{in} - V_{Rg}) - (V_{in} - V_{Rg})^2/2] \quad (4.14)$$

$$V_{Rg} = I_{mn1}\, R_g. \quad (4.15)$$

Substituting Equation 4.14 in 4.15 and solving for V_{Rg} gives two solutions, the feasible one is

$$V_{Rg} = V_{dd} - V_{tn} + \frac{1}{R_g\beta_n} - \sqrt{(V_{dd} - V_{in} - V_{tn})^2 + \frac{2(V_{dd} - V_{th})}{R_g\beta_n} + (\frac{1}{R_g\beta_n})^2}. \quad (4.16)$$

Substituting Equation 4.16 in 4.13 gives V_{HL}. Unfortunately, the answer is not simple and can not be put in a simple analytical form, because V_{HL} is also contained in the square root. Therefore a numerical approach will be used to calculate the V_{HL} in the following

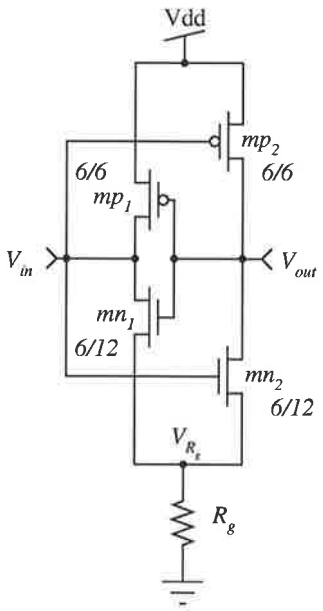


Figure 4.17. A schematic diagram of the finite input impedance Schmitt trigger circuit. This circuit uses uses resistors to move the switching points of the bistable circuit away from the supply voltages.

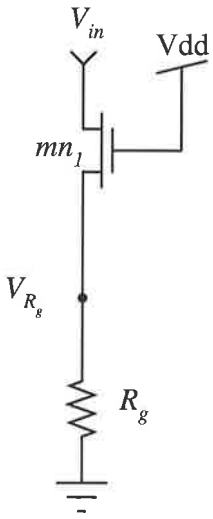


Figure 4.18. A simplified circuit a schematic diagram of the finite input impedance Schmitt trigger circuit. This circuit was derived when the output of the Schmitt trigger circuit is high.

paragraph. The input voltage at which the Schmitt trigger output switches from low to high, V_{LH}, is shifted from the expected $V_{dd}/2$, because of the current passing through mp_2 and mn_2 before switching, causing a voltage drop across R_g, hence a shift in the switching point from $V_{dd}/2$. The analytical expression for V_{LH} is not derived as the interest is to have a complementary structure of the circuit as will be discussed later in this section.

A numerical value for V_{HL} can be obtained by substituting $\kappa = 1$, $R_g = 50$ kΩ, $V_{tn} = 0.94$ V, $V_{tp} = 0.94$ V at $V_{dd} = 3$ V in Equations 4.16 and 4.13 at $V_{in} = V_{HL}$ giving $V_{R_g} = 1.18$ V and $V_{HL} = 2.09$ V. The circuit shown in Figure 4.17 was simulated using HSPICE simulator using Level 13 with fully symmetrical nMOS and pMOS transistors models. These models are used in all the following simulations with the sizes of the n and pMOS transistors set to $W/L = 6/6$ (in μm), unless otherwise stated. The simulation results are shown in Figure 4.19. The measured V_{HL} was 2.0 V compared with the 2.08 V value calculated from the above analysis, resulting in 4% error, which is acceptable in comparing an analytical results to measurements.

The circuit shown in Figure 4.17 can be exploited further to provide fully symmetrical hysteresis by using another resistor between the supply terminal of the latch and V_{dd}, as shown in Figure 4.20. The switching points V_{HL} and V_{LH} cannot also be expressed in simple analytical form. Therefore the circuit simulator was used to verify the circuit operation as the concept was verified through simple analysis. As this circuit is a fully symmetrical version of the circuit shown in Figure 4.17, the expected hysteresis width should be symmetrical around $V_{dd}/2$. This is verified by the simulation results shown in Figure 4.21. These simulations show that the hysteresis width is symmetrical around $V_{dd}/2$ and have V_{HL} and V_{LH} switching points at 1.99 V and 1.01 V.

4.3.2 Fully Adjustable FII Schmitt Trigger

Passive resistors are undesirable components because they consume large silicon area and have wide parameter spread. The passive resistors used in Figure 4.20 can be replaced by active resistors, such as a MOS transistor operating in the linear region as shown in Figures 4.23.a, b and c. In all of these circuits the hysteresis width can be adjusted as function of an external bias voltage. The circuit shown in Figure 4.23.c was simulated with the bias voltage of mn_3 swept from 2 to 3 V in 0.25 V steps, while the bias voltage of mp_3 was swept from 2 to 0 V in -0.25 V steps as shown in Figure 4.22. The results show that the switching points of the Schmitt trigger change as a function of the external bias voltages.

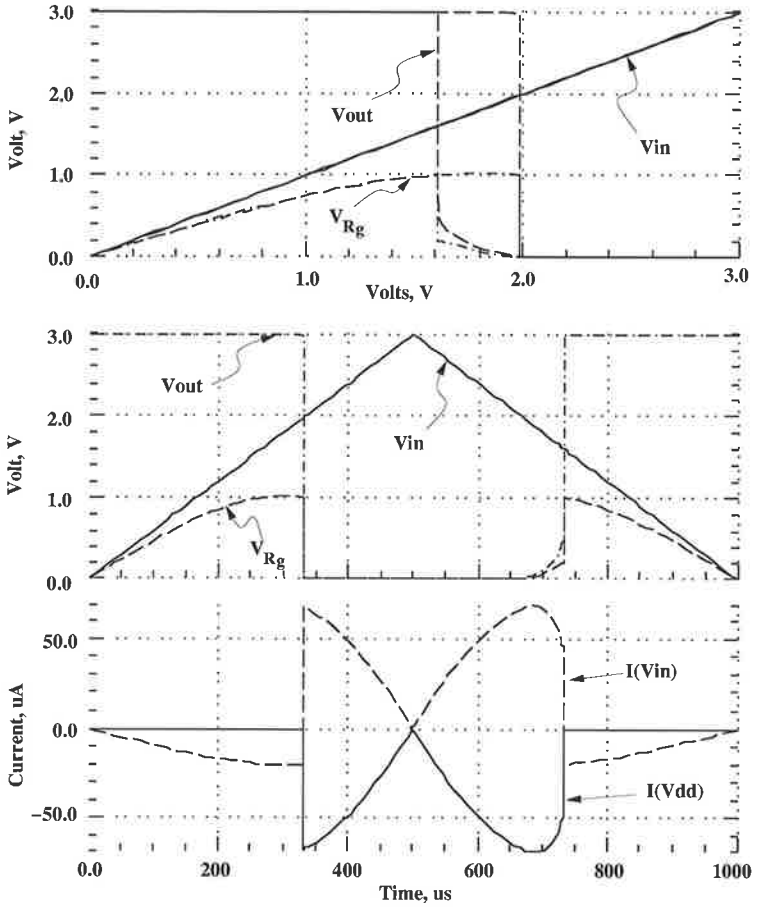


Figure 4.19. Simulation results of the Schmitt trigger circuit shown in Figure 4.17. The upper panel shows the input-output characteristics, the middle panel shows the input output signals as function of time, the lower panel the current drawn from power supply as function of the input signal in the time domain.

4.3.3 Self-Biased FII Schmitt Trigger

In some applications, it is desirable to fix the hysteresis width without the need for an external signal, i.e. a self-biased Schmitt trigger circuit. This can be achieved by connecting the bias voltage of mn_3 and mp_3 to V_{in}, as shown in Figures 4.24.a, b and c. Following the same analytical procedures used in the passive resistor case, the switching point for these configurations can be found. However, the switching points for these circuits can not be expressed in a simple analytical form. Hence, a numerical approach is used to show the circuits behaviour.

The simulation results for the circuit shown in Figure 4.23.c are presented in Figure 4.25. The simulation results show that the circuit exhibits a hysteresis width function

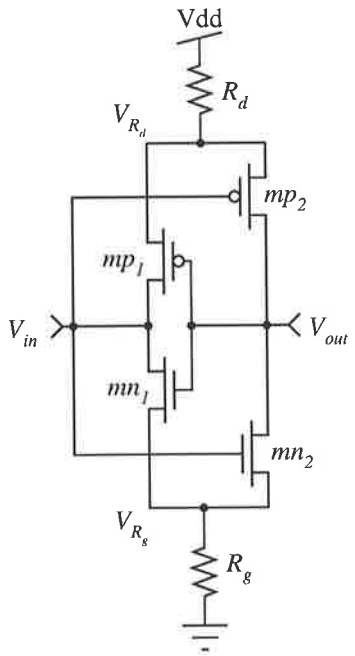


Figure 4.20. A schematic diagram of a fully symmetrical Schmitt trigger circuit with a finite input impedance. The R_d and R_g resistors are used to move the switching points of the bistable circuit away from V_{dd} and ground.

of the input signal with $V_{LH} = V_{dd}/3$ and $V_{HL} = 2\,V_{dd}/3$. These switching points can be controlled by sizing mn_3, mp_3, mn_1 and mp_1 at the design level. The first two transistors control the resistors' value, while the last two determine the current passing through these resistors as function of the input signal.

In summary, a number of Schmitt trigger circuits are designed by expanding on the idea of the digital latch circuit. Some of these circuits use passive resistors. These resistors are used to deliver the concept of the new Schmitt trigger circuit without the involvement of active resistors. As the use of passive resistors is not favoured in CMOS VLSI design because they consume large silicon area and have a wide parameter spread, MOS transistors biased in the linear region are used as active resistors. The integration of voltage controlled active resistors in the new Schmitt trigger circuits enabled the hysteresis adjustment through an external bias voltage. The operation of the complementary version shown in Figure 4.23.c was verified by simulation. As in some applications, it is desirable to fix the hysteresis width without the need for an external bias voltage. A third family of self-biased Schmitt trigger circuits was designed and their operation was also verified through simulation.

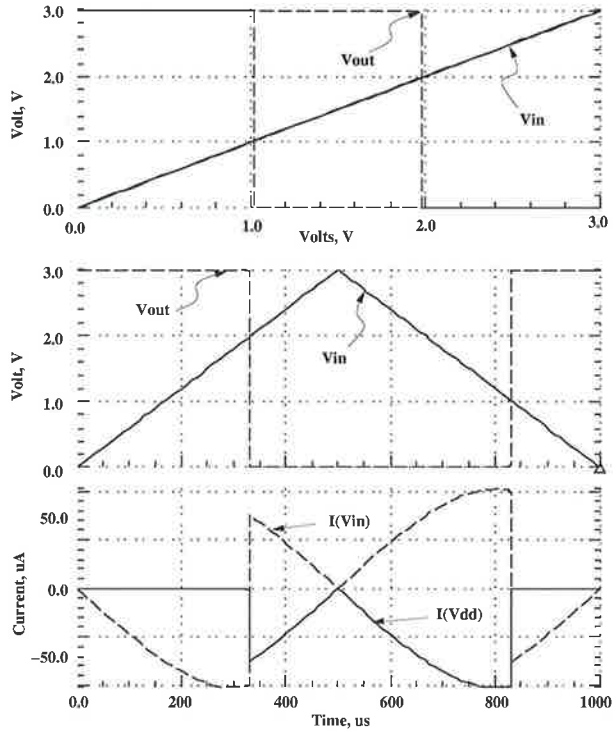


Figure 4.21. Simulation results of the Schmitt trigger circuit shown in Figure 4.20. The upper panel shows the input-output characteristics, the middle panel shows the input output signals as function of time, the lower panel the current drawn from power supply and the input current as function of the input signal in the time domain.

4.4 Experimental Work

As the prime interest of this research is circuit techniques that result in low power characteristics and small silicon area, the circuit shown in Figure 4.8 was chosen for fabrication. This circuit was fabricated in a 2 μm double poly, double metal standard p-well CMOS process through Orbit Semiconductor. A micro-photograph of the fabricated circuit is shown in Figure 4.26. The circuit layout contains another inverter added at the circuit output to drive an output pad. The measurements were conducted at 3 and 5 Volt supply voltages to see the hysteresis variation as function of the supply voltage as shown in Figures 4.29 and 4.30. The simulated characteristics using provided model parameters from the foundry are shown in Figures 4.27 and 4.28. Comparing the measured results to the simulation results listed in Table 4.2, it can be seen that there is a good agreement between the simulated and the measured characteristics with less than 3% difference between simulations and measurements.

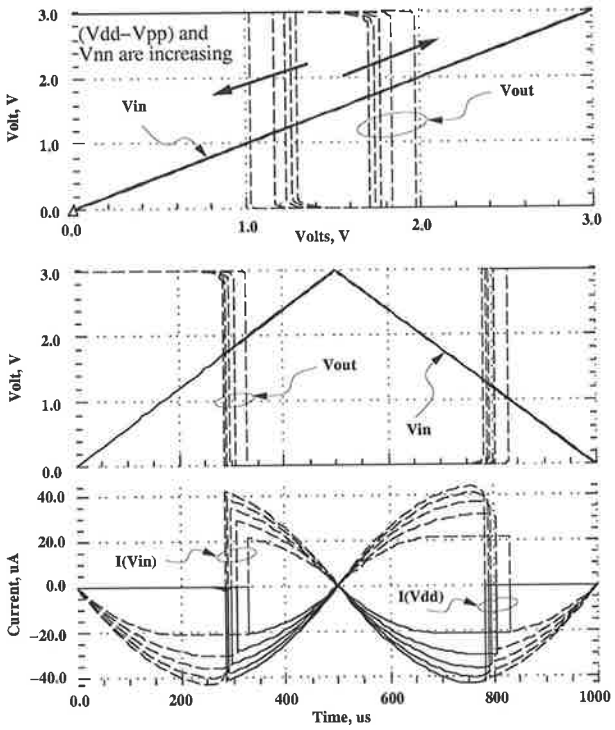


Figure 4.22. Simulation results of the Schmitt trigger circuit shown in Figure 4.23.c. The upper panel shows the input-output characteristics of the circuit, the middle panel shows the input output characteristics of the circuit as function of time, the lower panel shows the current drawn from power supply as function of the input signal in the time domain.

Table 4.2. Comparison between measured and simulated characteristics of the fabricated low power Schmitt trigger circuits. Comparison between measured and simulated characteristics of the fabricated low power Schmitt trigger circuit shown in Figure 4.8.

Description	Measured	Simulated	Error (%)
V_{LH}@3 V	0.80	0.78	2.5
V_{HL}@3 V	2.26	2.25	0.4
V_{HW}@3 V	1.46	1.47	-0.7
V_{LH}@5 V	1.55	1.50	3.3
V_{HL}@5 V	3.30	3.20	3.0
V_{HW}@5 V	1.75	1.70	2.9

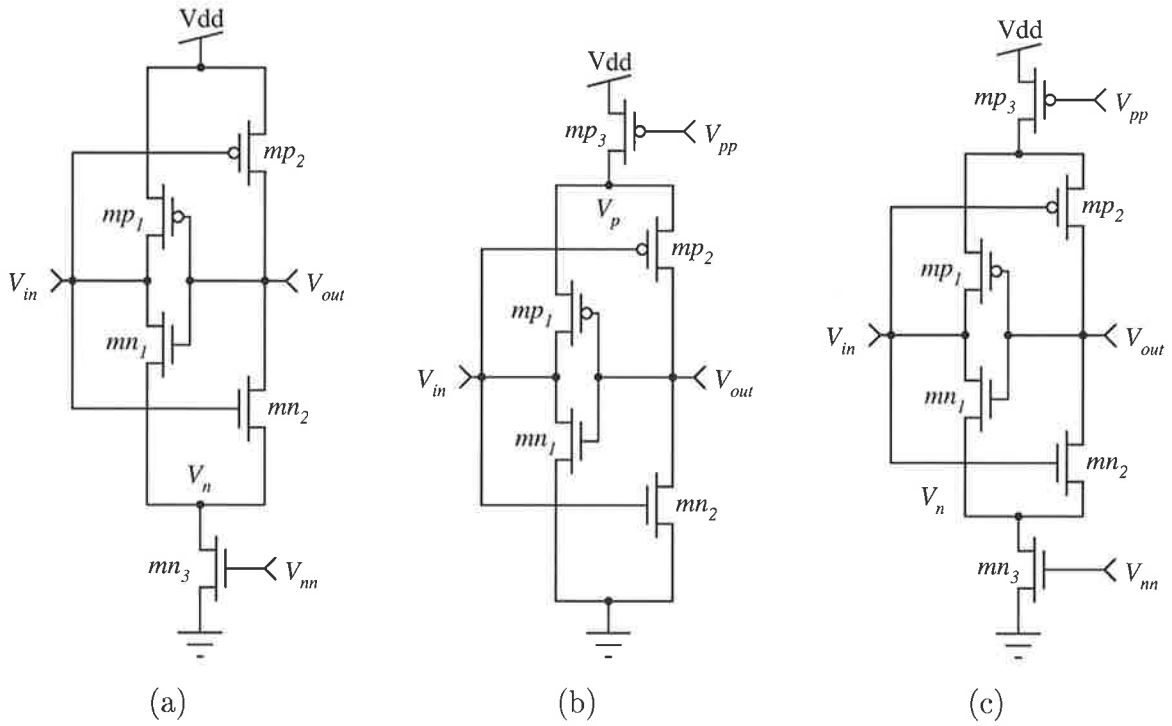


Figure 4.23. Three finite input impedance Schmitt trigger circuits. Three finite input impedance Schmitt trigger circuits with adjustable hysteresis using a MOS transistor biased in the linear region as an active resistor

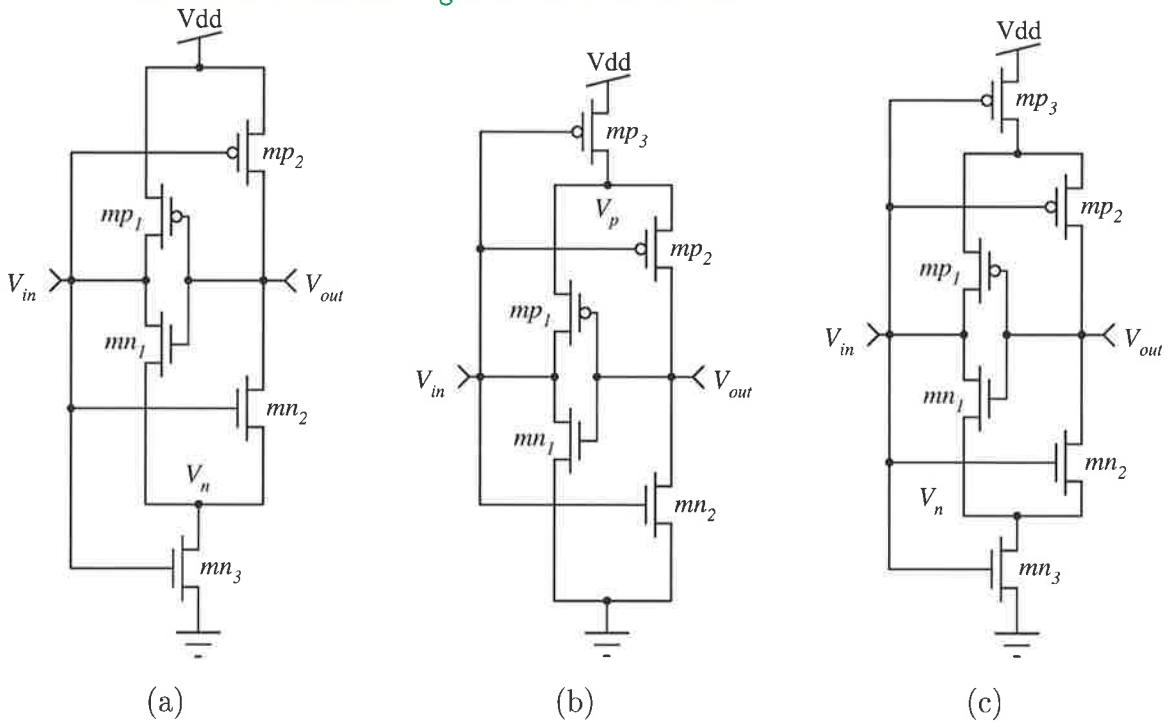


Figure 4.24. Three self-biased finite input impedance Schmitt trigger circuits. Three self-biased finite input impedance Schmitt trigger circuits with adjustable hysteresis using a MOS transistor biased in the linear region as an active resistor

4.5 Discussion

In this section the low power performance of the low power Schmitt trigger circuit shown in Figure 4.8 is compared with other Schmitt trigger circuits discussed in literature. Most of the CMOS Schmitt trigger circuits known to the author were simulated using fully symmetrical n and p MOS transistors. The Schmitt trigger circuits compared are: The IBM CMOS Schmitt trigger buffer [IBM 1986], the non-inverting regenerative CMOS logic circuit [Bundalo & Dokic 1985, Steyaert & Sansen 1986], the commonly known Schmitt trigger circuit [Dokic 1984] and the new waveform-reshaping circuit presented in [Kim *et al.* 1993]. The schematic circuit diagrams of these circuits are shown in Figures 4.31.a–d. Other Schmitt trigger circuits which use either bipolar technology, specially characterised devices, contain passive resistive elements or use operational amplifiers are not included in the comparison with the new Schmitt trigger circuit as these circuits are either not compatible with standard CMOS technology, require large silicon area or an external bias supply.

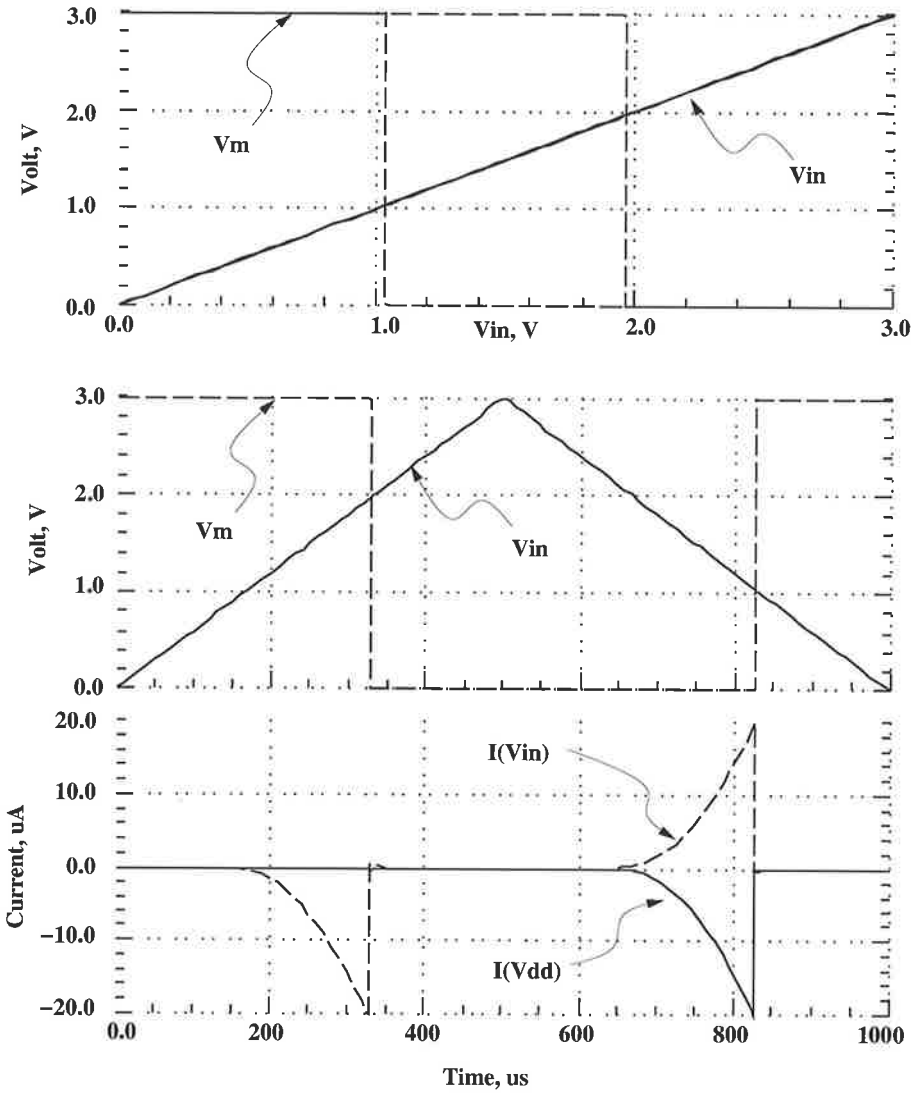


Figure 4.25. Simulation results of the self-biased Schmitt trigger circuit shown in Figure 4.24.c. The upper panel shows the input-output characteristics of the circuit, the middle shows the input-output characteristics as function of time, the lower panel the current drawn from power supply as function of the input signal in the time domain.

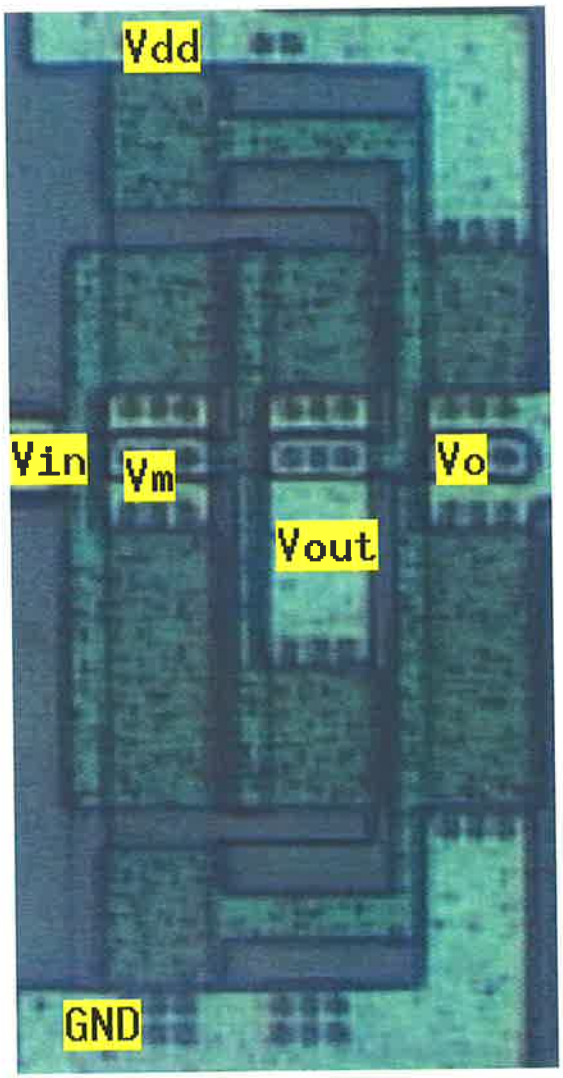
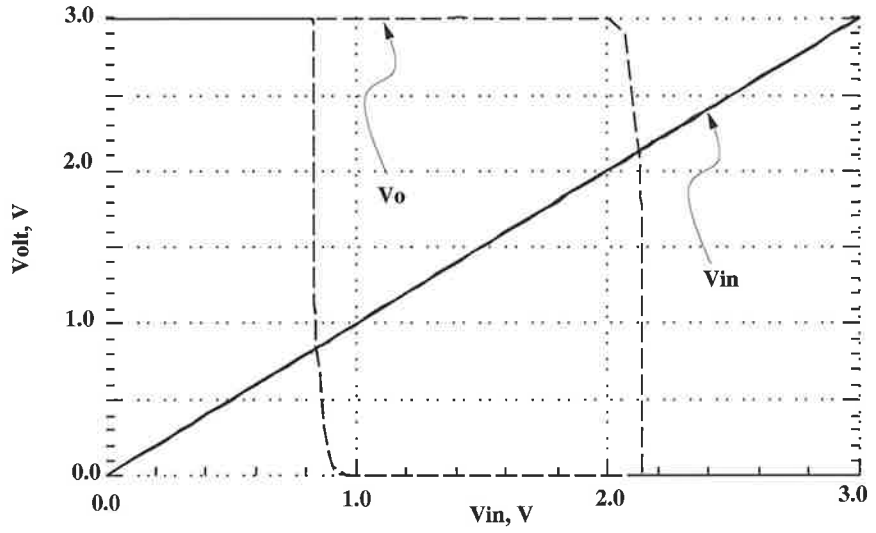
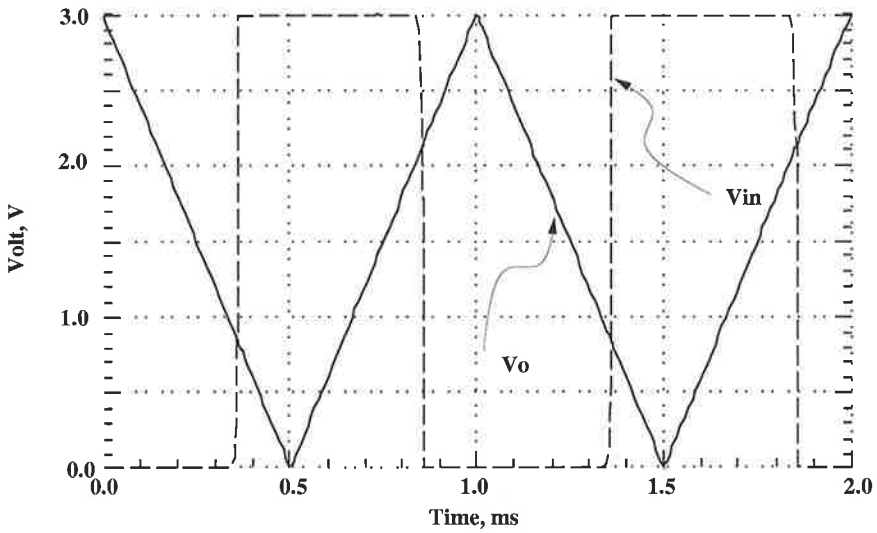


Figure 4.26. A micro-photograph of the fabricated Schmitt trigger circuit shown in Figure 4.8. The corresponding schematic is shown in Figure 4.8.

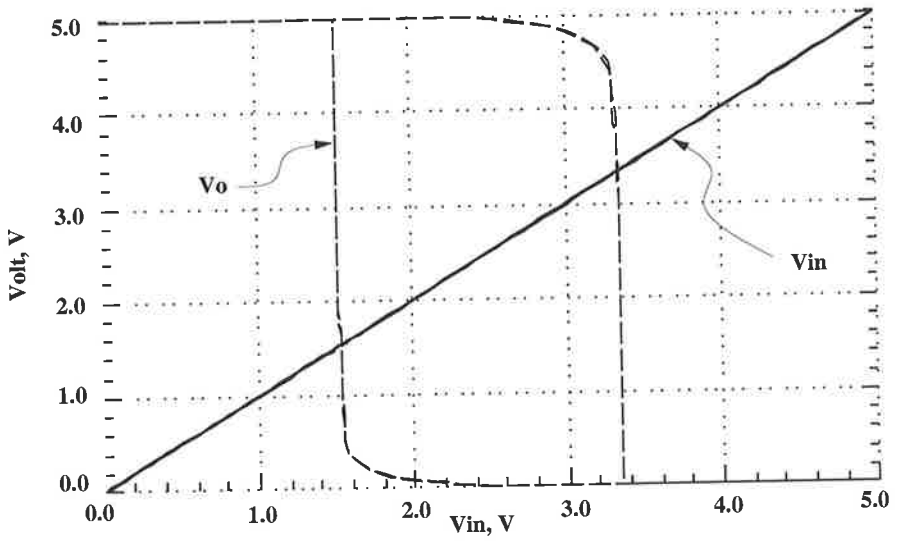


(a)

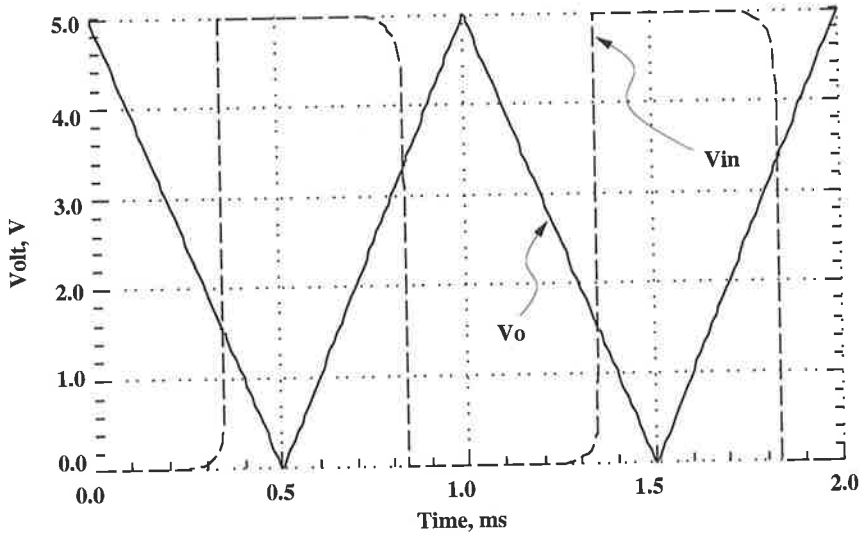


(b)

Figure 4.27. Simulation results of the fabricated Schmitt trigger circuit at 3 V. Simulation results of the fabricated Schmitt trigger circuit. (a) The simulated output characteristics of the fabricated Schmitt trigger circuit as of the input signal at 3 Volt supply, (b) the input output characteristics as function of time



(a)



(b)

Figure 4.28. Simulation results of the fabricated Schmitt trigger circuit at 5 V. Simulation results of the fabricated Schmitt trigger circuit. Panel (a) shows the output characteristics at 5 Volt supply, panel (b) shows the input-output characteristics as function of time.

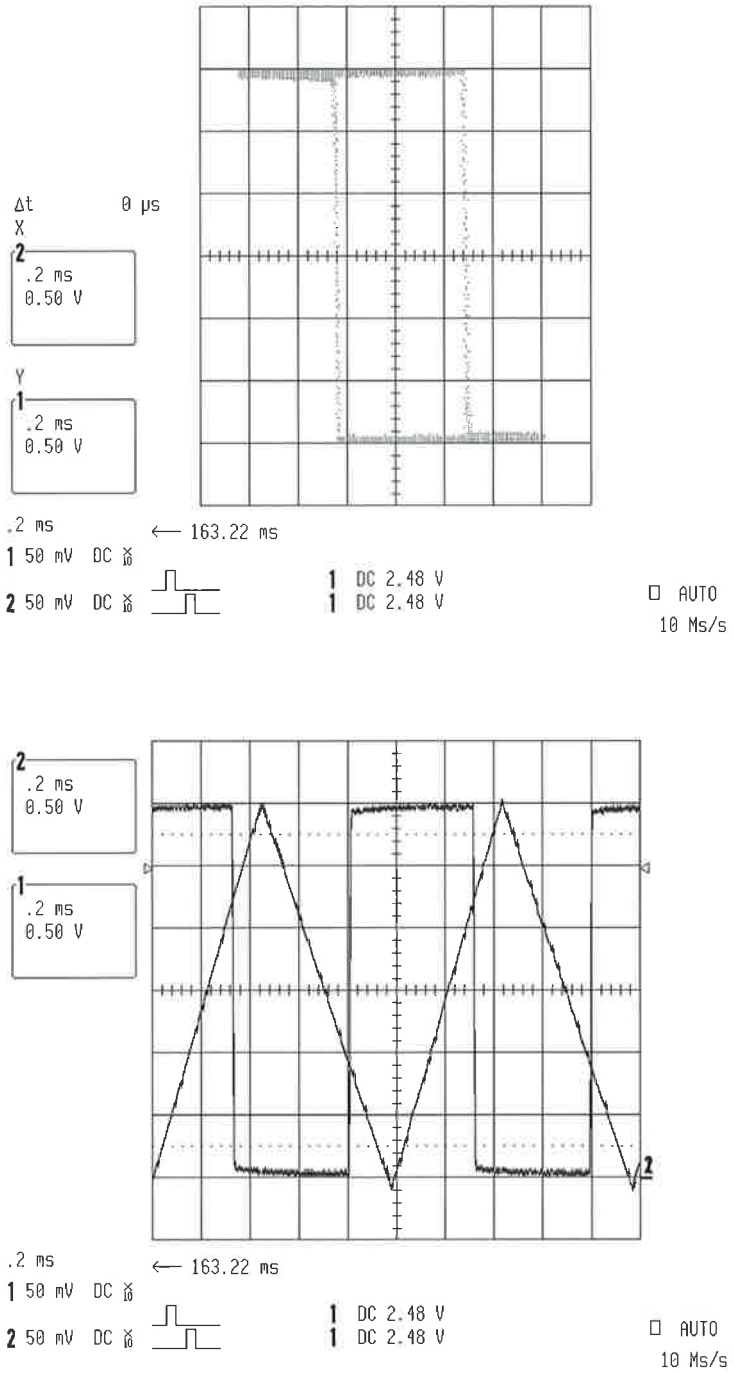
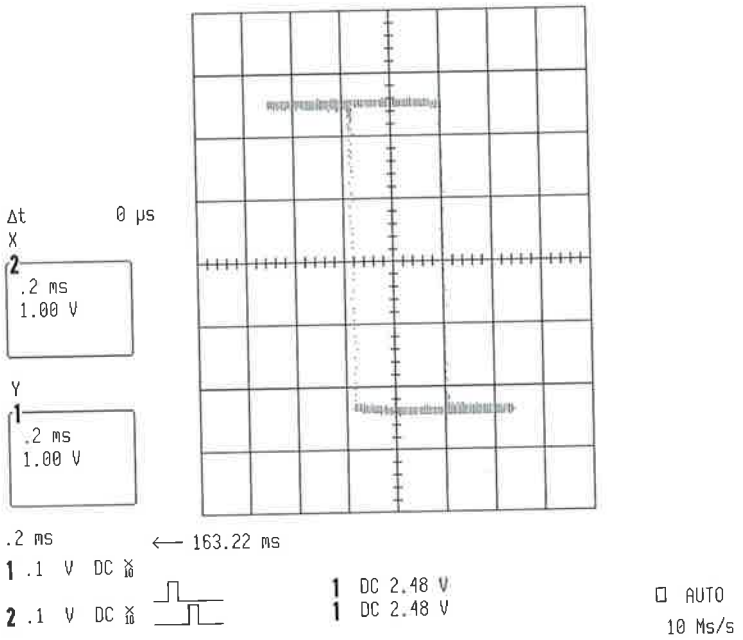


Figure 4.29. Measured characteristics of the fabricated Schmitt trigger circuit at 3 Volt supply. The upper panel shows measured output characteristics of the schmitt trigger circuit shown in Figure 4.26 as function of its input at 3 Volt supply, the lower panel shows the input-output characteristics as function of time (Screen dump from the LeCroy 9360 Oscilloscope).



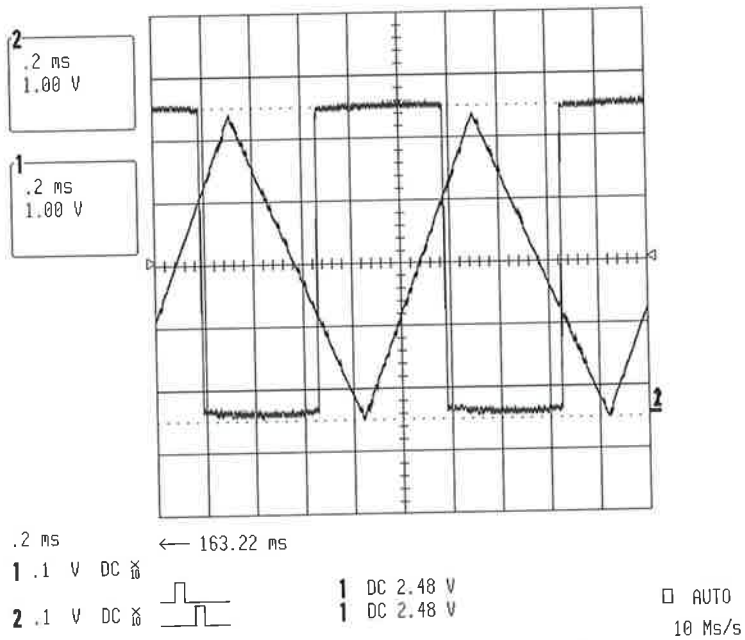


Figure 4.30. Measured characteristics of the fabricated Schmitt trigger circuit at 5 Volt supply. The upper panel shows the measured output characteristics of the Schmitt trigger circuit shown in Figure 4.26 as function of its input at 5 Volt supply, the lower panel shows the input-output characteristics of the circuit as function of time (Screen dump from the LeCroy 9360 Oscilloscope).

The simulation results of the input-output characteristics for: (a) the low power Schmitt trigger circuit presented Section 4.2.3, (b) the IBM Schmitt trigger buffer, (c) the commonly known Schmitt trigger circuit, (d) the non-inverting regenerative CMOS logic circuit and (e) the alternative approach to Schmitt trigger circuit, are shown in Figures 4.32 from top to bottom, respectively. The transistors sizes shown on the schematics were used in the simulations. Then, these circuits were simulated using a symmetrical 200 kHz saw tooth input signal with rail-to-rail amplitude. Figure 4.33 shows the current drawn from the power supply for the previous circuits in the same order mentioned earlier. The first observation about the simulation of the different Schmitt trigger circuits is that the output for some of them is complemented compared to the circuit proposed by Schmitt. The second observation is that some of these circuits do not provide a fully symmetrical hysteresis around $V_{dd}/2$, as is the case with the IBM Schmitt trigger buffer circuit. The third observation is related to the current drawn from the supply voltage, some of these Schmitt trigger circuits draw a considerable amount of current from the supply voltage when the input signal is either low or high. Comparing the low power performance of the low power Schmitt trigger circuit presented in this work with the Schmitt trigger circuits presented in the literature, it is evident from the simulations that the new low power Schmitt trigger circuit draws 5-6 times less current from the supply voltage compared to the best of the other Schmitt trigger circuits. Figure 4.34 shows the measured RMS power dissipation at different load capacitances for the different Schmitt trigger circuits using the previously mentioned input waveform. Another measurement of the power dissipation as function of the supply voltage was carried out to demonstrate the low power performance of the different Schmitt trigger as function of the supply voltage using the previous waveform and 5 Volt supply voltage, as shown in Figure 4.35. From the figure, it is clear that the new low power Schmitt trigger circuit has low power characteristics that supersede its counterparts by a factor of 10. However, because of the low power nature of the new Schmitt trigger circuit, its driving capability is limited by the output capacitance load.

4.6 Summary

In summary, two prototype Schmitt trigger circuits are discussed. The one discussed in Section 4.2 is of principal interest for its low power characteristics. The circuit discussed in Section 4.3 represents another approach to the design of Schmitt trigger circuits. As a result, two new families of Schmitt trigger circuits are developed based on the concept discussed in that section. The first family uses passive resistive elements, the second

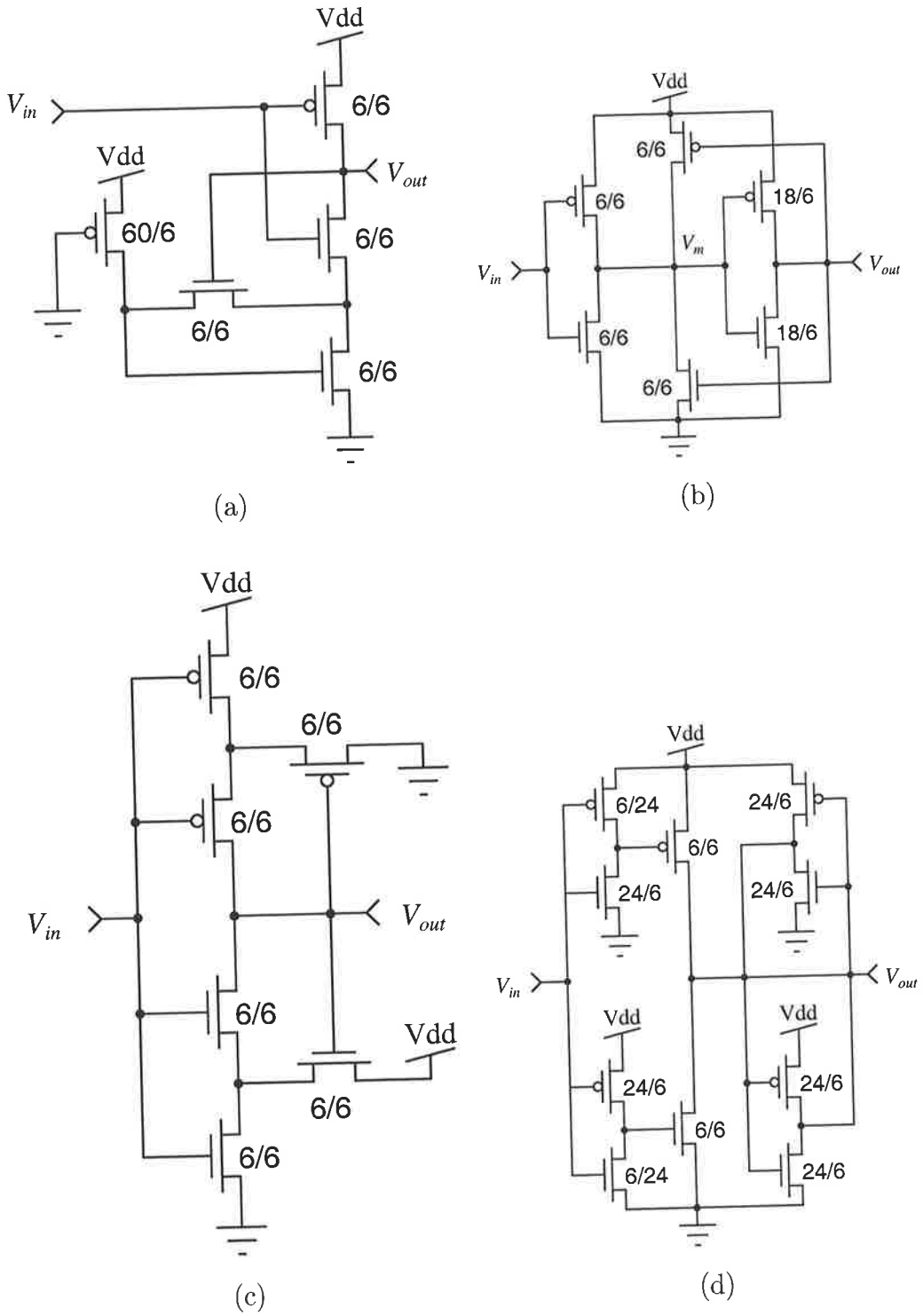


Figure 4.31. A collection of commonly used CMOS Schmitt trigger circuits in literature. A collection of commonly used CMOS Schmitt trigger circuits in literature. (a) The IBM CMOS Schmitt trigger buffer [IBM 1986], (b) the non-inverting regenerative CMOS logic circuit [Bundalo & Dokic 1985, Steyaert & Sansen 1986], (c) the commonly known Schmitt trigger circuit [Dokic 1984], (d) A new waveform-reshaping circuit as an alternative approach to Schmitt trigger [Kim *et al.* 1993].

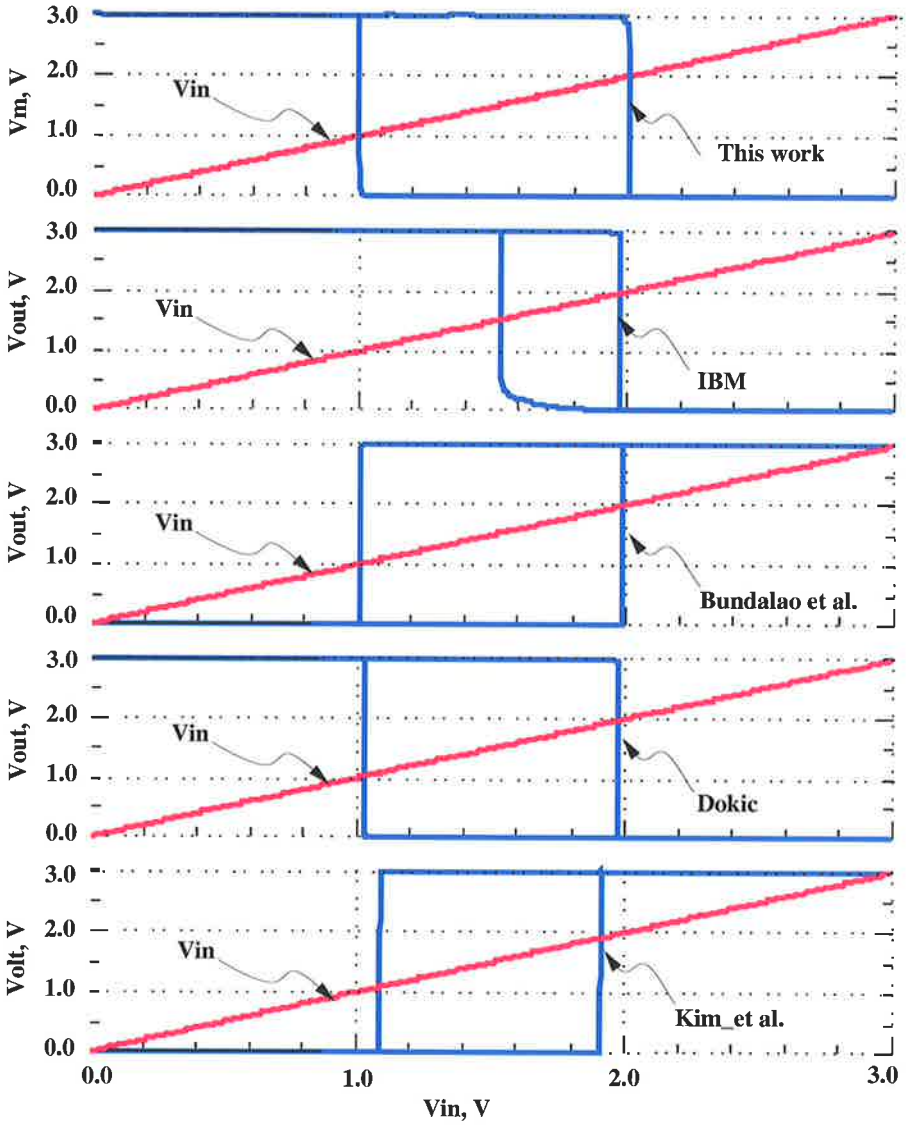


Figure 4.32. Simulated input-output characteristics of the common Schmitt trigger circuits. Simulated input-output characteristics of the common Schmitt trigger circuits from top to bottom: this work, the IBM CMOS Schmitt trigger buffer [IBM 1986], the non-inverting regenerative CMOS logic circuit [Bundalo & Dokic 1985, Steyaert & Sansen 1986], the commonly known Schmitt trigger circuit [Dokic 1984], the new waveform-reshaping circuit as an alternative approach to Schmitt trigger [Kim *et al.* 1993].

family uses active resistors to replace the passive resistors in the previous family, while the third is a self-biased Schmitt trigger circuit family. The second family has interesting features in the area of hysteresis controllability, while the third family, does not require an external bias when no hysteresis adjustment is needed. It is believed that the application of the finite input impedance Schmitt trigger circuits will be limited due to its finite input impedance, however, it is left to the designer to decide on this matter. Furthermore, comparing the low power Schmitt trigger circuit with other types of Schmitt trigger circuits presented in the literature shows that the new circuit based on the modulated conductance configuration has the best performance characteristics in terms of area, power and drivability of a capacitive load. The new Schmitt trigger thus presents a very attractive building block in low power mixed signal applications.

In the next chapter, low power reduction in mixed signal applications is targeted at the device and circuit levels. This is achieved by using a recently developed device called the Neuron-MOS transistor. The device structure consists of a MOS transistor with capacitively coupled inputs to its floating gates. Techniques using these devices in designing analog circuit modules with emphasis on area and power reduction are given.

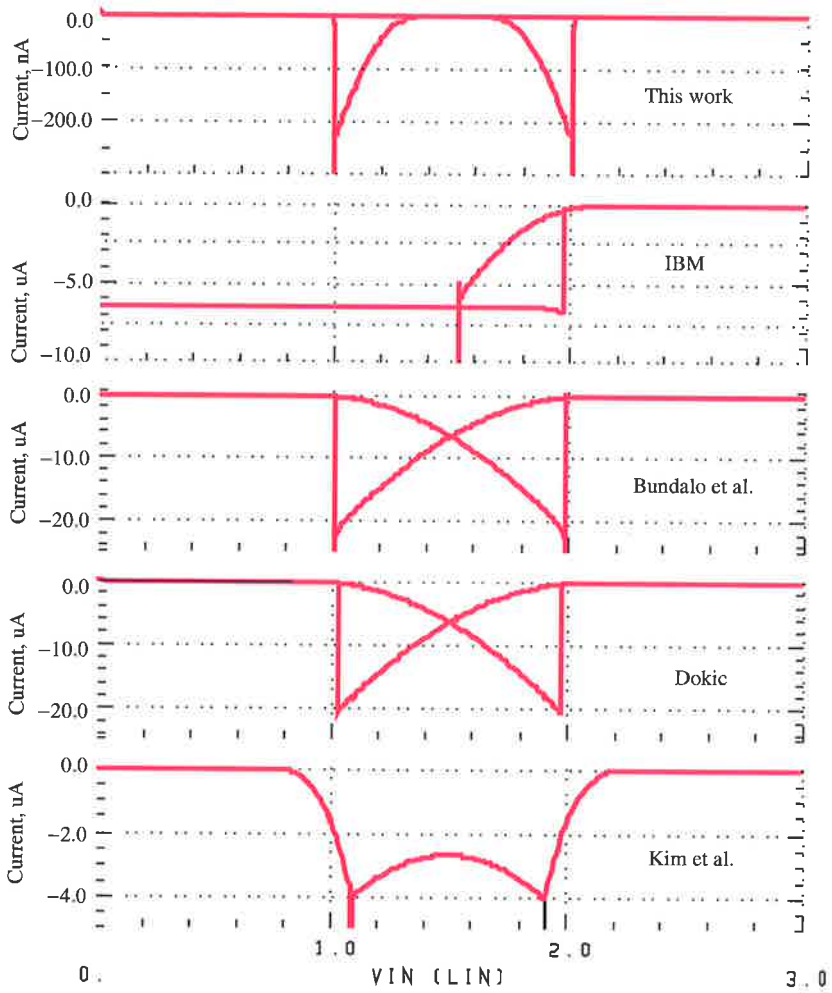


Figure 4.33. Simulated current drawn from the supply voltage as function of the input signal for the commonly known Schmitt trigger circuits. Simulated current drawn from the supply voltage as function of the input signal for the commonly used Schmitt trigger circuits from top to bottom: this work, the IBM CMOS Schmitt trigger buffer, the non-inverting regenerative CMOS logic circuit, the commonly known Schmitt trigger circuit, the new waveform-reshaping circuit as an alternative approach to Schmitt trigger.

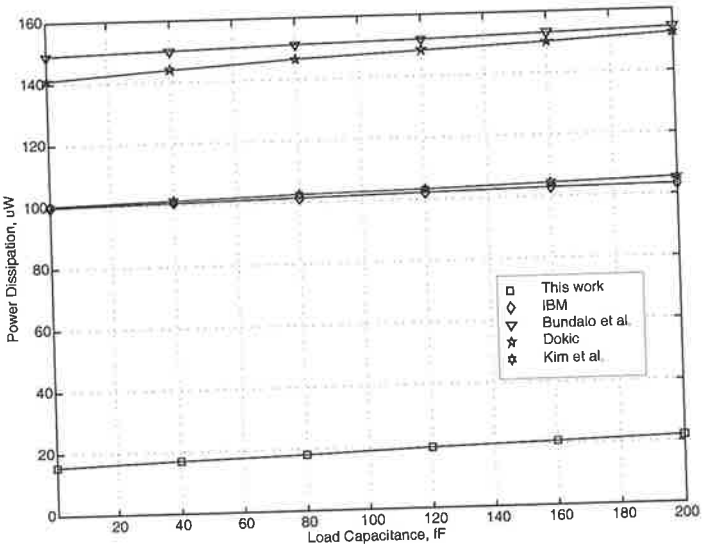


Figure 4.34. Measured RMS power dissipation from simulations for the commonly known Schmitt trigger types as function of a load capacitance. These simulations show that the performance of the low power Schmitt trigger circuit presented in this research supersede the other types of Schmitt trigger circuits and results in a power reduction by a factor of 5.

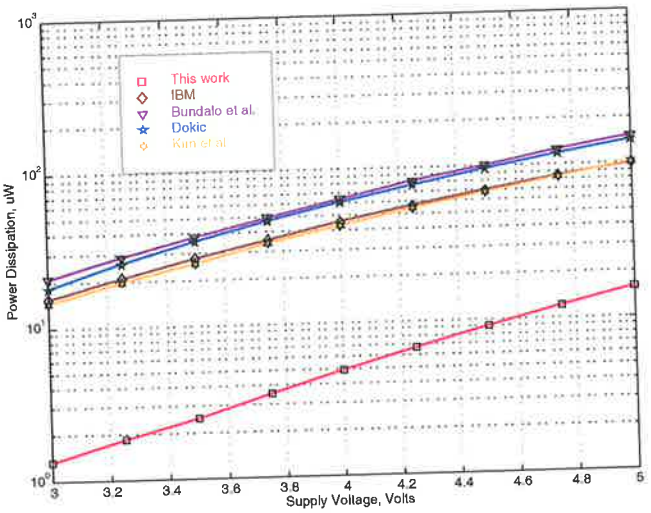


Figure 4.35. Measured RMS power dissipation from simulations for the commonly known Schmitt trigger circuits as function of the supply voltage. The simulations show that the presented Schmitt trigger circuit in this research have supersede the other types of Schmitt trigger circuits and results in a power reduction by also a factor of 10 as shown by the simulations.

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Chapter 5

Analog Circuit Design using Neuron MOS

IN the early 1990s, a new device that can evaluate the weighted sum of capacitively coupled inputs to a floating gate was proposed by Shibata and Ohmi. This device is referred to by the inventors as *neuron MOS* or *νMOS* in short. It was given this name because it mimics the operation of a neuron. The device has been extensively used in digital circuit design and resulted in low-power area efficient designs. The use of this device in mixed mode analog-digital design was given very little attention in the literature. In this chapter, we present a model for the device and demonstrate how this device can be used in designing basic analog building blocks in standard CMOS technology. The presented circuits have characteristics as a function of capacitor ratios and consume very small area. Resulting designs are portable between different processes with minimal amount of effort.

5.1 Introduction

The neuron MOS transistor is a functional device that has been proposed recently by Shibata & Ohmi [1991] based on the MOSFET. The device works more intelligently than a mere switching device because it evaluates the weighted sum of all input signals at the gate level, and controls the 'ON' and 'OFF' of the transistor based on the result of the weighted sum operation [Shibata & Ohmi 1992a]. The behaviour of the transistor resembles very well that of a biological neuron, with the turn-on of the transistor being analogous to the firing of a neuron. In this respect, the device inventors called it a neuron-MOSFET or nu-MOS (νMOS) in short. νMOS circuits operate with mixed mode analog/digital functions and can even perform Boolean logical operations that are dynamically reconfigurable. The use of νMOS circuits can greatly increase functionality/per unit area [Hirose & Yasuura 1996] while still maintaining low cost via the use of standard CMOS fabrication. In addition to neural networks [Rantala, Franssila, Kaski, Lampinen, Aberg & Kuivalainen 2001], the application areas of νMOS have included digital arithmetic units [Celinski *et al.* 2000], analog-to-digital and digital-to-analog converters [Rantala, Kuivalainen & Aberg 2001], smart sensors, motion detectors, monolithic imaging/compression and optical neural arrays [Lange *et al.* 1994].

So far, most of the circuits designed using these transistors use digital input signals to achieve certain functions [Shibata & Ohmi 1993, Kosaka *et al.* 1995, Ohmi & Shibata 1994, Ishii *et al.* 1992, Weber *et al.* 1996, Shibata & Ohmi 1992b]. However, a few researchers have used νMOS in analog circuit design [Al-Sarawi *et al.* 1997, Yang & Andreou 1994]. It can be seen that such a device can play an important role in the design of analog circuitry with small area and with low power potential, because all the input signals are capacitively coupled to the νMOS floating gate. In contrast to switched capacitor circuits that deal with discrete time signals, Neuron MOS circuits provide continuous time circuits with characteristics as a function of capacitor ratios, without requiring control signals.

Section 5.2 of this chapter provides a detailed derivation of the neuron-MOS transistor model. Section 5.3 emphasises some of the main key design parameters used in the design of both analog and digital circuitry. Section 5.4 discusses new analog circuits that have been designed using νMOS. Section 5.5 discusses some techniques to reduce the power dissipation for some of the designed modules in Section 5.4, while Section 5.6 presents experimental work for some of the circuits designed in Section 5.4.

5.2 General Model Derivation of the νMOS Transistor

A general model for neuron-MOS transistor is derived. This model includes all the terminal capacitances, namely the drain (D), source (S) and inputs (V_i). To simplify the derivation, the following are assumed:

- no charge injection occurs during device operation;
- all voltages are measured with respect to the ground.

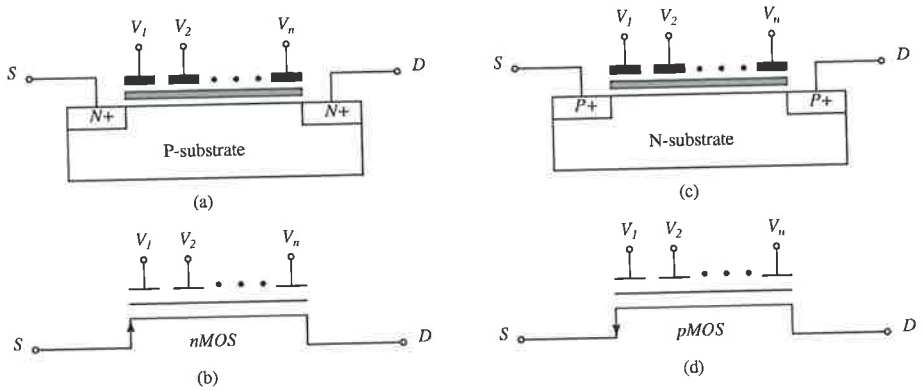


Figure 5.1. The basic structure and symbol of νMOS transistor. Subfigure (a) shows the basic structure of the n type νMOS transistor and illustrates how the input are capacitively coupled to the floating gate. Subfigure (b) shows the commonly used symbol for the n type νMOS in the literature. Subfigures (c) and (d) shows the corresponding p type νMOS transistor. This symbol is used in this thesis.

The structure of the νMOS transistor is similar to the structure of the normal MOS transistor but with the input gate capacitively coupled to a number of inputs as shown in Figure 5.1. So, the MOS transistor equivalent circuit can be employed to generate an *equivalent circuit for νMOS* as shown in Figure 5.2.a and simplified in Figure 5.2.b. From these figures the total charge on the floating gate, Q_F, can be calculated as

$$\begin{aligned} Q_F &= C_{gs}(\phi_F - V_s) + C_{gd}(\phi_F - V_d) \\ &\quad + C_{gate}(\phi_F - (\psi_s + \phi)) + \sum_{i=1}^{n} C_i(\phi_F - V_i) \end{aligned} \tag{5.1}$$

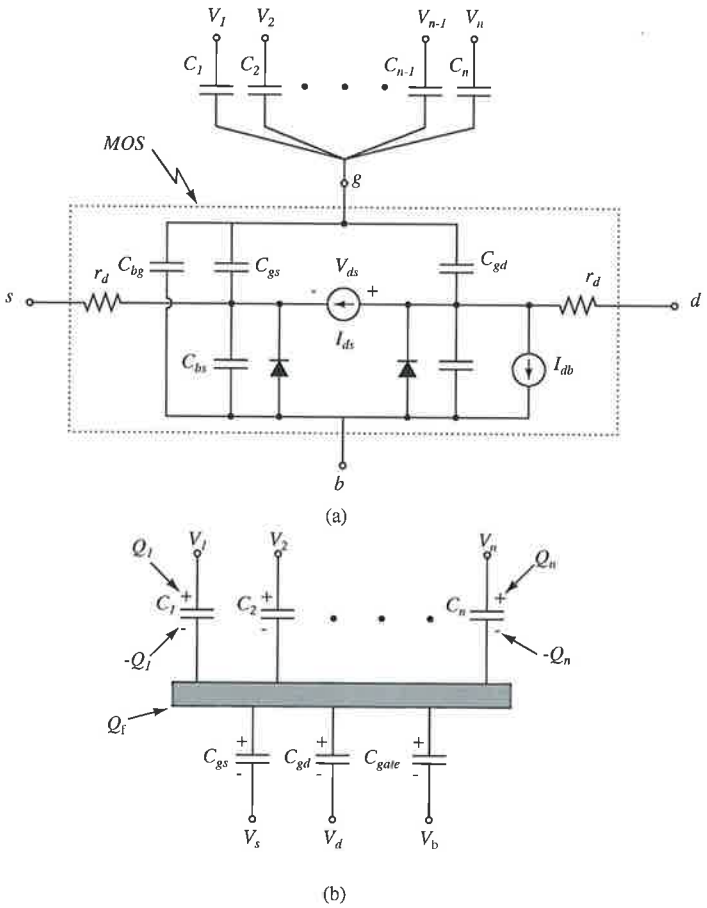


Figure 5.2. Equivalent circuit and capacitance representation of νMOS transistor. Subfigure (a) shows the equivalent circuit of the νMOS transistor and shows all the parasitics from the floating gate to source, drain and substrate. Subfigure (b) shows the capacitance representation of the νMOS transistor and shows the charge distribution on these capacitances.

where

C_{gd}	Floating gate to drain capacitance, F;
$C_1, \ldots, C_n$	Coupling capacitor between the floating gate and each of the input gates, F;
Q_F	Charge on the Floating gate, C;
V_d	Drain voltage, V;
V_s	Source voltage, V;
$V_1, \ldots, V_n$	Input signal voltages, V;
ψ_s	Surface potential for channel, V;
ϕ	Flat band voltage, V.
C_{gate}	Floating gate to channel surface capacitance, F.

Writing Equation 5.1 in terms of the *floating gate voltage*, ϕ_F, results in

$$\phi_F = \frac{C_{gs}V_s + C_{gd}V_d + C_{gate}(\psi_s + \phi) + \sum_{i=1}^{n} C_i V_i + Q_F}{C_{gs} + C_{gd} + C_{gate} + \sum_{i=1}^{n} C_i}. \tag{5.2}$$

Equation 5.2 can be simplified by letting $C_T = \sum_{i=0}^{n} C_i$, where $C_0 = C_{gs} + C_{gd} + C_{gate}$, and $\triangle\phi_F = C_{gs}V_s + C_{gd}V_d + C_{gate}(\psi_s + \phi)$ as follows

$$\phi_F = \frac{\triangle\phi_F + Q_F + \sum_{i=1}^{n} C_i V_i}{C_T}. \tag{5.3}$$

The above equation represents a *general model for the neuron-MOS* transistor with all of its terminal capacitances. The inclusion of all terminal capacitances in the general model may not be very significant for digital circuit design. However, it is significant when designing analog circuits because they can provide a feedback mechanism, which can, depending on the circuit under consideration, cause a shift in the floating gate potential.

The model given by Equation 5.3 can be simplified to give the simplified model given in [Shibata & Ohmi 1992a, Choi & Sheu 1994] by assuming that: (i) the initial charge on the floating gate equals zero, $Q_F = 0$; (ii) the source and the back-gate are connected together, $V_S = V_D = 0$, and (iii) $\sum_{i=1}^{n} C_i V_i \gg \triangle\phi_F$, resulting in

$$\phi_F = \frac{\sum_{i=1}^{n} C_i V_i}{C_T}. \tag{5.4}$$

5.3 Key Design Parameters for νMOS Transistor

This section identifies some of the main key design parameters that are used in designing analog and digital circuitry based on the general model developed in the previous section.

5.3.1 Floating-Gate Gain Factor

The first design parameter to be considered is the *floating-gate gain factor*, γ_g, which is defined as

$$\gamma_g = \frac{C_1 + C_2 + \ldots + C_n}{C_T} = \frac{C_T - C_0}{C_T}. \tag{5.5}$$

The product of γ_g and V_{dd} represents the maximum floating-gate voltage obtained when all input gates are at V_{dd}. In the above equation C_0 can vary depending on the

operating condition of the transistor. However, it can be approximated by the gate oxide capacitance when the device is 'ON' and can be regarded as a constant as long as the channel is formed [Embabi *et al.* 1993, Shibata & Ohmi 1992a]. The value of γ_g can be maximised by increasing the ratio of $\sum_{i=1}^{n} C_i$ to C_0. Hence, a trade-off between circuit area and the needed floating-gate gain factor needs to be decided. From experience, a floating-gate gain factor of 0.9 and more was found good enough for digital circuit design. However, the γ_g factor for analog circuits depends on the circuit functionality.

5.3.2 Threshold Voltage Seen from the Floating Gate

The second key design parameter is the threshold voltage seen from the floating gate V_{TH}^*, which is the threshold voltage of the transistor seen from the floating gate. V_{TH}^* represents the boundary between the 'ON' and 'OFF' states of the transistor. So, for the transistor to turn 'ON', $\phi_F > V_{TH}^*$, i.e.

$$\frac{C_1V_1 + C_2V_2 + \ldots + C_nV_n}{C_T} > V_{TH}^* \tag{5.6}$$

Equation 5.6 states that *when the linear weighted sum of all the input signals exceeds a certain threshold value V_{TH}^*, the transistor turns 'ON'*. V_{TH}^* is one of the main design parameters of the νMOS transistor.

5.3.3 Floating Gate Offset Voltage

Two separate effects can cause a shift in the floating gate voltage. The first is due to an initial charge on the floating gate that is trapped in the floating gate during the fabrication process. The magnitude of such a shift can be as large as 1 to 2 Volts [Luck *et al.* 2000]. A number of methods can be used to reduce this effect. The first is to shine an UV light on the transistor while all terminals are grounded. This will excite some electrons to energy states above the conduction band of the oxide layer, resulting in an increase in the oxide layer conductance, allowing the discharge of the floating gate until its potential is the same as ground [Yang & Andreou 1994, Shibata & Ohmi 1992a]. The second method is to inject some charge carriers into the floating gate, i.e. programming the floating gate using Fowler-Nordheim tunnelling effect [Thomsen & Brooke 1994]. The third method is to electronically initialise the floating gate charge by connecting the floating gate to a predefined voltage. Such a method is used in [Shibata *et al.* 1996, Ohmi & Shibata 1995, Kotani *et al.* 1995]. As can be deduced from Equation 5.2, another method to cancel the initial charge on the floating gate is to adjust the source voltage

of the neuron-MOS transistor. However, such adjustment will affect the neuron-MOS transconductance, g_m.

The second effect that might cause a shift in the floating gate potential is the gate to drain capacitance, C_{gd}, which will have an effect mainly in the linear region [Embabi *et al.* 1993]. The effect of such capacitance can be reduced by using minimum size transistors, careful layout design and maximising the ratio of $\sum_{i=1}^{n} C_i V_i$ to $\triangle\phi_F$.

5.4 Analog Circuit Design using νMOS Transistor

In the following subsection, techniques to design analog circuitry using νMOS transistor are discussed.

5.4.1 A Linear Grounded Resistor

Normally, an active resistor with a moderate resistance value can be implemented by using a MOS transistor with its gate connected to its drain, such configuration is referred to as a diode connected MOS transistor. Another technique is to bias the MOS transistor in the linear region of operation. However, in both of these cases the active resistor suffers from non-linearity because the transistor drain current is proportional to square of the drain voltage. Such non-linearity can be linearised by using a dual input νMOS transistor with one of the inputs connected to drain and the other to a programming input voltage [Shibata & Ohmi 1992a], as shown in Figure 5.3. The I-V characteristics of such a configuration when the νMOS transistor is operating in the triode region is given by

$$I_d = \beta \left[(\frac{C_{in}}{C_T} V_{in} - V_{TH}^*) V_d + (\frac{C_d}{C_T} - \frac{1}{2}) V_d^2 \right], \tag{5.7}$$

where I_d is the drain current, V_{TH}^* is the threshold voltage of the transistor seen from the floating gate, V_d is the drain voltage of the νMOS transistor, $\frac{C_d}{C_T}$ and $\frac{C_{in}}{C_T}$ are the coupling coefficients from the drain and input to the floating gate, respectively. From Equation 5.7, the dependency of I_d on V_d^2 can be reduce by letting $\frac{C_d}{C_T} = \frac{1}{2}$. The simulation results of this resistor, with V_{in} increased from 1 to 5 V in 0.4 V steps, while V_d was swept from 0 to 5 V for every increment in V_{in}, are shown in Figure 5.4.

This circuit was discussed in [Shibata & Ohmi 1992a] and is re-discussed here because it represents a good basic analog building block and because of its relevance to the controlled gain amplifier circuit, which will be discussed in Section 5.4.2.

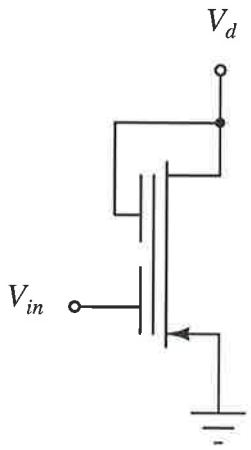


Figure 5.3. Grounded active resistor design based on νMOS transistor. The value of the grounded resistor is function of the coupling capacitor from V_d to the floating gate and the coupling capacitor from V_{in} to the floating gate.

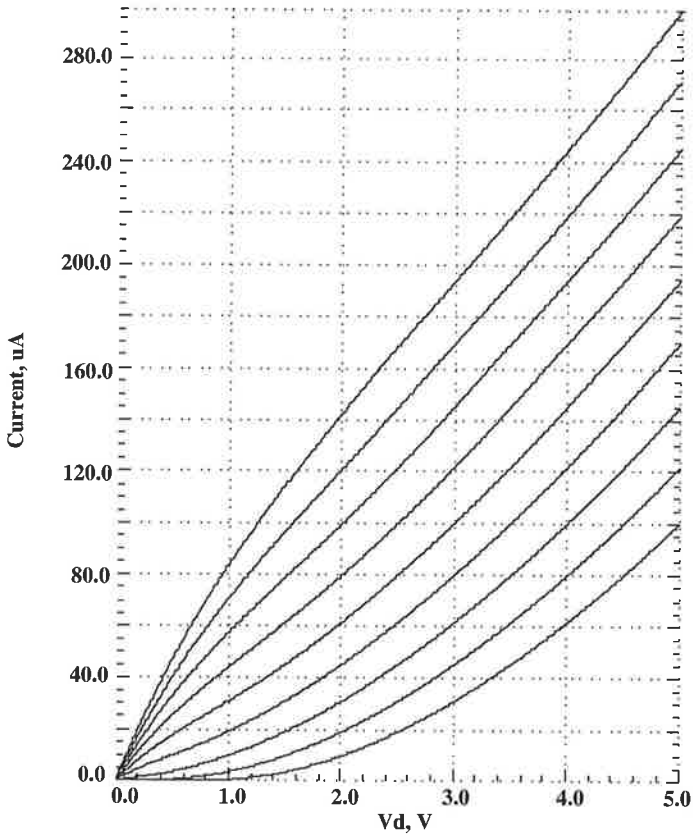


Figure 5.4. Neuron-grounded resistor simulation. These simulations were conducted with $C_{in} = C_d$, and the input voltage, V_{in}, was swept from 1 to 5 V in 0.5 V steps. These simulations show that the value of the resistor can be tuned as function of the V_{in} over a wide dynamic range and maintain good linearity.

5.4.2 Controlled Gain Amplifiers

This section discusses the design of a new *controlled gain amplifier* using νMOS transistors, where the gain of the amplifier is controlled through capacitor ratios instead of transistor size ratios. The amplifier design is based on the linear grounded resistor discussed in Section 5.4.1. Later in this subsection, another approach to the amplifier design using a '*neuron-inverter*' (νCMOS inverter) is also discussed.

The first approach is to use two grounded resistors, one using n-νMOS, while the other using p-νMOS and connect them as shown in Figure 5.5. The gain of the amplifier circuit can be found analytically by writing the current equations of the n- and p-νMOS transistors as follows

$$I_n = \frac{\beta_n}{2}(W_{in_n}V_{in} + W_{o_n} + V_{gg} - V_{t_n})^2 \tag{5.8}$$

$$I_p = \frac{\beta_p}{2}(V_{dd} - W_{in_p}V_{in} - W_{o_p}V_o - V_{gg} + V_{t_p})^2 \tag{5.9}$$

where

I_n, I_p are the drain currents of the n- and p-MOS transistors, respectively;

W_{in_i} is the ratio of the input coupling capacitance of transistor type i, C_{in_i}, to the total capacitances at the floating gate of that transistor, C_{T_i}. i.e. $W_{in_n} = \frac{C_{in_n}}{C_{T_n}}$ and $W_{in_p} = \frac{C_{in_p}}{C_{T_p}}$;

W_{o_i} is ratio of the output to input coupling capacitance of transistor type i, C_{o_i}, to the total capacitance at the floating gate of that transistor, C_{T_i}. i.e. $W_{o_n} = \frac{C_{o_n}}{C_{T_n}}$ and $W_{o_p} = \frac{C_{o_p}}{C_{T_p}}$;

V_o is the output voltage of the amplifier;

V_{gg} is the initial voltage at the floating gate;

V_{t_i} is the threshold voltages of transistor type i.

Solving Equations 5.8 and 5.9 for V_o results in

$$V_o = -\frac{\sqrt{\frac{\beta_n}{\beta_p}}W_{in_n} + W_{in_p}}{\sqrt{\frac{\beta_n}{\beta_p}}W_{o_n} + W_{o_p}}V_{in} - \frac{\sqrt{\frac{\beta_n}{\beta_p}} + 1}{\sqrt{\frac{\beta_n}{\beta_p}}W_{o_n} + W_{o_p}}V_{gg} + \frac{V_{dd} + V_{t_n}\sqrt{\frac{\beta_n}{\beta_p}} + V_{t_p}}{\sqrt{\frac{\beta_n}{\beta_p}}W_{o_n} + W_{o_p}}. \tag{5.10}$$

Equation 5.10 can be simplified by letting $\beta_n = \beta_p$, $V_{t_n} = |V_{t_p}|$, $W_{in} = W_{in_p} = W_{in_n}/2$, $W_{o_n} = W_{o_p} = W_o/2$ and $V_{gg} = V_{dd}/2$, to

$$V_o = -\frac{C_{in}}{C_o}V_{in}. \tag{5.11}$$

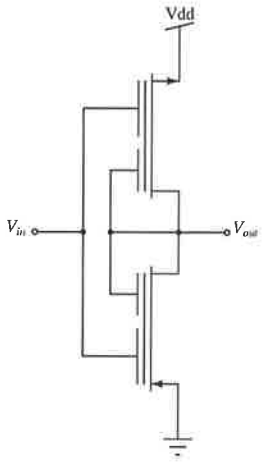


Figure 5.5. A controlled gain amplifier circuit designed using linear grounded resistors. This amplifier structure uses two complementary νMOS transistors with feedback from the output of the amplifier to each input of the n and p νMOS device. The gain of this amplifier is purely a function of the ratio of the input coupling capacitor to the feedback coupling capacitor. The difference in between the βs of the n and pMOS transistors used in the νMOS implementation was compensated for to have an operating point around $V_{dd}/2$.

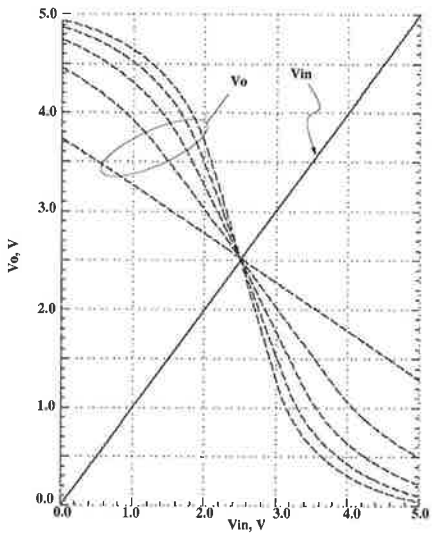


Figure 5.6. The simulation results of the controlled gain amplifier circuit which uses νMOS transistors. These simulations show the relationship between the output voltage, V_o and the input voltage, V_{in}. They were conducted using a 10 pF coupling capacitor from the amplifier output to the input of each νMOS device, then the input coupling capacitance for each νMOS device was swept from 5 pF to 25 pF in 5 pF steps. The simulations show that the gain of the amplifier is 1/2, 1, 2, 3, 4 and 5 for the corresponding input capacitances of 5 pF, 10 pF, 15 pF, 20 pF and 25 pF, respectively.

The above equation shows that the amplifier gain is purely function of a capacitor ratio and it is independent of process parameters. To confirm Equation 5.11, the amplifier circuit was simulated with $C_o = 10$ pF while C_{in} was swept from 5 pF to 25 pF in 5 pF steps. The simulation results are shown in Figure 5.6.

The second approach to the design of a controlled gain amplifier is to use the '*νCMOS inverter*,' which is simply an inverter that uses νMOS transistors, as shown in Figure 5.7. For the amplifier design a dual input gate 'neuron-inverter' is used with one of the inputs connected to the output terminal, while the other is used as an input terminal, as shown in Figure 5.8. Once such a connection is made, the functionality of the circuit is completely different from the 'neuron-inverter,' as in the case the 'neuron-inverter' the output signal is a digital state of either '1' or '0,' while with new connection the circuit will act as an amplifier with a continuous output signal as function of the input signal, as will be seen in the following analysis.

The gain of the amplifier can be calculated by writing the current equations of the p-νMOS and n-νMOS transistors using simple transistors model in the saturation region as follows

$$I_n = \frac{\beta_n}{2}(W_{in}V_{in} + W_oV_o + V_{gg} - V_{t_n})^2 \tag{5.12}$$

$$I_p = \frac{\beta_n}{2}(V_{dd} - W_{in}V_{in} - W_oV_o - V_{gg} + V_{t_p})^2, \tag{5.13}$$

where

W_{in} is the ratio of the input coupling capacitance, C_{in}, to the total capacitance, C_T;

W_o is the ratio of the output to input coupling capacitance, C_o, to the total capacitance, C_T.

Solving Equations 5.12 and 5.13 for V_o gives

$$V_o = -\frac{W_{in}}{W_o}V_{in} - \frac{V_{gg}}{W_o} + \frac{V_{dd} + V_{t_n}\sqrt{\frac{\beta_n}{\beta_p}} + V_{t_p}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}. \tag{5.14}$$

The above equation can be simplified by letting $\beta_n = \beta_p$, $V_{t_n} = |V_{t_p}|$ and $V_{gg} = V_{dd}/2$, to give

$$V_o = -\frac{C_{in}}{C_o}V_{in}. \tag{5.15}$$

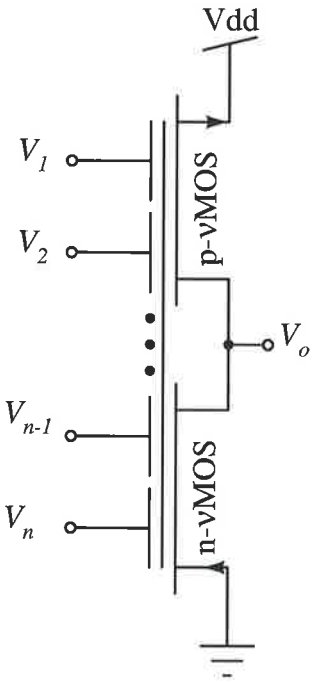


Figure 5.7. A schematic circuit diagram of a 'neuron-inverter.' The diagram shows the input coupling capacitors to the common floating gate of the n and p-νMOS transistors.

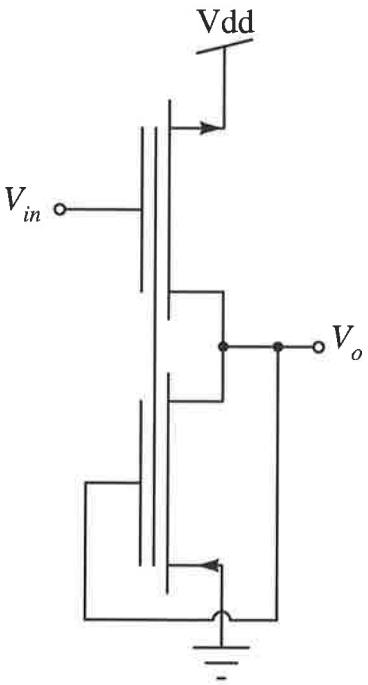


Figure 5.8. A schematic diagram of a controlled gain amplifier using νCMOS inverter. This diagram shows how to design a controlled gain amplifier using a two input νCMOS inverter.

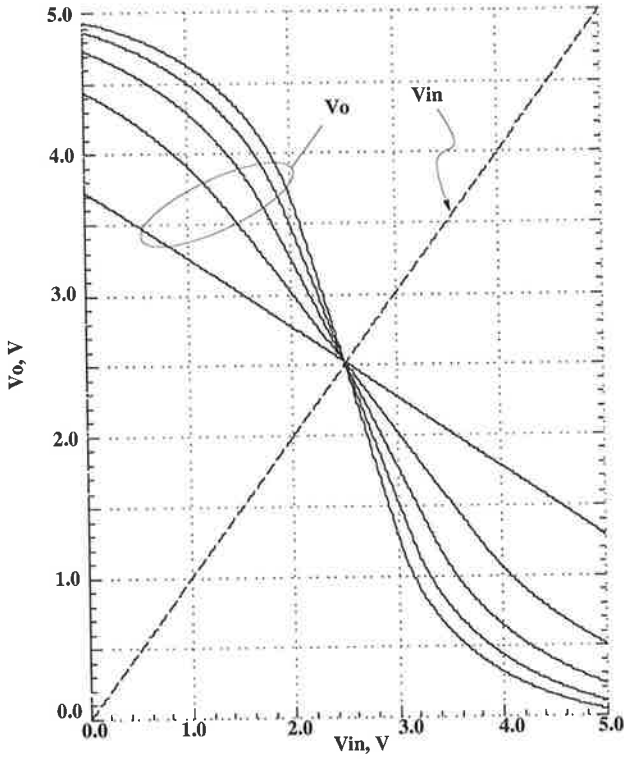


Figure 5.9. The simulation results of the neuron controlled gain amplifier circuit. These simulations show the relationship between the output voltage, V_o, and the input voltage, V_{in}, of the controlled gain amplifier circuit with input coupling capacitor, C_{in}, swept from 10 pF to 50 pF with 10 pF steps, while C_o was fixed at 20 pF. These simulations show that the νCMOS controlled gain amplifier has a gain as a function of the ratio of input coupling capacitance C_{in} and the feedback coupling capacitor C_o. Comparing these curves with Figure 5.6 confirms that the circuits in Figures 5.5 and 5.8 function identically.

From the above first order analysis, it can be seen that the gain is also a function of the ratio of C_{in} to C_o. The simulation results of the circuit with different coupling capacitance from the input to the floating gate, while setting $\beta_n = \beta_p$ and $V_{t_n} = |V_{t_p}|$, are shown in Figure 5.9.

An interesting feature of the above circuits can be seen by taking the special case when $C_{in} = C_o$, this results in an inverting analog buffer circuit with linearity completely independent of the transistors parameters and purely function of a capacitor ratio.

The circuit shown in Figure 5.8 can be explored even further by replacing C_{in} by a number of capacitors, $C_{in_{1\ldots k}}$, where $\sum_{k=1}^{N} C_{in_k} = C_{in}$. By digitally controlling the connection of these capacitors to the floating gate, the gain can be changed accordingly.

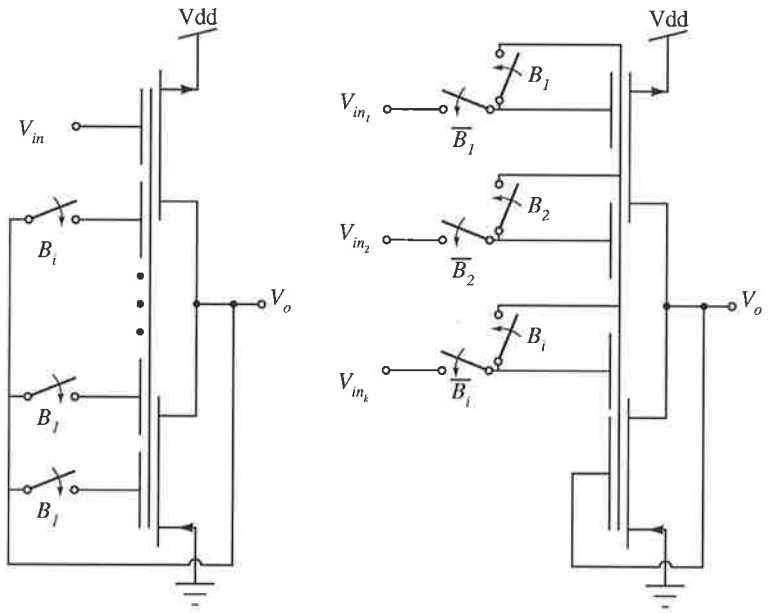
Two simplified conceptual schematic diagrams of the digitally programmable controlled gain amplifiers are shown in Figure 5.10. The gain of the circuit shown in Figure 5.10.a is

$$V_o = -\frac{C_{in}}{\sum_{i=1}^{N} B_i C_{o_i}} V_{in}, \tag{5.16}$$

while the gain of the circuit shown in Figure 5.10.b is given by

$$V_o = -\frac{\sum_{i=1}^{N} B_i C_{in_i}}{C_o} V_{in}, \tag{5.17}$$

where B_i is the state of the switch i, [0,1], and $\overline{B_i}$ represents the complement of the switch state.



(a) (b)

Figure 5.10. A two digitally programmable controlled gain amplifiers using νCMOS inverter. The gain of the neuron-amplifier can be controlled by either controlling the value of the feedback coupling capacitor as in (a) or controlling value of the of the input coupling capacitor as in (b). In both cases a bank of digitally switched capacitors can be used to control the gain.

The implementation of these circuits requires extra care, because the use of switches can inject charge to the floating gate which is hard to estimate and can lead to a shift

in the amplifier operating point. Moreover, the circuit shown in Figure 5.10.a is easier to implement compared to the circuit shown in Figure 5.10.b. The first configuration does not upset the floating gate potential and isolates the floating gate from the switches. However, there is a need to develop a mechanism to provide the right initial voltage on the floating gate as a result of switching coupling capacitance 'in' and 'out'.

5.4.3 Schmitt Trigger Circuits

A Schmitt trigger circuit can be designed using a dual input νCMOS inverter, with positive feedback from the circuit output to one of the input terminals through a digital inverter, as shown in Figure 5.11. The inverter is needed for two reasons, firstly to provide the right polarity at the νCMOS inverter input, secondly, to increase the gain of the output signal and its driving capability. The switching points of the Schmitt trigger circuit can be calculated by finding the conditions under which the νCMOS inverter switches, which can be formulated as

$$\frac{C_{in}}{C_T}V_{in} + \frac{C_o}{C_T}V_o \geq V_{TH}^*, \tag{5.18}$$

where C_{in} is the input coupling capacitor, C_o is the coupling capacitor from the output of the inverter to the floating gate, C_T is the sum of C_{in} and C_o, V_o is the inverter output voltage and V_{TH}^* is threshold voltage of the inverter seen from the floating gate.

The input voltage at which the Schmitt trigger circuit output, V_o, switches from low to high, V_{LH}, can be calculated by considering the circuit initial state when the νCMOS inverter input is grounded. The output of the νCMOS inverter, which will be high, forcing the output of the digital inverter to be low, leading to zero voltage coupling from the output of the Schmitt trigger to its input. So, Equation 5.18 can be written as

$$V_{LH} = \frac{C_T}{C_{in}}V_{TH}^*. \tag{5.19}$$

In a similar fashion, the input voltage at which the Schmitt trigger output switches from high to low, V_{HL}, can be calculated to be

$$V_{HL} = \frac{C_T}{C_{in}}V_{TH}^* - \frac{C_o}{C_{in}}V_{dd}. \tag{5.20}$$

The hysteresis width of the Schmitt trigger circuit, V_{HW}, can be calculated by subtracting Equation 5.20 from 5.19 resulting in

$$V_{HW} = \frac{C_o}{C_{in}} V_{dd}. \tag{5.21}$$

From Equation 5.21, the hysteresis width is function of C_{in}/C_o and linearly dependent on V_{dd}. To make the hysteresis independent of V_{dd}, the switching point of the νCMOS inverter and the inverter has to be independent of V_{dd} which is impractical.

The circuit shown in Figure 5.11 was simulated using C_{in} = 2 pF and C_o= 1 pF. So the switching point of the Schmitt trigger according to Equations 5.19 and 5.20 should be V_{LH} = 3.75 V and V_{HL} = 1.25 Volt, respectively. However, from the simulation results, which are shown in Figure 5.12, the switching points are 1.4 Volt and 3.8 Volt. At first glance, it was thought that the shift from the calculated values is due to the simplified model used in the calculation of the switching point given by Equations 5.19 and 5.20. Further investigation was done and it was found that the difference is not due to the simplified model, but instead was due to the variation of the output level of the second inverter before reaching the switching points. This was verified by buffering the second inverter output using two other inverters to maintain the required phase as shown in Figure 5.13. The switching points after buffering V_o are 1.33 V and 3.68 V. These values correspond to an error value of less than 2% for the calculation of V_{LH} and less than 5.5% for V_{HL}.

The previous Schmitt trigger circuit can be extended further to provide a digitally adjustable hysteresis Schmitt trigger circuit by replacing C_{in} by $C_{1...i}$ capacitors, where $C_{in} = \sum_{i=1}^{N} C_{in_i}$, as illustrated by the conceptual schematic diagram shown in Figure 5.14. Furthermore, as a result of this modification, Equations 5.19, 5.20 and 5.21 can be rewritten as

$$V_{LH} = \frac{C_T}{\sum_{i=1}^{k} B_i C_{in_i}} V_{TH}^* \tag{5.22}$$

$$V_{HL} = \frac{C_T}{\sum_{i=1}^{i} B_i C_{in_i}} V_{TH}^* - \frac{C_o}{\sum_{k=1}^{N} B_i C_{in_i}} V_{dd} \tag{5.23}$$

$$V_{HW} = \frac{C_o}{\sum_{i=1}^{N} B_i C_{in_i}} V_{dd}. \tag{5.24}$$

From the above first order analysis, it can be seen that the switching point of the Schmitt trigger circuit and the hysteresis width are function of the ratio of the multiple input capacitances to the feedback capacitance and the supply voltage. Moreover, the physical implementation of such circuit should take into account the possible charge injection of the switches and their effect on the Schmitt trigger circuit switching points.

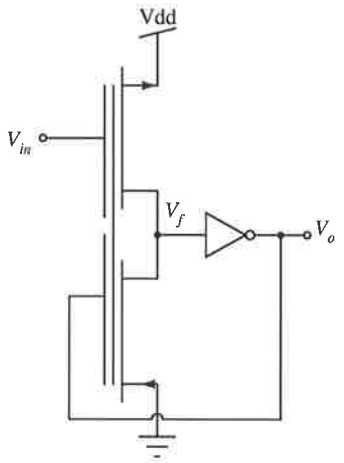


Figure 5.11. Neuron-Schmitt trigger circuit. A *neuron-Schmitt trigger* circuit can be designed using νCMOS inverter. The neuron-Schmitt is composed of a two input νCMOS inverter and a standard CMOS inverter. The second inverter is used to provide the right phase at the inputs of the νCMOS inverter. The switching points of this circuit are purely function of the ratio of the input coupling capacitor connected to C_{in} and the feedback capacitor connected from the inverter output to the second νCMOS inverter input.

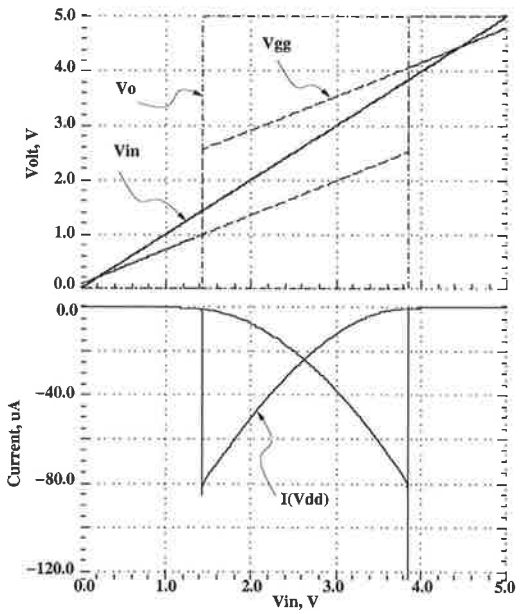


Figure 5.12. The simulation results of the neuron-Schmitt trigger shown in Figure 5.11. The upper panel shows the input-output characteristics of the Schmitt trigger circuit, where V_{gg} is the voltage at the floating gate of the νCMOS inverter, V_o is the neuron-Schmitt trigger output and V_{in} is the input voltage sweep. The lower panel is the current drawn from the supply voltage as function of the input voltage.

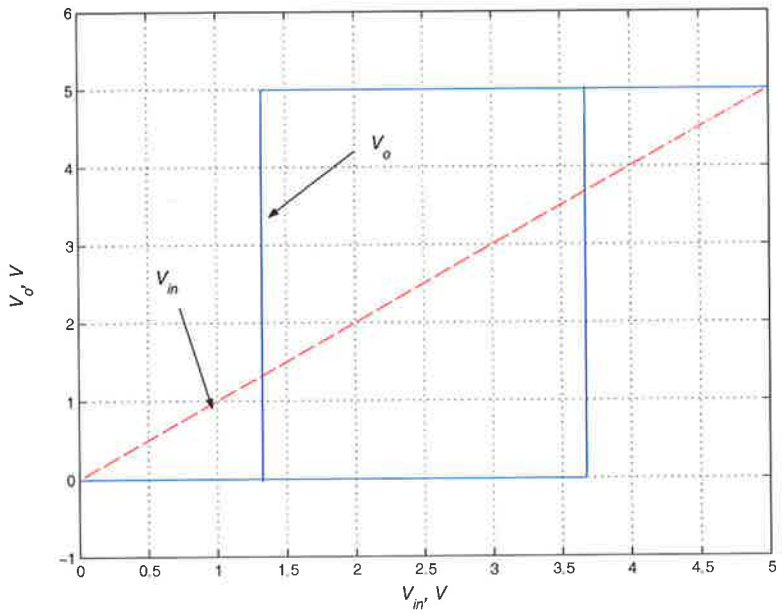


Figure 5.13. The simulation results of a Schmitt trigger shown in Figure 5.11 with buffered output. These simulations show the neuron-Schmitt trigger output, V_o after being buffered by two standard CMOS inverters. Two inverters were used to obtain the right phase at the νCMOS inverter input. These simulations show that switching points of the neuron-Schmitt circuit is consistent with switching points of $V_{LH} = 1.33$ V and $V_{HL} = 3.68$ V calculated by Equations 5.19 and 5.20.

5.5 Power Dissipation Reduction

There is no one way to reduce the power dissipation of circuits designed using νMOS transistors. In fact most of the techniques used for power reduction in conventional CMOS circuits can be used with circuits designed using νMOS transistors. For example, the common method to reduce the power dissipation is to reduce the supply voltage. Another is by limiting the current passing through the circuit. The current limiting technique will work well with the controlled gain amplifier circuit discussed in Section 5.4.2, and it will not affect the gain given by Equation 5.15. The combined amplifier with a limiting circuit is shown in Figure 5.15. The use of the limiting circuit shown in Figure 5.15 will reduce the power through two effects. Firstly, through reducing the power supply due to the voltage drop across mp_1, secondly, through limiting the current through the amplifier which is controlled through the reference current source, I_{ref}. The simulated output characteristics of the circuit shown in Figure 5.15 with a reference current of 1 μA

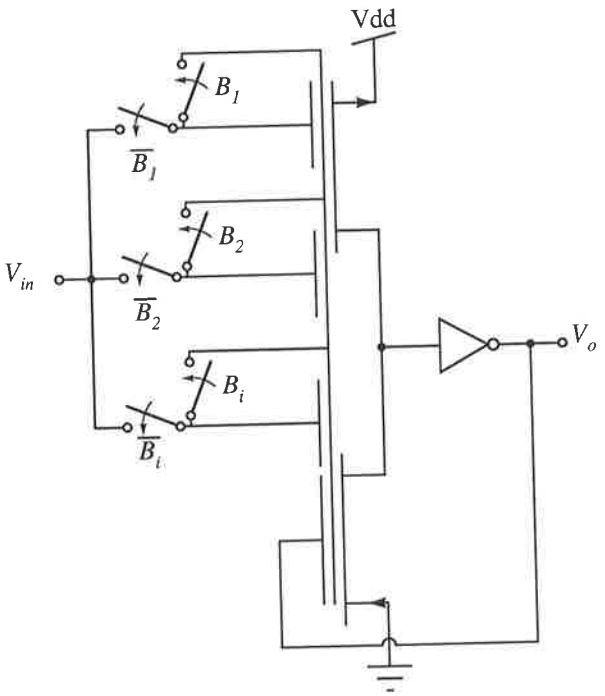


Figure 5.14. A conceptual Digitally adjustable neuron-Schmitt trigger hysteresis. A digitally adjustable neuron-Schmitt trigger hysteresis can be designed by controlling the ratio of the coupling capacitor the feedback capacitor.

are shown in Figure 5.16. These simulations show that the amplifier gain is still function of the capacitor ratios and it is independent of the supply voltage variation.

To reduce the current consumption of the Schmitt trigger circuit shown in Figure 5.11, the use of the limiting current technique is not appropriate because it will limit the driving capability of the νCMOS and digital inverters, leading to slow switching of these inverters, which will affect the Schmitt trigger circuit functionality. For such circuits, reducing the power supply is more appropriate and result in less current consumption without affecting the circuit functionality.

5.6 Experimental Work

The amplifier circuit shown in Figure 5.8 and the Schmitt trigger circuit shown in Figure 5.11 were chosen to demonstrate the feasibility of using neuron-MOS transistors in analog design. These circuits were fabricated in a double poly, double metal 0.8 μm HP process through MOSIS. For the amplifier circuit, the ratio of the n and p MOS transistors were adjusted in order to have an operating point around $V_{dd}/2$, while the capacitor

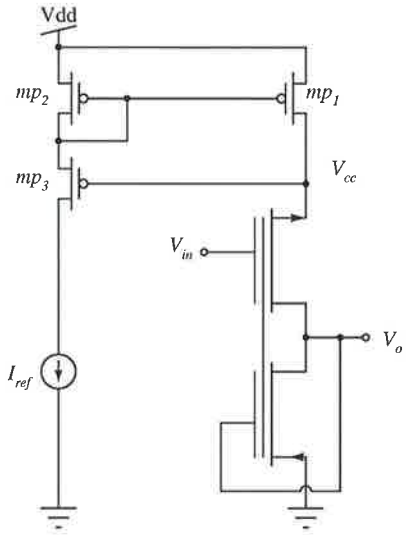


Figure 5.15. A low power controlled gain neuron-amplifier. The current drawn from the power supply by the amplifier can be limited to reduce the power consumption.

sizes used are 2 pF for the input capacitance and 1 pF for the feedback capacitor. The measured amplifier gain shown in Figure 5.17 is 2 or 6 dB. This gain is consistent with the gain predicted by Equation 5.14. However, the operating point is shifted from $V_{dd}/2$. This offset voltage can be due (i) to some trapped charges in the floating gates, (ii) due to the difference in the threshold voltages or (iii) the β's of the n and p MOS transistors, resulting in a dc offset voltage at the output according to Equation 5.14. An attempt was made to illuminate the whole chip to UV light for 3 hours with all the circuit terminals connected to ground. This experiment resulted in no shift in the output offset voltage, hence it was concluded that the offset is either due to threshold voltage difference or the β's of the n and p MOS transistors as the same amount of voltage shift was observed in the Schmitt trigger circuit as discussed later.

For the Schmitt trigger circuit, an input coupling capacitance of 2 pF and a feedback capacitor of 1 pF were used in the design shown in Figure 5.11. According to the design example presented in Section 5.4.3, the Schmitt trigger switching points should be $2V_{dd}/3$ and $V_{dd}/3$. The measured results for V_{LH} and V_{HL} from Figure 5.18 are 4 V and 1.8 V, respectively. Comparing these measurements with the simulation results reported on page 152 the resultant error is less than 1% after removing the 200 mV offset voltage that was observed during the measurements. This offset did result in shifting the hysteresis width of the Schmitt trigger circuit by 200 mV. This hysteresis shift is equal to the input offset voltage observed in the amplifier measurements. The neuron-amplifier and

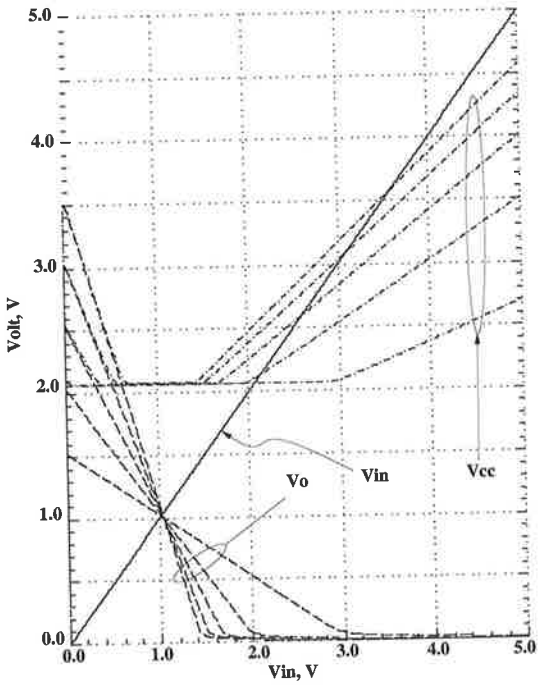


Figure 5.16. Simulation results of the low power controlled gain neuron-amplifier. These simulations show the input-output characteristics of the controlled gain amplifier circuit shown in Figure 5.15. The simulations were conducted at 3 V, 3.5 V, 4 V, 4.5 V and 5 V with the input voltage is swept from 0 to 5 Volt and the input coupling capacitor was swept from 10 pF to 50 pF in 10 pF steps, while the feedback coupling capacitor was set to 20 pF. These simulations show the amplifier gain is independent of the power supply voltage and only dependent on the ratio of the input coupling capacitor and the feedback capacitor.

neuron-Schmitt measurements indicate that the shift is due the deviation of the inverter input-output characteristics at $V_{in} = V_{out}$ from $V_{dd}/2$ during the fabrication process.

5.7 Summary

The neuron-MOS transistor has been used extensively in digital circuit design, however, the use of such transistors in analog design has not been fully investigated. In this chapter, a general model for the neuron-MOS transistor has been developed. The model includes all the transistor terminal capacitances – such capacitances have negligible effect on digital circuitry. However, they can cause a shift in the circuit operating point in the case of

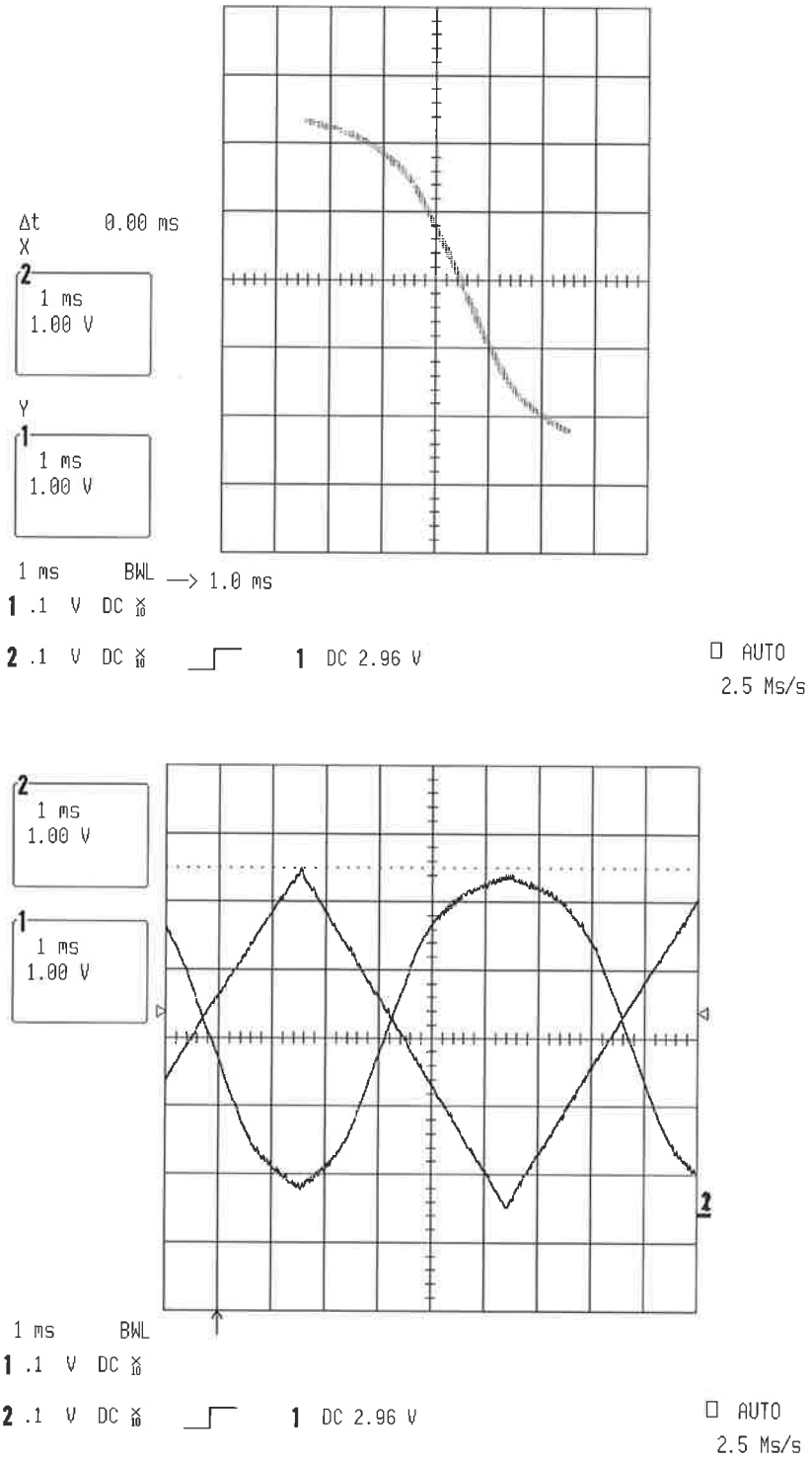
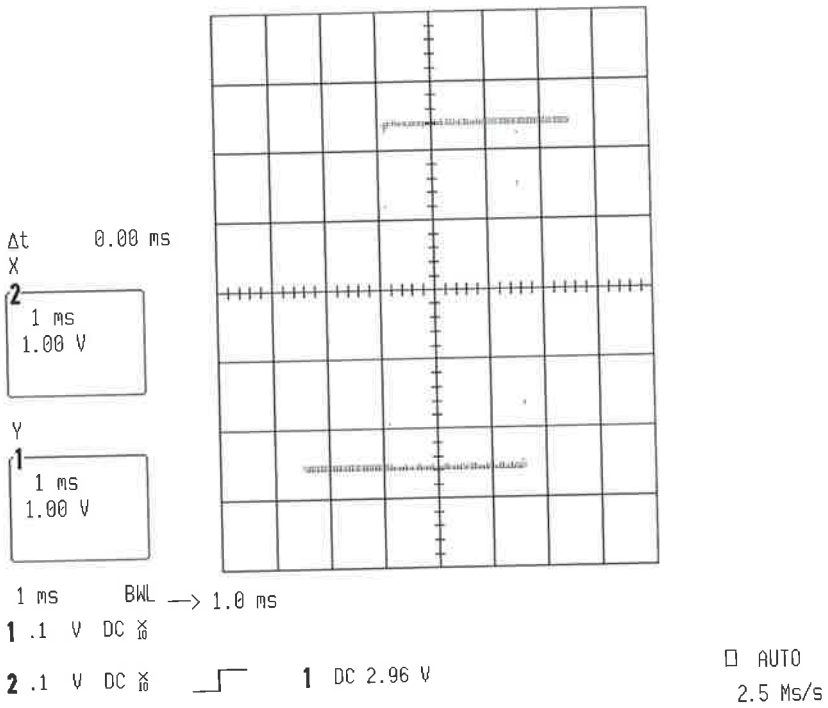


Figure 5.17. The measured input-output characteristics from fabricated neuron-amplifier. The upper panel shows the measured input-output characteristics of the neuron-amplifier circuit. These measurements show a voltage gain of 2 (6 dB) as designed at a 5 V supply. The lower panel shows the measured input-output characteristics in the time domain (Screen dump from the LeCroy 9360 Oscilloscope).



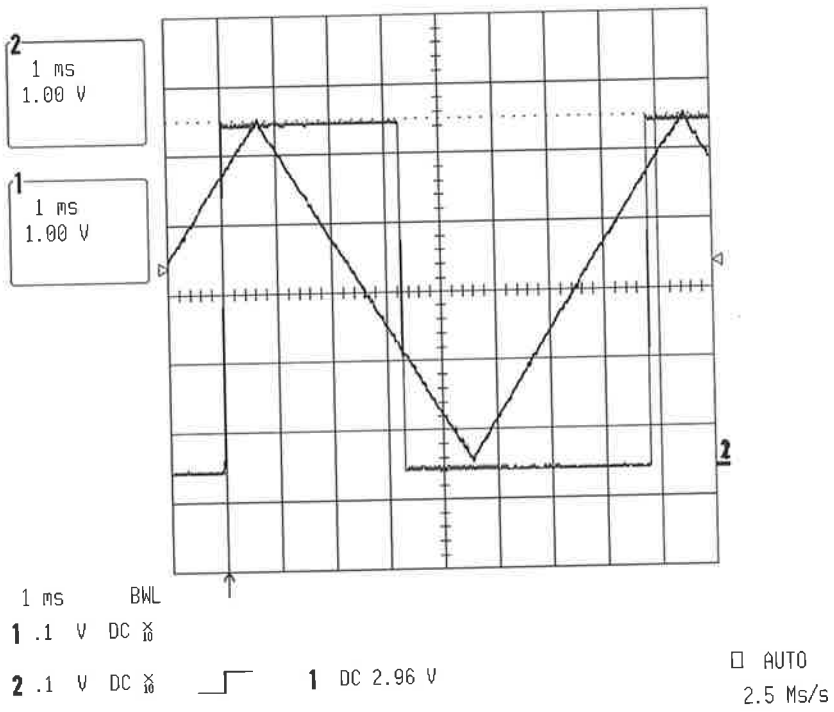


Figure 5.18. The measured input-output characteristics of the neuron-Schmitt trigger circuit. The upper panel shows the Schmitt trigger hysteresis measured input-output characteristics of the neuron-MOS Schmitt trigger at 5 V supply. The lower panel shows the measured input-output characteristics in time domain (Screen dump from the LeCroy 9360 Oscilloscope).

analog circuit design. Moreover, a number of key parameters have been identified to help in designing both analog and digital circuitry.

The analog examples designed and discussed in this chapter are meant to demonstrate that νMOS transistor can be used to designing practical precision analog circuits. The controlled gain amplifiers discussed in Section 5.4.2, represent good candidates as basic building blocks for analog signal processing. Furthermore, the Schmitt trigger circuits, discussed in Section 5.4.3 represent alternative analog circuitry where the circuit characteristics are function of capacitor ratios. The extension of this circuit to a digitally adjustable hysteresis provides more functionality and flexibility by using easy to generate digital control signals.

The operation of the controlled gain amplifier circuit shown in Figure 5.8 and the Schmitt trigger circuit shown in Figure 5.11 were verified experimentally through the fabrication of these circuits in a HP process through MOSIS. The measured results are consistent with presented analysis and simulations presented for these circuits.

Even though, νMOS has the potential for low power and small area, there are a number of pitfalls that limit the performance of circuits designed using νMOS. The charge storage on the floating gate can present an offset voltage at the output of these circuits and might drive them out of the useful dynamic range of operation. Secondly, device performance is affected by scaling, as scaled νMOS devices result in higher parasitic capacitance from the floating gate to the devices' terminals and hence a reduction in the floating gate gain factor. In digital circuit design, the major pitfall in using νMOS is the reduction of noise margin. This margin reduces as a function of the number of inputs of a neuron-MOS gate. Further research is needed to develop techniques that reduce the charge storage at floating gate and improving the noise margin of neuron-MOS circuits. A combined νMOS structure with EEPROM structure to result in "νEEPROM" is a possibility. However, this would complicate the device operation.

In this chapter we have demonstrated that targeting fabrication process and circuit design levels are used successfully in designing useful analog building blocks with small area and has the potential to provide low power circuitry using νMOS device. This is due to the fact that the input signals are capacitively coupled to the floating gate and hence all of the device operations rely on charge manipulation on the floating gates. Moreover, as the functionality per unit area is increased, this will enable the design of systems with complex functions with smaller silicon area compared to traditional MOS circuitry. Hence, these designs represent a step forward for ultra large scale integration (ULSI) density. In the next chapter, we will show also how targeting circuit design level can be used to design very high value floating resistors in the GΩ range using the output conductance for MOS

transistors biased using very small current. This structure will result in low power and small area active floating resistor.

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Chapter 6

Novel Low Power Ripple Through Gray Code Counters

AS mentioned earlier, power dissipation of a mixed signal system can be reduced at a number of design levels: the process fabrication technology, circuit, architectural and algorithmic levels. In this chapter the circuit, architectural and algorithmic levels are targeted to reduce power dissipation in such systems. This is achieved by developing new generalised formulas for generating an n bit *Gray code sequence*. Using these formulas in the design of a counting circuit will result in low power dissipation, reducing the number of disturbances on the common power supply for the analog and the digital parts and hence reduce the noise injection from the digital part to the analog part of the mixed system.

These formulas are used to implement counting circuits that produce $n+1$ bit Gray and n bit binary outputs using only n flip-flops. To improve the power further, an optimised static flip-flop circuit that has favoured characteristics in mixed systems are discussed. The resulting counting circuits have attractive features that qualify them as a basic building block in mixed signal applications.

6.1 Introduction

In mixed mode analog-digital applications the noise coupling from the digital circuitry to the analog part will not only degrade or limit the system performance but can also cause malfunction of the analog circuitry [Nagata *et al.* 2000, Blalack & Wooley 1995]. Hence, special attention should be given to the analog part of the system. These sources of noise can be reduced at both the architectural and circuit levels. At the architectural level the noise can be reduced by (*i*) physically separating the analog and the digital parts on the chip, (*ii*) shielding the analog part by surrounded it by a grounded well, and (*iii*) using a separate supply voltage for the analog part. The noise at the circuit level can be reduced by (*i*) using differential analog and digital circuit designs, (*ii*) reducing the switching activity of the digital part, (*iii*) reducing the simultaneous switching in the digital circuitry, (*iv*) using a slew rate limited digital cells, and (*v*) ordering the input transistors for minimum switching [Ercan *et al.* 2002, Parra *et al.* 2001, Hakenes & Manoli 2000, Hakenes & Manoli 1999a, Hakenes & Manoli 1999b]. Hence, reducing the switching activity and the simultaneous switching will serve in both power reduction of the overall system and reducing noise coupling to the analog circuitry.

Counters are basic modules in digital system design. When these modules are used in mixed analog-digital applications, they can be the source of digital switching noise in addition to a power drainage components. For example, in the targeted RFID system most of the disturbances on the common power supply are a result of a carrier oscillator and state machine. The later is usually replaced by a binary counting circuit. The reduction of transients due to the oscillator circuit are dealt with through the design of low power Schmitt-oscillator circuits using the low power Schmitt trigger circuit discussed in Chapter 4. The transients and the activities of the counter circuit can be reduced by using a low power unit step counter.

There are a number of *unit step codes* [Savage 1997] that can be used in the counting circuit. Binary counting is the most common one, however Gray code counting was chosen because it is a commonly known unit step code and has features that are favourable in mixed analog-digital applications [Pace *et al.* 1998, Daponte *et al.* 1996]. For comparison, the number of transitions in a Gray code sequence and a binary sequence – in counting from the minimum to maximum – is given by Equation 6.1, where n is the number of bits. From the equation it is evident that when using a Gray code sequence there is a substantial decrease in the number of transitions for the same number of states represented.

$$\text{No. of transitions} = \begin{cases} 2^n & \text{Gray code} \\ \sum_{i=1}^{n} 2^i = 2^{n+1} - 2 & \text{Binary code.} \end{cases} \quad (6.1)$$

There are a number of procedures a designer can follow to design Gray code counters. These methods include using finite state machine [McCalla 1992, Pucknell & Eshraghian 1986], using the rules described in [Bartee 1981], or converting a binary sequence to a Gray code sequence by using a set of combinatorial logic elements [McCalla 1992]. However, if any of these methods are used in a Gray counter design, the resulting circuitry will be complicated and will have a larger number of transistors compared to proposed approaches in this chapter.

In this chapter, a number of ripple through Gray code counters are proposed. Each of these counters is composed from a basic cell. The attractive features of the proposed counters are:

- they can be extended to any number of bits by just cascading a number of basic cells without any additional combinatorial circuitry;
- some of them use a race free basic cell;
- they have low power features with few internal and simultaneous transitions;
- they provide the binary code sequence at no additional circuitry;
- they use n basic cells to generate an $n+1$ bit of Gray code output;
- they provide n binary bits in addition to the $n+1$ Gray code bits at no extra cost.

6.2 Gray Code Sequence Generation

From Table 6.1 generalised formulas for each Gray code bit in terms of CLK can be deduced as follows:

$$\begin{aligned} G_0 &= \diamond(\Delta(CLK)) \\ G_1 &= \diamond(\Delta^2(CLK)) \\ G_2 &= \diamond(\Delta^3(CLK)) \\ G_{n-1} &= \diamond(\Delta^n(CLK)) && \text{; for all bits except the last bit} \\ G_n &= \Delta^n(CLK) && \text{; unique to the last bit} \end{aligned}$$

Table 6.1. A four bit Gray code sequence referenced to input clock states. This table shows how to derive the Gray count sequence based on the clock signal transitions and the application of the divide Δ and shift $\diamond$ operators to the clock signal transitions.

State No.	G_3	G_2	G_1	G_0	CLK	$\Delta(CLK)$	$\diamond(\Delta(CLK))$
1	0	0	0	0	0	0	0
2	0	0	0	1	1	0	1
3	0	0	1	1	0	1	1
4	0	0	1	0	1	1	0
5	0	1	1	0	0	0	0
6	0	1	1	1	1	0	1
7	0	1	0	1	0	1	1
8	0	1	0	0	1	1	0
9	1	1	0	0	0	0	0
10	1	1	0	1	1	0	1
11	1	1	1	1	0	1	1
12	1	1	1	0	1	1	0
13	1	0	1	0	0	0	0
14	1	0	1	1	1	0	1
15	1	0	0	1	0	1	1
16	1	0	0	0	1	1	0

where

$\Delta(arg)$	is an operator that divides the frequency of *arg* by two and aligns the negative transitions;
arg	represents an input waveform;
$\diamond(arg)$	is an operator that delays *arg* by a quarter of the *arg* period and inverts the result;
$n+1$	is the number of Gray code bits.

Furthermore, the binary counting sequence can be written using the divide, Δ operators as

$$
\begin{aligned}
B_0 &= \Delta(CLK) \\
B_1 &= \Delta^2(CLK) \\
B_2 &= \Delta^3(CLK) \\
B_{n-1} &= \Delta^n(CLK) && \text{; for all bits except the last bit} \\
B_n &= \Delta^n(CLK) && \text{; unique to the last bit.}
\end{aligned}
$$

Comparing the binary counting formulas to the Gray counting formulas, it can be seen that the binary formulas are a byproduct of the Gray code counting formula. Hence, it is possible to obtain the binary counting sequence from the Gray counting formula at no extra cost.

6.3 Formulas Implementation

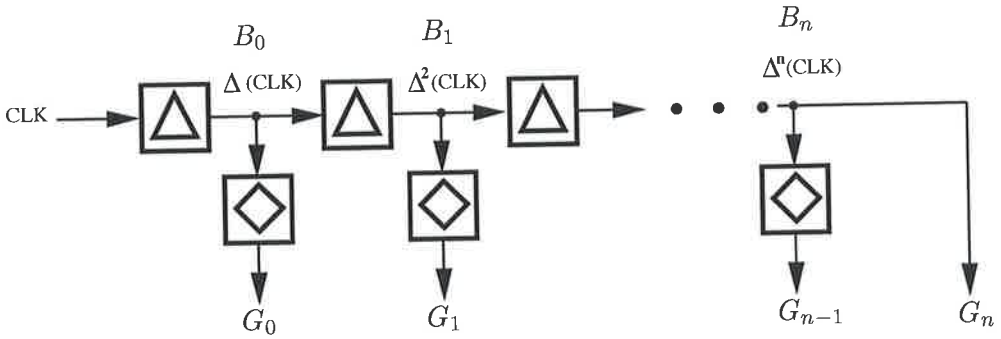

Figure 6.1. A block diagram of an N-bit Gray code counter. This diagram is a direct implementation of the technique presented in Table 6.1 to generate an N-bit Gray code counter. The counter can be extended to any number of bits by adding extra Δ and $\diamond$ at no extra combinational logic.

The formulas discussed in the previous section can be implemented in hardware by either designing circuit modules to perform the Δ and $\diamond$ operations as shown in Figure 6.1 or by designing a circuit that performs both of these operations in one circuit. The Δ and $\diamond$ operations are an integral part of edge-triggered JK, as will be illustrated by the following two implementations of these operations. Firstly, using an *optimised JK flip-flop*, secondly by using a *dynamic JK flip-flop*.

6.3.1 Formulas implementation using JK flip-flops

Hence we present an example of implementing the formulas presented in Section 6.2, through the use of JK flip-flops. A *static JK flip-flop* optimised by Vittoz [Vittoz 1985] is used. The original 22 transistor circuit was developed as a race-free binary counter and then optimised to reduce the power dissipation, and the number of the transistors, resulting in the 19 transistor basic counter cell shown in Figure 6.2. This circuit was redesigned for the 1.2 μm CMOS technology and the used transistor sizes are shown on the schematic. The reduction in the number of transistors was achieved by keeping only transistors necessary to cause transitions, and transistors needed to maintain static behaviour of the circuit. The attractive features of the circuit are:

- it is triggered on the negative transition of the input as is appropriate for an upward counter;
- it is a true single phase circuit, i.e. there is no need for the input signal complement;
- each internal variable transitions occurs at half the frequency of the input signal, and may thus be used as the output of the divider;
- the circuit is race-free;
- it provides both the direct form and the complement of the divided input.

Careful examination of the waveforms within that circuit shows that it is possible to obtain the two basic operations required for the Gray code counter design. The Δ operation is taken from node B, while the $\diamond$ operation is taken from node G. A suitable assembly of the basic building block to form an N bit Gray code counter is shown in Figure 6.3.

The optimised JK flip-flop shown in Figure 6.2 was used in the design of a 3 bit Gray – 2 bit binary counter. The design was simulated as shown in Figure 6.4 using Level 28 model parameters obtained from Orbit Semiconductor for a 1.2 μm, double poly, double metal p-well process.

6.3.2 Formulas implementation using a dynamic D-flip-flops

An implementation of a Gray code counter using dynamic logic was presented in [Milgrome *et al.* 1992, Milgrome *et al.* 1991] and shown in Figure 6.5. Unfortunately, the simulation of this circuit as it is, shows that it is not possible to obtain Gray code counting. However,

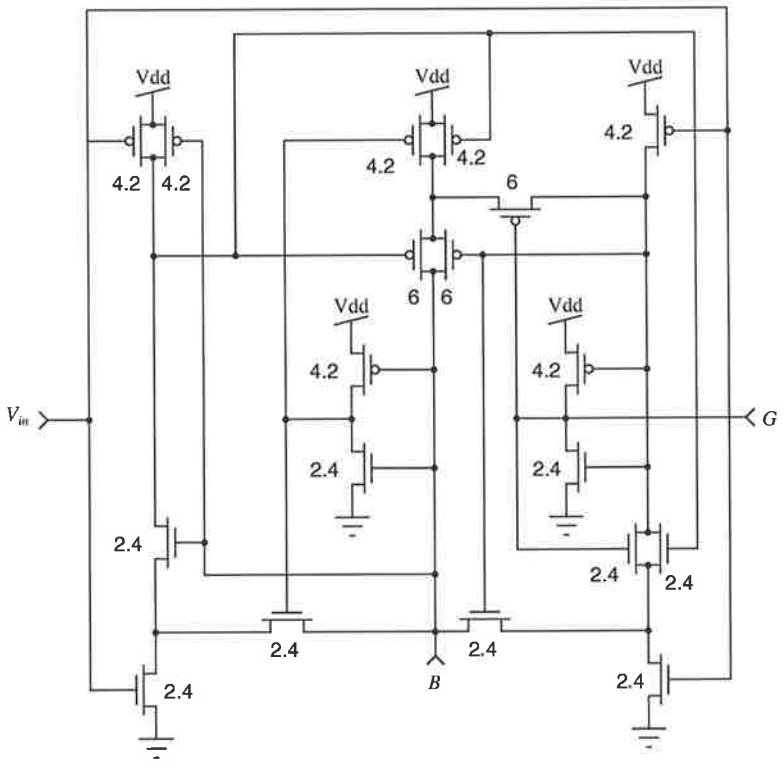

Figure 6.2. Circuit diagram of the optimised divide by two circuit. This circuit was proposed by Vittoz [1985]. The numbers shown on the diagram are width of transistors in micrometers. All transistors in the schematic use a minimum length of 1.2 μm.

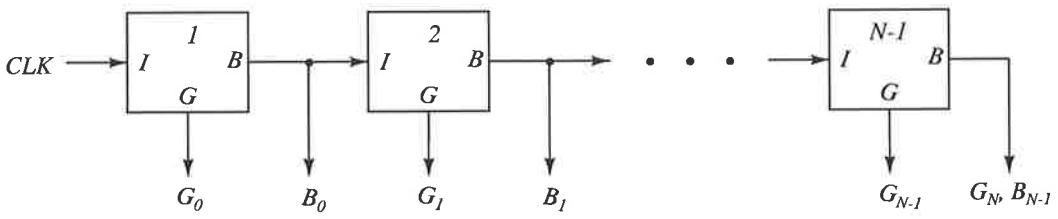

Figure 6.3. Block diagram of an N bit Gray code counter. As the circuit shown in Figure 6.2 produces the Δ and $\diamond$ operators needed to produce Gray count sequence, the block diagram shown in Figure 6.1 can be mapped directly to implement an N bit Gray code counter.

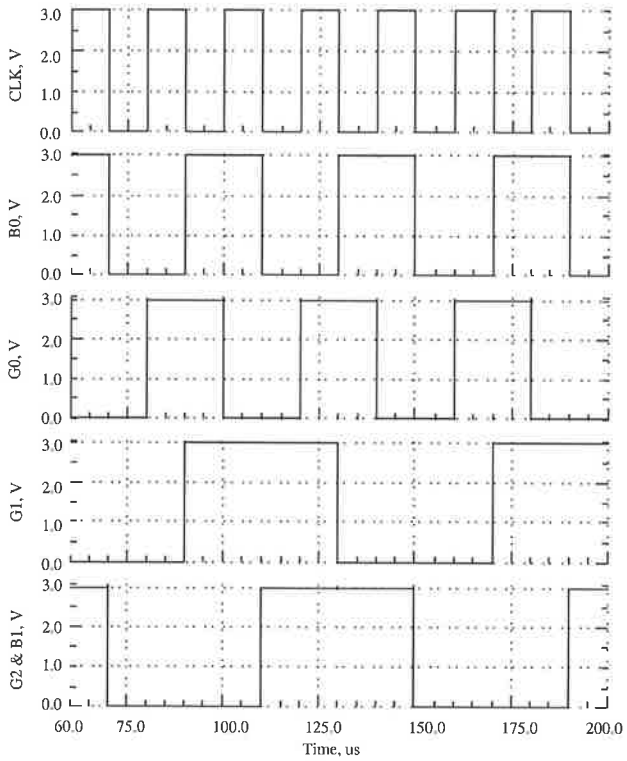

Figure 6.4. The simulation results for a 3-bit Gray and 2-bit binary code counter. These simulations show how that the presented counter can produce both Gray and Binary counting sequences at no extra cost.

investigating the structure formed by INV0 – INV2, shows that the internal waveforms produce an equivalent to divide and shift functions needed to produce the Gray code sequence. Hence, a new dynamic Gray circuit can be implemented either using inverters and transmission gates or simply by using clocked inverters as shown in Figures 6.6 and 6.7, respectively. The simulation results for a 4 bit Gray – 3 bit binary counter using inverters and transmission gates, and clocked inverters are shown in Figures 6.8 and 6.9, respectively. These simulation results are obtained by applying a symmetrical input signal with 100 kHz pulse repetition rate (not shown).

In practical designs the initial conduction of a dynamic circuit should be set correctly. For the dynamic JK flip-flop discussed above, the internal nodes can be initialised to either the supply voltage or ground by connecting a transistor between the required node to be initialised and either of the supply terminals, based on the required initialisation state. The gate of this transistor can be connected to a monostable multivibrator that produces a short reset pulse during the energisation of the common supply terminals.

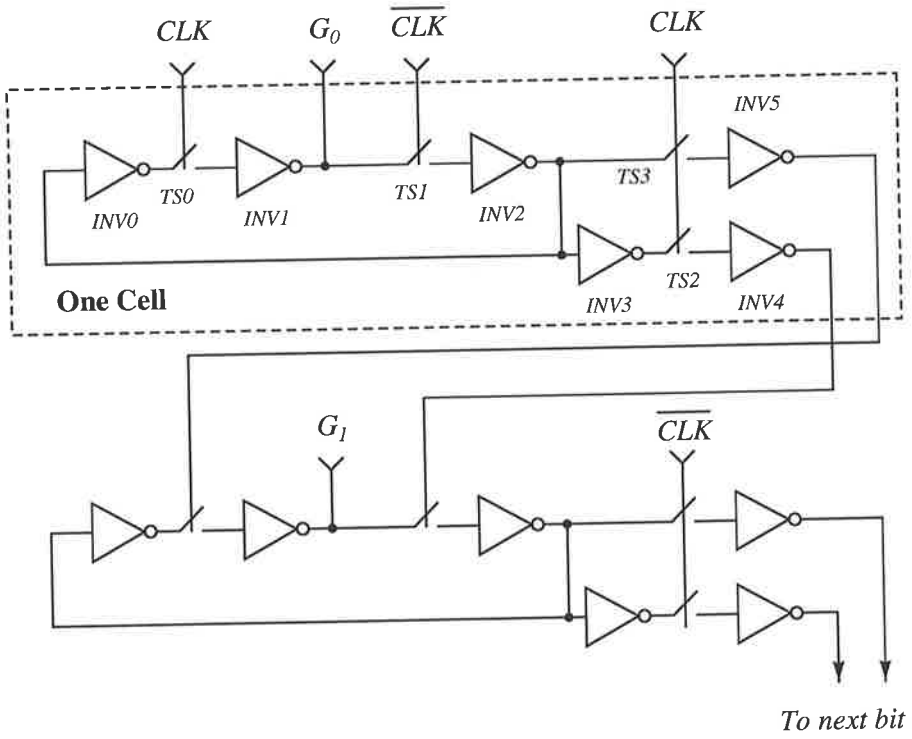

Figure 6.5. A schematic diagram of the dynamic Gray code counter. A schematic diagram of a dynamic Gray code counter from [Milgrome *et al.* 1992]. This circuit was not able to produce Gray code counting without modification, as discussed in the text.

It should be mentioned that both versions of the dynamic counters are sensitive to the skew between CLK and $\overline{CLK}$. Such skew can cause the counter to oscillate. When CLK and $\overline{CLK}$ have the same state the counter is reduced to a 3 stage ring oscillator. This problem can be solved by either equalising the delay between the counter input signals, or by feeding the CLK signal into a phase splitting circuit. Such a circuit can be a simple inverter implemented using the *cascade voltage switch logic* (CVSL) family as shown in Figure 6.10. In addition to the skew reduction and the production of simultaneous outputs, the CVSL inverter also improves the rise and the fall time of the CLK signal, which is also important to maintain the functionality of the counting circuit. However, CVSL is known to be a current 'hungry' logic family as a direct low impedance path between the supply terminals can occur when skew between the input signals and their complements occurs.

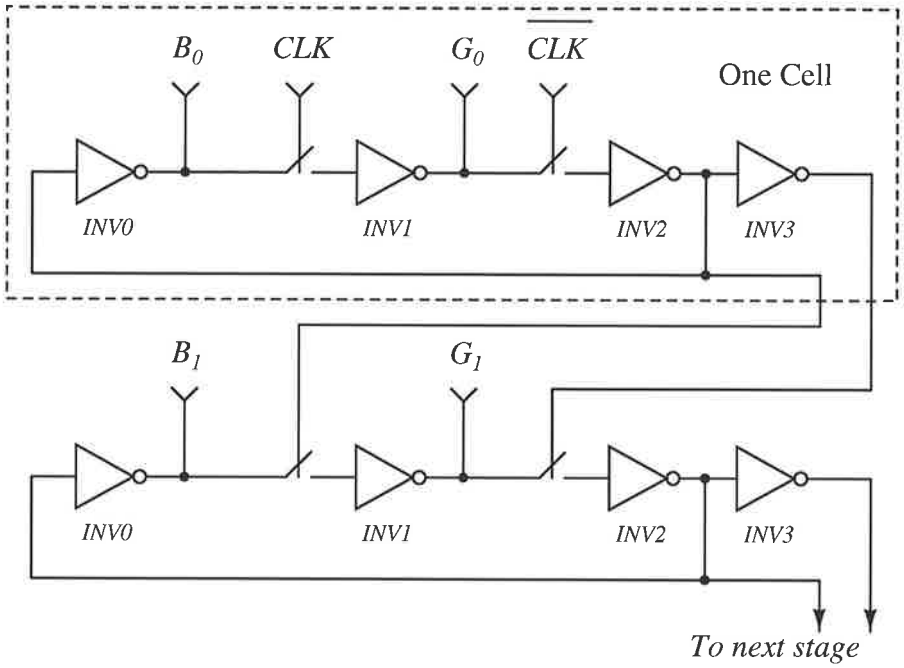

Figure 6.6. A schematic diagram of the new dynamic Gray-binary counter that uses inverters and transmission gates. This circuit a modified version of the circuit proposed by Milgrome *et al.* [1992] to produce the correct Gray code counting sequence.

6.4 Experimental Work

The optimised JK flip-flop circuit shown in Figure 6.2 was used in the implementation of a compact counter that produces a 4 bit Gray and 3 bit binary counting sequences. For this purpose a compact layout of the circuit shown in Figure 6.2 was generated as shown in Figure 6.11. The block diagram of the designed counter is shown in Figure 6.12. The Gray and the binary counting outputs were multiplexed to reduce the number of output pads required. This structure was fabricated in a 2 μm double poly, double metal n-well process through MOSIS. The input signal was a symmetrical pulse with a 1 kHz pulse repetition rate and 5 Volts amplitude. The measured Gray code count is shown in Figure 6.13, while the measured binary code count is shown Figure 6.14. These waveforms were measured using the Tektronix 3001 GPX instrument.

6.5 Summary

Based on the formulas discussed in Section 6.2, two types of counting circuits were designed, namely static and dynamic. The operation of the static version was verified both

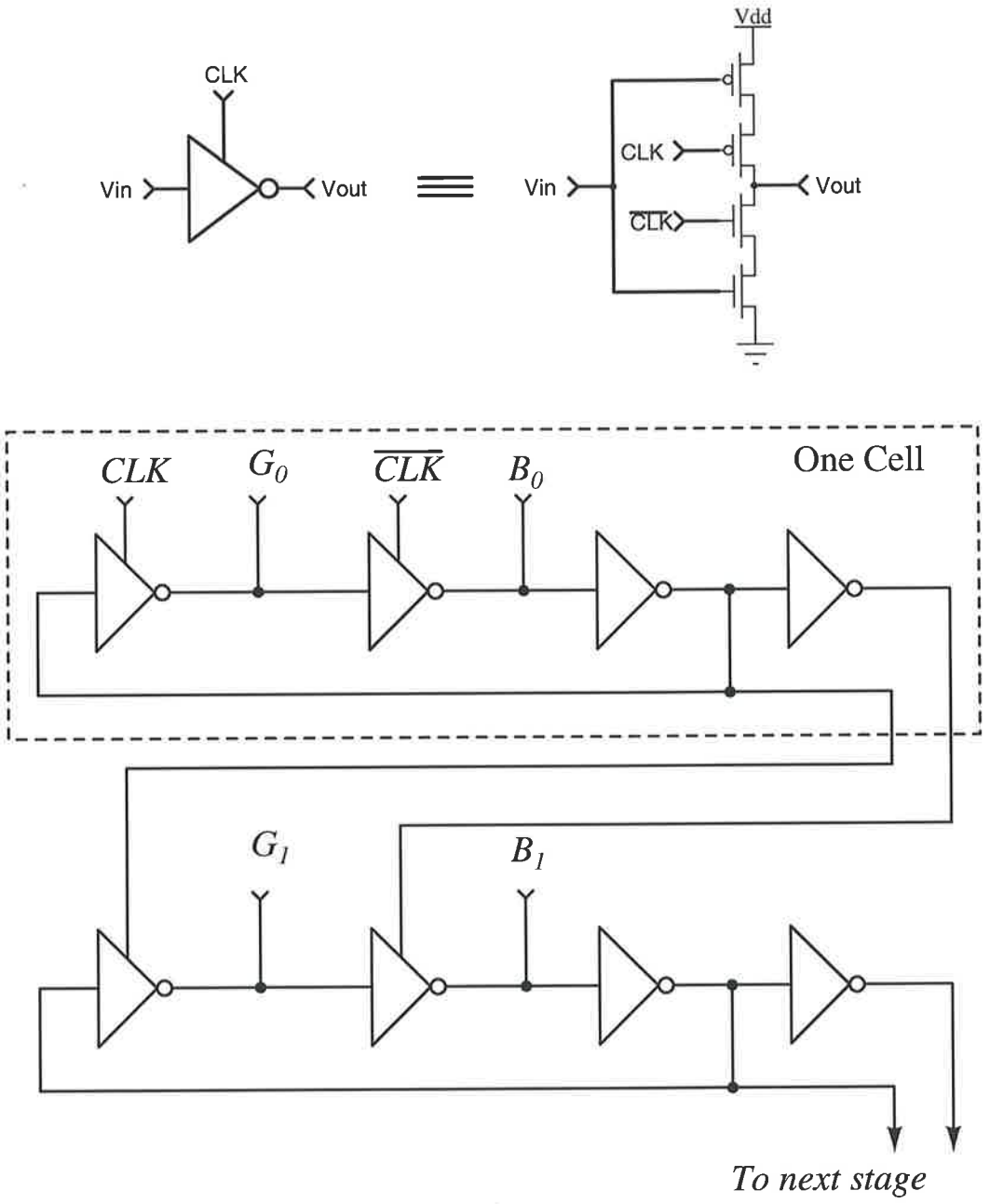

Figure 6.7. A schematic diagram of the new dynamic Gray-binary counter using clocked inverters. In this counter the clocked inverters were used. This allows a very compact layout and a slightly lower-power compared to the transmission line equivalent structure.

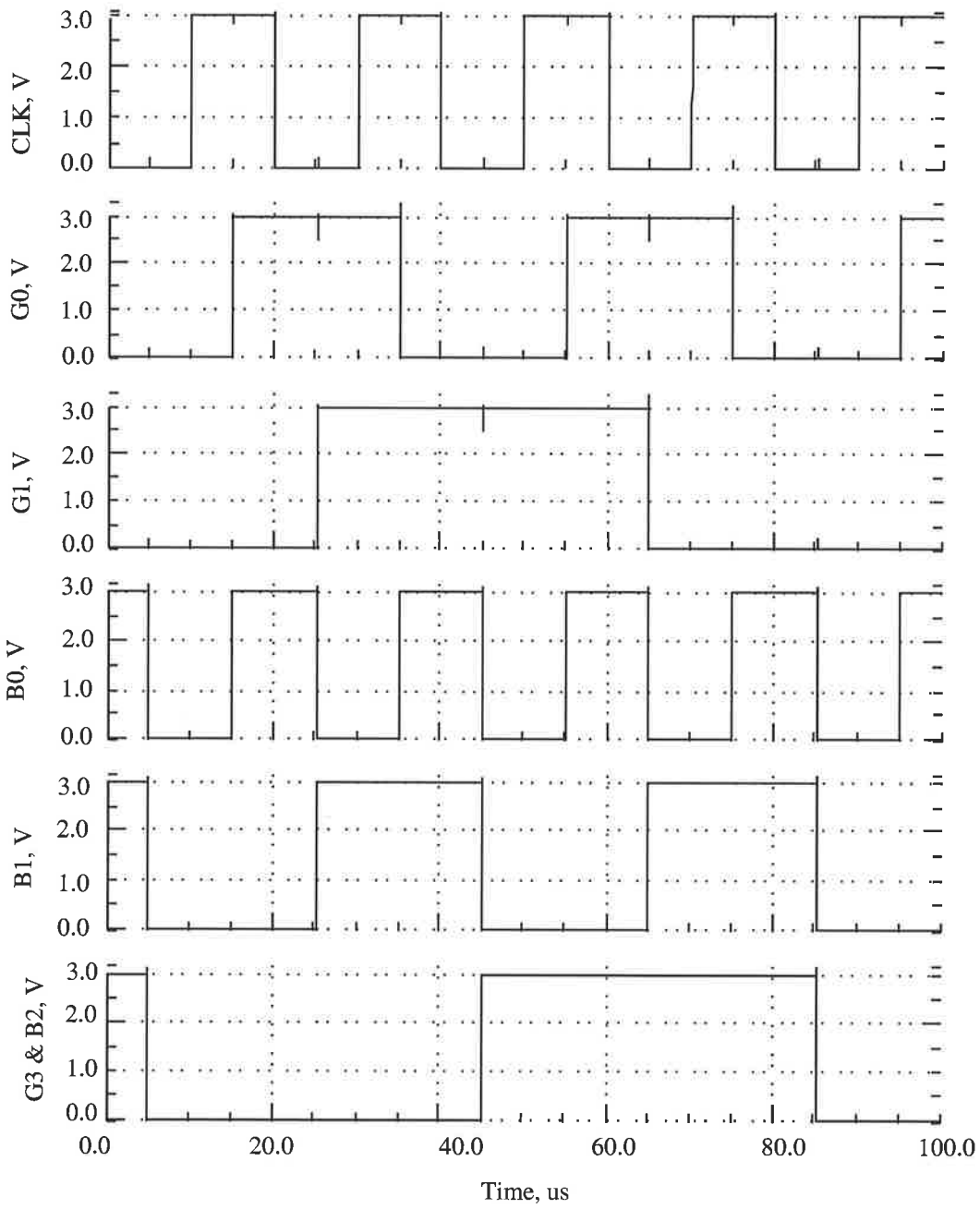

Figure 6.8. The simulation results of the new dynamic Gray-binary counter shown in Figure 6.6. These simulations show both the Gray and binary counting outputs from the dynamic version Gray-binary counter that uses transmission gates.

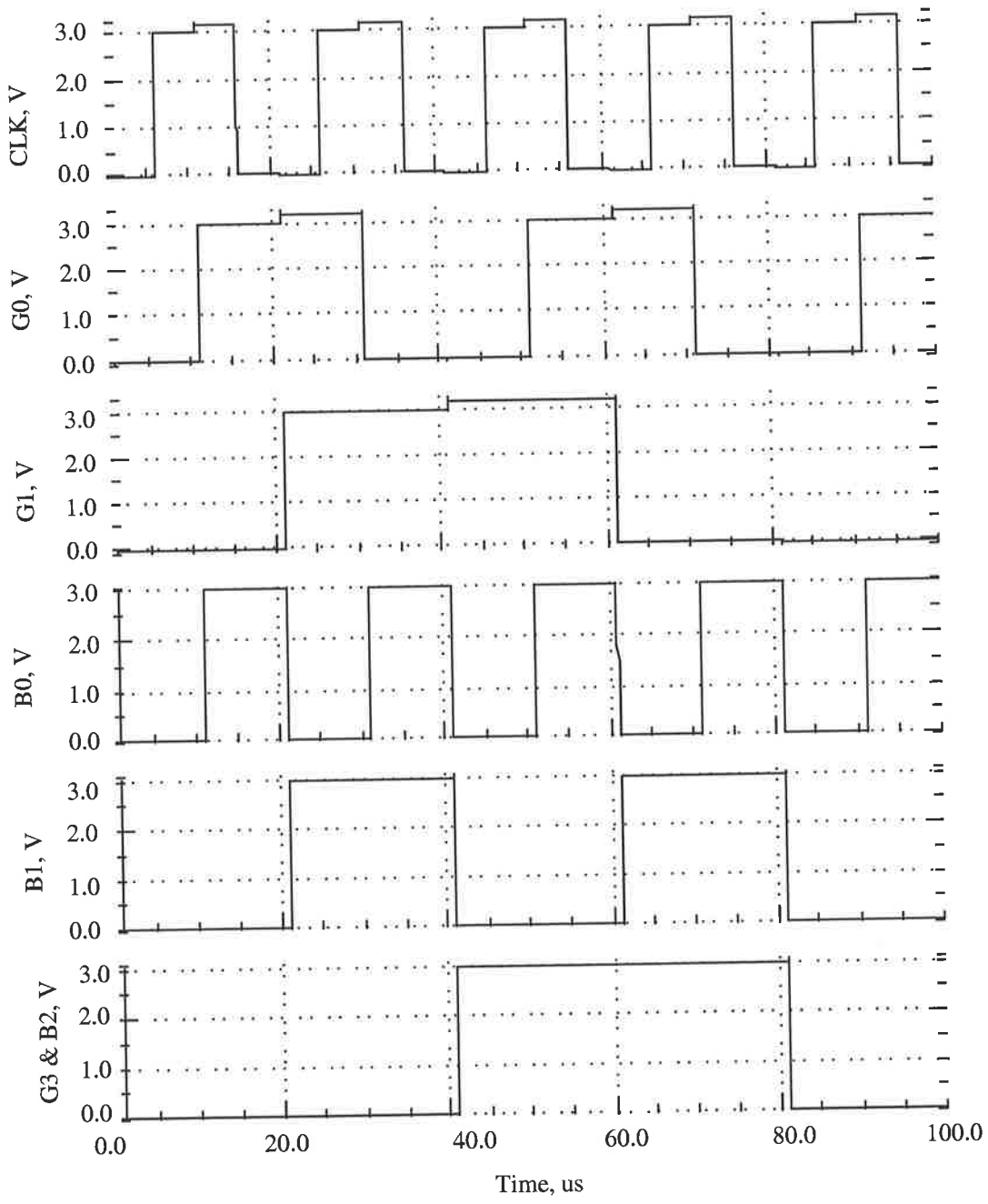

Figure 6.9. The simulation results of the new dynamic Gray-binary counter shown in Figure 6.7. These simulations show both the Gray and binary counting outputs from the dynamic version Gray-binary counter that uses clocked inverters.

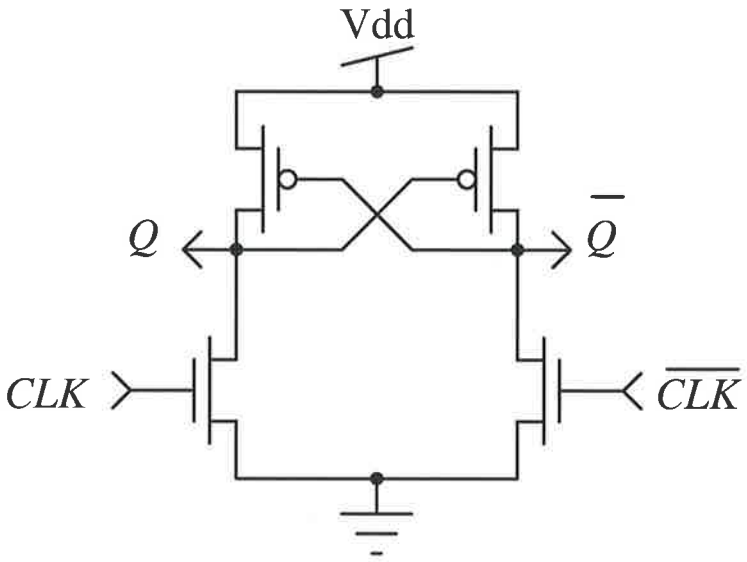

Figure 6.10. An inverter circuit using CVSL family. This inverter can be used to produce two complementary clocks and reduce the skew between CLK and $\overline{CLK}$.

in simulation and through fabrication. The static version is a low power and area efficient circuit as it is based on an optimised JK flip-flop circuit for power and silicon area. In designing the dynamic versions, simulations showed that the dynamic version proposed by Milgrome *et al.* [1992] is producing a binary sequence instead of a Gray code sequence. Furthermore, the operation of the two dynamic versions was verified through simulations. Issues related to hazards due to clock skews were addressed and a simple solution was presented. Also issues relate to the establishment of the correct initial condition in the dynamic version of the Gray-binary counter were discussed.

The concept of dual counting schemes has an interesting application in analog to digital converters specially in the multichannel Wilkinson architecture [Emery, Ericson, Britton, Smith, Frank, Young, Allen & Clonts 1997, Emery, Frank, Britton, Wintenberg, Simpson, Ericson, Young, Clonts & Allen 1997, Milgrome *et al.* 1992, Kinbara 1977], where the Gray code can be used in the generate the analog ramp signal, while the state of the counter can be easily identified without conversion by reading the binary state of the counter.

In summary, in this chapter new formulas to produce Gray and binary counting sequence to reduce power consumption at the circuit, architectural and algorithmic levels are presented. These formulas that show the relations between clock transitions and a Gray code sequence were presented and discussed. An area and power efficient implementation of the formulas in CMOS technology realising an $n+1$ bit low power Gray code counter by using static and dynamic circuits was presented and discussed. Simulation

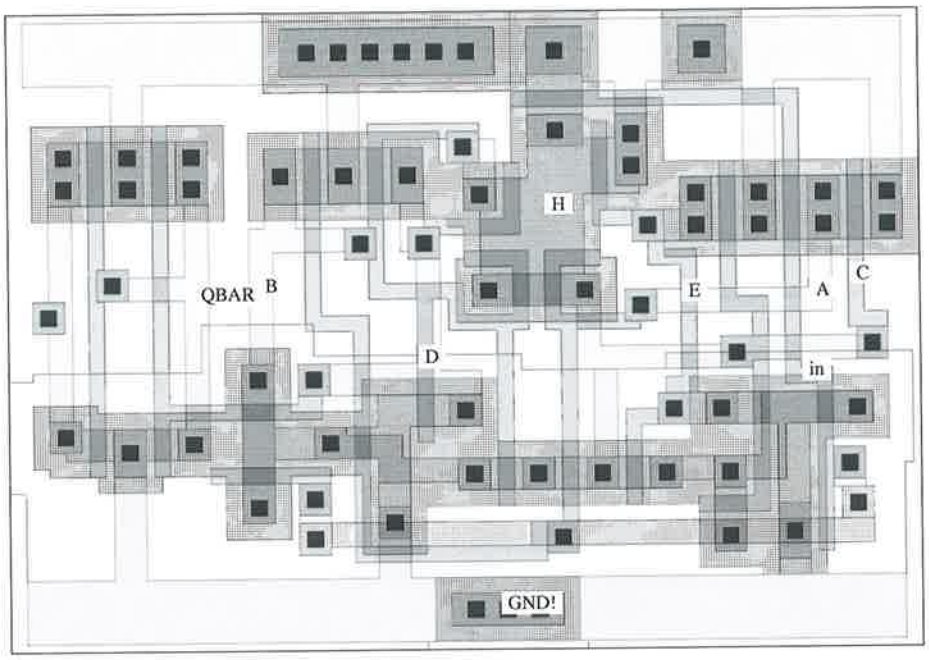

Figure 6.11. Compact layouts of the optimised JK flip-flop shown in Figure 6.2. These layouts were custom design for compactness. The transistor size of these transistors are given on the schematic shown in Figure 6.2.

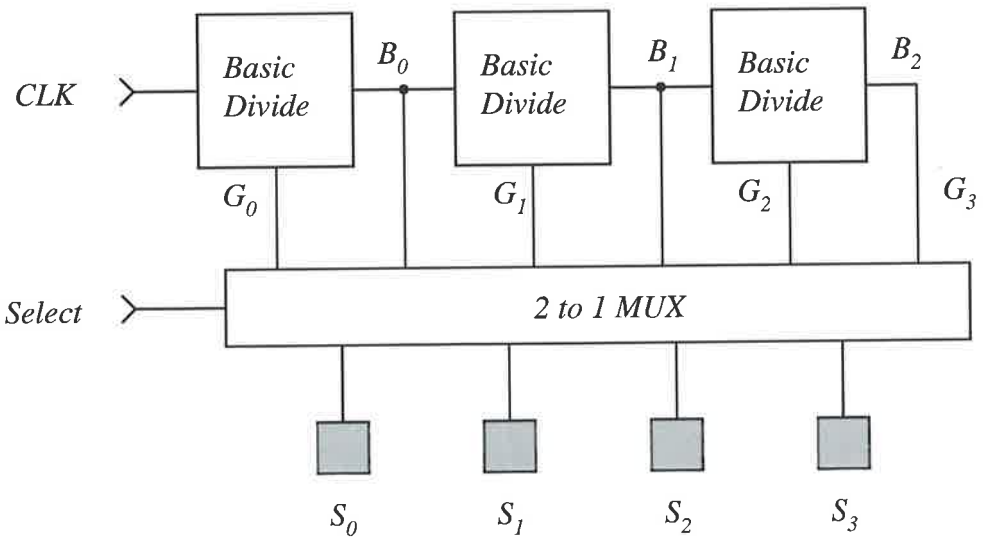

Figure 6.12. A block diagram of the fabricated 4 bit Gray – 3 bit binary counter. This setup was used used to reduce the number of output pads needed by this test structure.

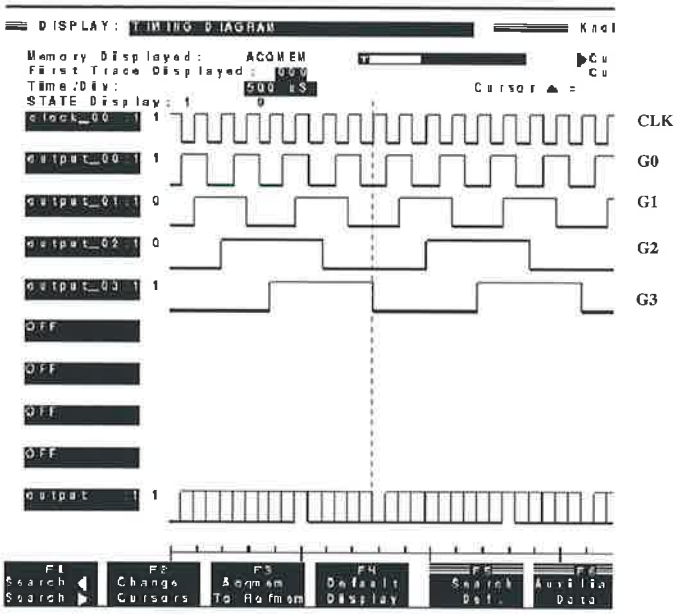

Figure 6.13. Measured results from the fabricated 4 bit Gray – 3 bit Gray-binary counter. These results show the Gray count output from the test structure (Screen dump from Tektronix 3001 GPX).

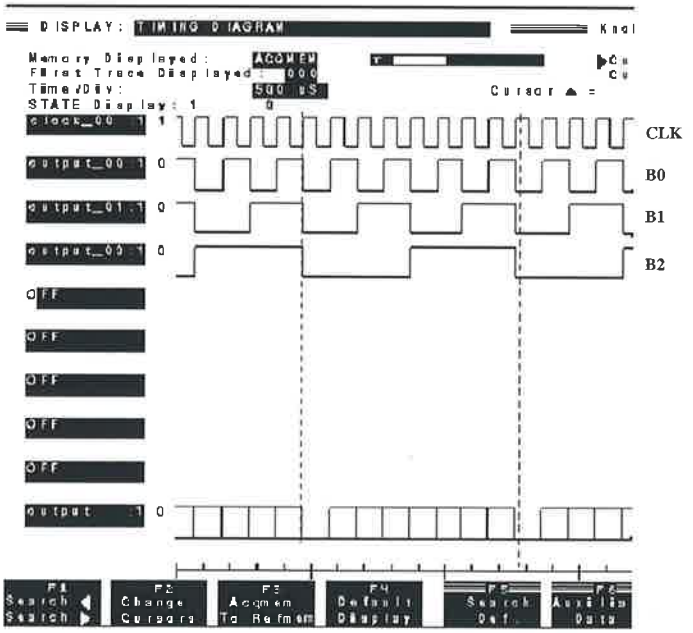

Figure 6.14. Measured results from the fabricated 4 bit Gray – 3 bit binary counter. These results show the binary count output from the test structure (Screen dump from Tektronix 3001 GPX).

results for the dynamic versions show the feasibility of a dynamic implementation of the Gray-Binary Counter.

In the next chapter the circuit level is targeted to reduce power consumption in mixed analog-digital circuit by a novel topology to convert either passive or active grounded resistors or conductances to a floating equivalent. The topology allows the implementation of very high value voltage and current controlled active floating resistors in standard low-cost CMOS technology at low power and small area.

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Chapter 7

A Novel Topology for Grounded-to-Floating Resistor Conversion

IN this chapter a new circuit topology to convert grounded resistors to an equivalent floating resistor is presented and discussed. The value of the resulting floating resistor equals the sum of the two grounded resistors. The new topology can be used to convert either passive, active grounded resistors or active grounded conductances. The new topology is used in the design of a current controlled very high value floating resistor in the range of GΩ. This was achieved by utilising the output conductance of two matched transistors operating in the subthreshold region and biased using a 500 nA current. The practicality of the new topology is demonstrated through the design of a very low frequency bandpass filter for artificial insect vision and pacemaker applications. Simulations results using Level 49 model parameters in HSPICE show an introduced THD of less than 0.25% for a 1 V_{pp} input signal in a 3.3 Volt 0.25 μm CMOS technology. Statistical modelling of the new topology is also presented and discussed.

7.1 Introduction

Resistors have a very important role in a wide variety of applications such as signal processing and neural networks, which rely heavily on the design of analog VLSI circuits. Due to the large area penalty of using passive resistors, wide spread, lack of accuracy and programmability [Voorman 1992, Coban & Allen 1994], a large number of implementations of active resistors and transconductors using MOS transistors have been discussed in literature [Cheng & Toumazou 1992, Li *et al.* 1993, Nauta 1993, Wilson & Chan 1989, Wilson & Chan 1990, Wilson & Chan 1992, Wilson & Chan 1993, Wilson & Chan 1991, Wilson & Chan 1994]. Some of these techniques exploit the MOS transistor characteristic in the triode [Nauta *et al.* 1991, Lee *et al.* 1994, Coban & Allen 1994], saturation regions [Coban & Allen 1994] and few exploit the subthreshold region of operation [Al-Sarawi 2001, Furth & Andreou 1995]. The new topology can be used to obtain low-power high-value floating resistors with high linearity and wide dynamic range.

Section 7.2 of this chapter presents and discusses the theoretical background and the implementation of the new circuit topology in standard CMOS technologies. Section 7.3, demonstrates the use of the new topology in converting voltage controlled grounded resistors to a voltage controlled floating resistor. Section 7.4, discusses the use of the new topology in the design of a current controlled very high value floating resistor. Section 7.5 presents and discusses statistical modelling of the new topology using passive resistors. Section 7.6, presents a practical example of using the new current controlled very high value resistor in the design of a current controlled differentiator circuit, which has practical use in artificial insect vision [Moini *et al.* 1997] and pacemaker applications.

In the following analysis it is assumed that the source and the back gate for the corresponding n and p type MOS transistors are connected together, unless mentioned otherwise.

7.2 A New Circuit Topology

7.2.1 Theoretical Analysis

The new topology is based on two diode connected matched transistors operating in the saturation region [Sakurai & Ismail 1992] as shown in Figure 7.1. V_x and V_y are the floating resistor terminal voltages, and $I_{in} = I_{out}$ is the current passing through the terminals. The current equation for the transistors in Figure 7.1 can be written as

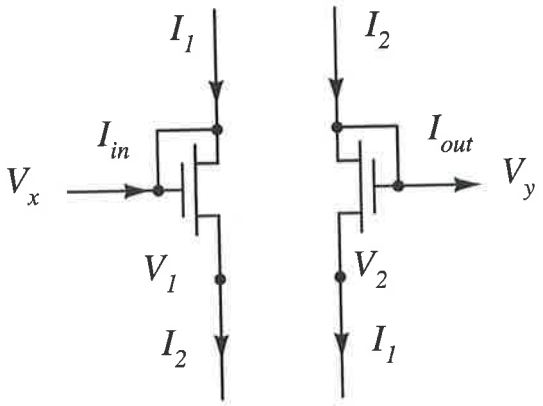

Figure 7.1. The basic MOS transistor cell. These two matched diode-connected transistors are used as the basic core elements of the topology.

$$I_1 = \frac{\beta}{2}(V_y - V_2 - V_{th})^2 \tag{7.1}$$

$$I_2 = \frac{\beta}{2}(V_x - V_1 - V_{th})^2, \tag{7.2}$$

where β is defined as $\mu_o C_{ox}(W/L)$, μ_o the carrier mobility, C_{ox} is the oxide capacitance per unit area, V_{th} is the MOS transistor threshold voltage, and W/L is the width to length ratio of the transistor. The current passing through the circuit topology can be written as

$$I_{in} = I_{out} = I_2 - I_1. \tag{7.3}$$

Substituting Equations 7.1 and 7.2 into Equation 7.3, and simplifying the results, I_{out} can be written as

$$I_{out} = \frac{\beta}{2}[(V_x - V_y) - (V_1 - V_2)][(V_x + V_y) - (V_1 + V_2) - 2V_{th}]. \tag{7.4}$$

The equivalent resistance, R_{eqv}, is defined as

$$R_{eqv} = \frac{V_x - V_y}{I_{in}} = \frac{V_x - V_y}{I_{out}}. \tag{7.5}$$

In order to achieve a circuit topology independent of the MOS transistor threshold voltage, let

$$V_1 = V_x - V_{th} + f(V_x) \tag{7.6}$$
$$V_2 = V_y - V_{th} + f(V_y). \tag{7.7}$$

The sum and the difference of V_1 and V_2 can be written as

$$V_1 + V_2 = V_x + V_y - 2V_{th} + f(V_x) + f(V_y) \tag{7.8}$$
$$V_1 - V_2 = V_x - V_y + f(V_x) - f(V_y). \tag{7.9}$$

By substituting Equations 7.8 and 7.9 in Equation 7.4, I_{out} can be written as

$$I_{out} = \frac{\beta}{2}(f(V_x)^2 - f(V_y)^2). \tag{7.10}$$

Equation 7.10 shows that the current passing through the topology is independent of the MOS transistor threshold voltage, a square function of V_x and V_y and is proportional to β.

7.2.2 Topology Implementation

A possible implementation of Equations 7.6 and 7.7, is shown in Figure 7.2. In this topology the current passing through mn_1 is mirrored by mn_2 and feeds back to the V_y terminal of mn_3 using mp_1. In a similar way, the current passing through mn_3 is mirrored by mn_4 and feeds back to the V_x terminal of mn_1 using mp_3. The relation between V_x and V_1, while assuming a passive resistor connected between V_1 and ground, can be written as

$$V_1 = R(2I_2) = \beta R(V_x - V_1 - V_{th})^2, \tag{7.11}$$

where R is the resistor value. Solving Equation 7.11 for V_1 gives two solutions, the feasible one is

$$V_1 = V_x - V_{th} + \frac{1 - \sqrt{1 + 2\beta R(V_x - V_{th})}}{2\beta R}. \tag{7.12}$$

A similar expression for V_2 can be written as

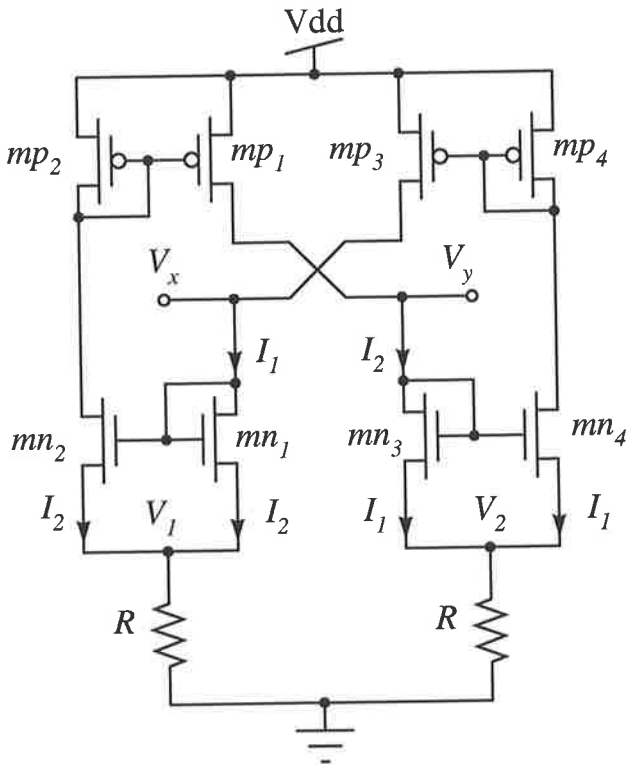

Figure 7.2. The new topology with two passive resistor connected at V_1 and V_2 and ground. This circuit diagram shows how the biasing currents for the topology is achieved and how the resistors are connected between V_1, V_2 and ground.

$$V_2 = V_y - V_{th} + \frac{1 - \sqrt{1 + 2\beta R(V_y - V_{th})}}{2\beta R}. \tag{7.13}$$

Comparing Equations 7.12 and 7.13 with Equations 7.6 and 7.7, respectively, $f(V_x)$ and $f(V_y)$ can be written as

$$f(V_x) = \frac{1 - \sqrt{X}}{2\beta R} \tag{7.14}$$

$$f(V_y) = \frac{1 - \sqrt{Y}}{2\beta R}, \tag{7.15}$$

where

$$X = 1 + 2\beta R(V_x - V_{th}) \qquad \text{and} \qquad Y = 1 + 2\beta R(V_y - V_{th}).$$

Substituting the values of $f(V_x)$ and $f(V_y)$ from Equations 7.14 and 7.15 in Equation 7.10, I_{out} can be written as

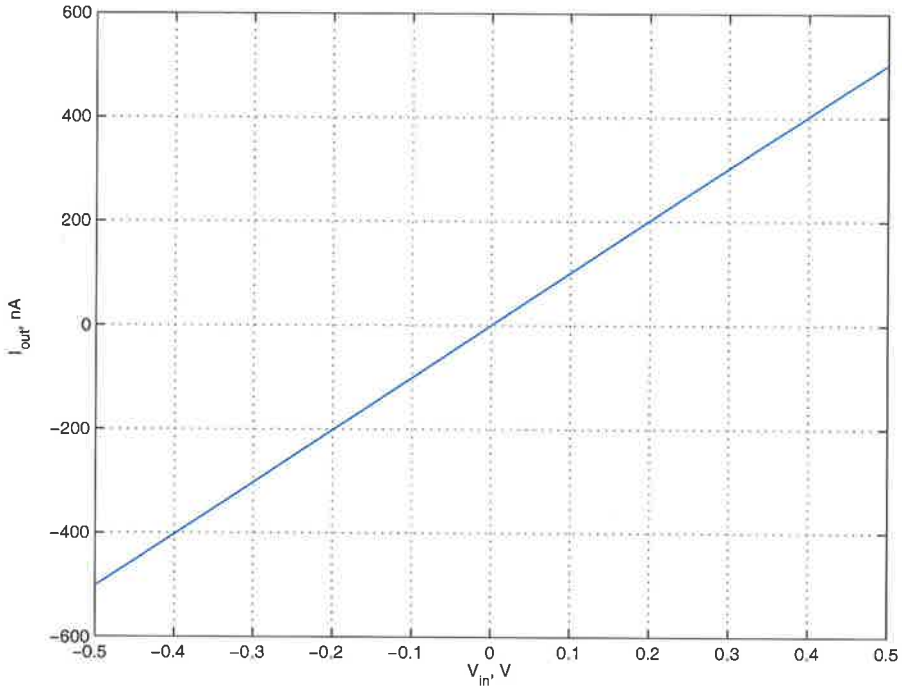

Figure 7.3. The simulation results of the new circuit topology with two 1 MΩ passive resistors connected at V_1 and at V_2 of Figure 7.2. These simulations show that the equivalent floating resistor between V_x and V_y is twice the value of the passive resistors connected to V_1, V_2 and ground. The bias voltage used at V_x is $V_B + V_{in}/2$ and V_y is $V_B + V_{in}/2$, where V_B is a DC bias voltage and V_{in} is the input voltage.

$$I_{out} = \frac{1}{8\beta R^2}\left[(1-\sqrt{X})^2 - (1-\sqrt{Y})^2\right]. \tag{7.16}$$

Assuming $\sqrt{X} \gg 1$ and $\sqrt{Y} \gg 1$, which is a valid assumption for large values of R, then Equation 7.16 is reduced to

$$I_{out} = \frac{1}{8\beta R^2}(X - Y). \tag{7.17}$$

Substituting the values of X and Y in Equation 7.17, with $V_x = V_B + V_{in}/2$ and $V_y = V_B - V_{in}/2$, Equation 7.17 is reduced to

$$I_{out} = \frac{V_{in}}{2R}. \tag{7.18}$$

An expression for the equivalent resistance R_{equ} can be written by substituting Equation 7.18 into Equation 7.5, as given by

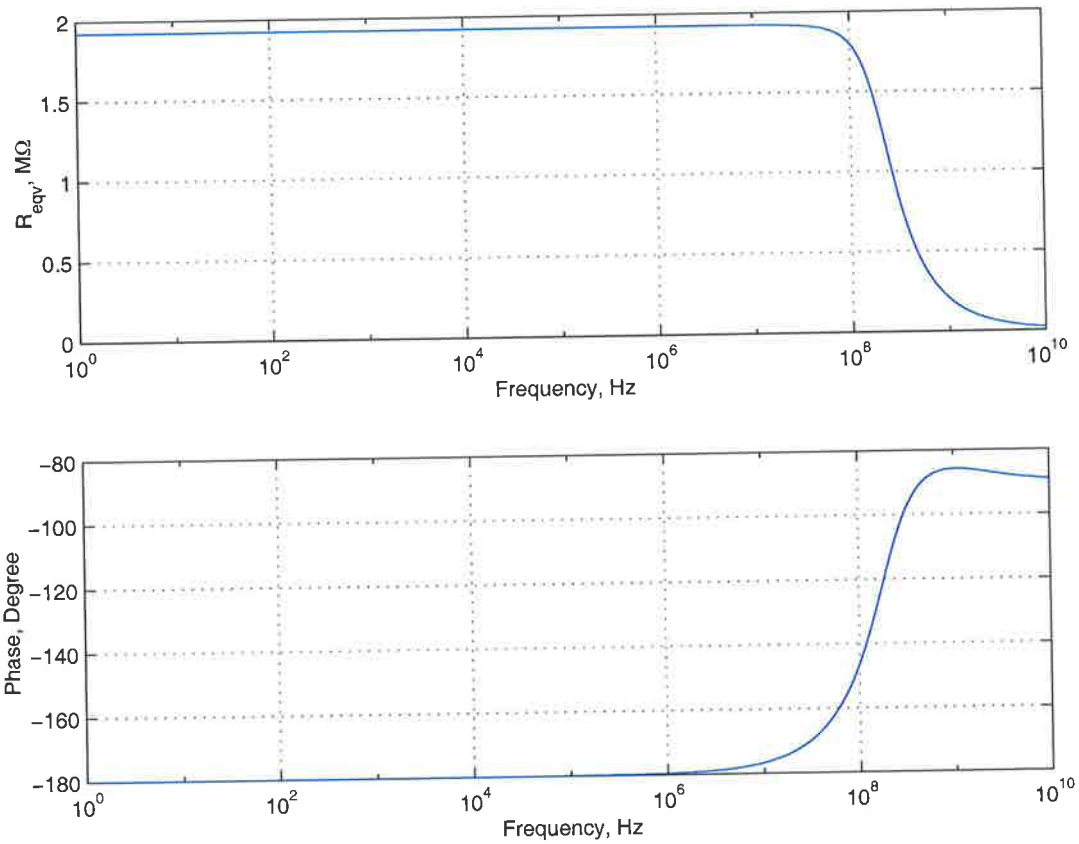

Figure 7.4. The frequency response of the new circuit topology with two 1 MΩ passive resistors connected at V_1 and V_2. These simulations show the frequency response of the floating resistor with passive resistors and show that a frequency response that extends to hundreds of MHz.

$$R_{eqv} = \frac{V_{in}}{I_{out}} = 2R. \tag{7.19}$$

Equation 7.19 shows that the equivalent floating resistor value is independent of the process model parameters and the MOS transistor's threshold voltage. Equation 7.19 also shows that the V-I relation of this topology resembles an ideal resistor with an equivalent floating resistor equal to the sum of the grounded resistors.

The circuit shown in Figure 7.2 was simulated with the length and width of all transistor sizes are set to 12 μm as shown in Figure 7.3. These simulations were conducted using HSPICE simulator with Level 49 process model parameters for 0.25 μm single poly, 5 metal n-well process. The simulated I-V characteristics with passive input resistors show a very wide dynamic range and very linear characteristics. The frequency response of the topology using passive resistors is shown in Figure 7.4. The AC simulations show a

frequency response that extends to the MHz range with constant resistance value. The introduced *total harmonic distortion* (THD) by the new topology for 1 V_{pp} input signal is less than 0.25 % as shown in Figure 7.5.

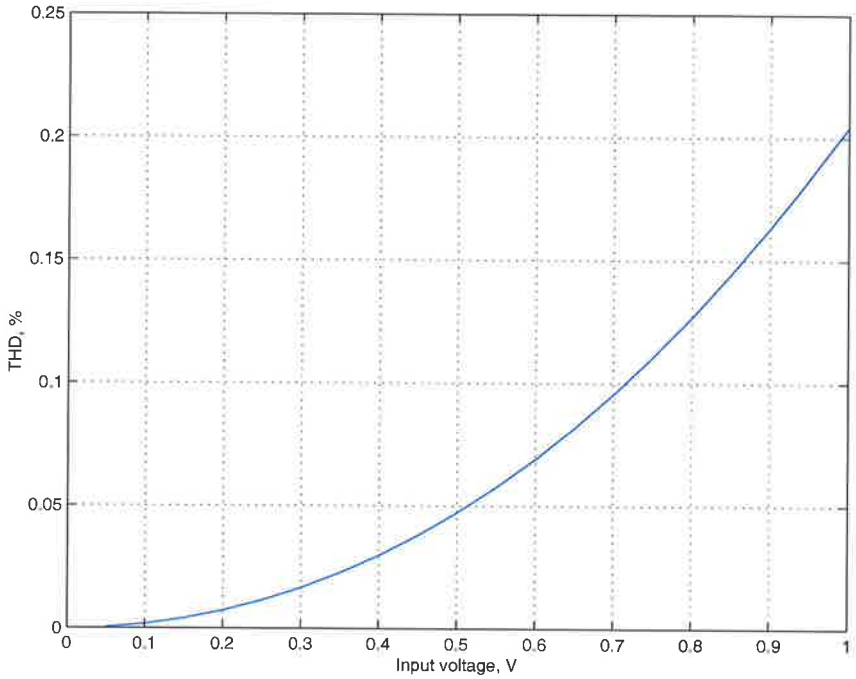

Figure 7.5. The total harmonic distortion (THD) introduced by the new circuit topology as function of the input signal amplitude. These simulations show that the THD of the topology with the increase in the input signal amplitude.

7.3 Converting a Grounded Resistor to a Floating Resistor

The analysis presented in Section 7.2 is still also valid when the passive resistors are replaced by active grounded resistors or conductances. As an example, the grounded resistor [Sliva-Martinez *et al.* 1990] shown in Figure 7.6 is used. This grounded resistor was chosen because of its simplicity, very high linearity and controllability. Other grounded resistors such as the ones described by Wilson & Chan [1989] and Wang [1990] can also be used.

The resistor shown in Figure 7.6 was simulated using the previously mentioned technology, with W_1/L_1 = 48 μm / 6 μm and W_2/L_2 = 6 μm / 48 μm. The control voltage V_c was swept from 1 to 3.5 Volts in a 0.5 Volts steps, while V_o was swept from 0 to 5 Volt

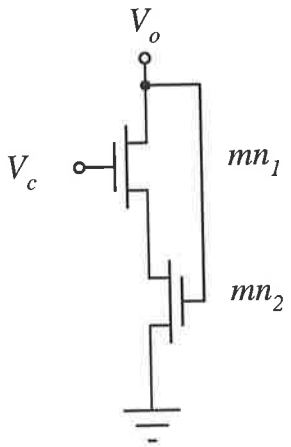

Figure 7.6. A very linear grounded resistor. The resistor value is function of transistor sizes and the control voltage V_c. This type of resistor was discussed in details in Section 2.2.

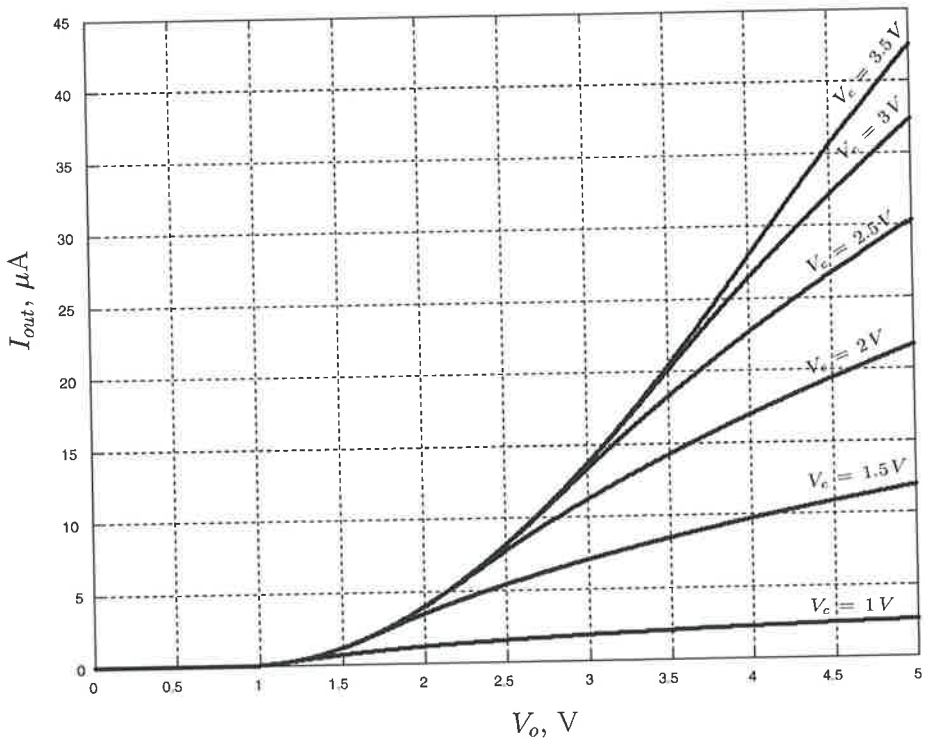

Figure 7.7. Simulation results of the grounded resistor shown in Figure 7.6. These simulations were conducted with the control voltage V_c swept from 1 to 3.5 Volts in 0.5 Volts steps. These simulations show that the active grounded resistor value between V_o is linear.

for every V_c, as shown in Figure 7.7. The resistor shown in Figure 7.6, was integrated in the new topology as shown in Figure 7.8, and simulated with all transistor sizes in the topology and the grounded resistors are kept as before. The simulation results for the new floating resistor are shown in Figure 7.9. The figure shows that the resultant voltage controlled floating resistor is also very linear.

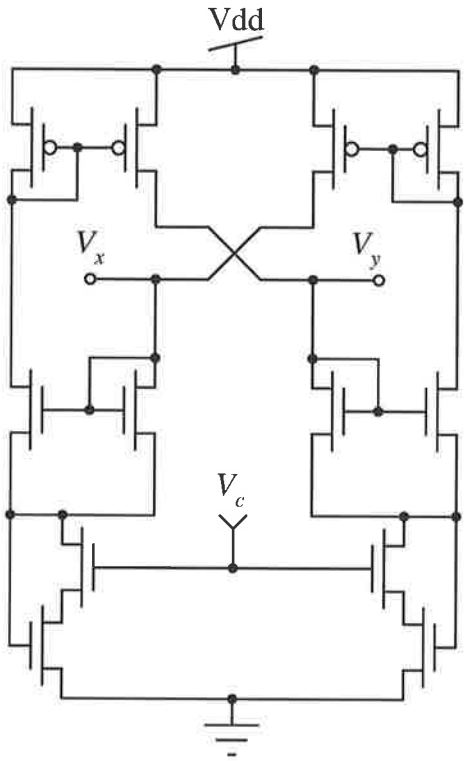

Figure 7.8. A voltage controlled floating resistor This schematic shows how the topology shown in Figure 7.2 can be used to implement a voltage controlled resistor by replacing each passive resistors with the voltage controlled grounded resistor shown in Figure 7.6. The control voltage V_c can be used to control the floating resistor value.

7.4 Very High Value Floating (VHVF) Resistor

A VHVF resistor can be designed using the previous topology if starting with very high value resistors or output conductances. To demonstrate the technique with a high output conductance configuration, the output conductance of the MOS transistor in the saturation region is used as shown in Figure 7.10. A MOS transistor biased with small value current provides a very high output conductance in the range of GΩ. The main concern

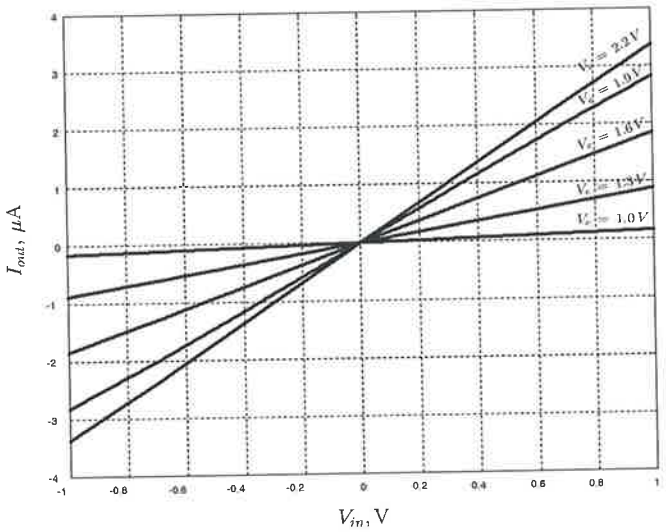

Figure 7.9. Simulation results of the new voltage controlled floating resistor shown in Figure 7.8 These simulations show the value of the current passing through the floating resistor at different control voltages. The control voltage V_c was swept from 1 to 2.2 Volts in a 0.3 Volts steps. The current passing through the floating resistor is directly proportional to the voltage across the floating resistor terminals V_x and V_y.

about using the MOS transistor output conductance is that it depends on the channel length modulation parameter λ, which is defined [Zarabadi *et al.* 1994] as

$$\lambda = \frac{\sqrt{\frac{\epsilon_{si}}{qN_{eff}(V_{DS}-V_{d,sat})}}}{L}, \tag{7.20}$$

where drain saturation voltage $V_{d,sat}$ is define as $V_{gs} - V_{th}$, ϵ_{si} is the dielectric constant of silicon, N_{eff} is the substrate doping density, q is the electron charge, V_{DS} is the drain to source voltage and L is the transistor length. From Equation 7.20, it is clear that λ is a process dependent parameter and it is not a favourable parameter to use in circuit design. However, such dependence does not exclude λ as a design parameter [Steyaert *et al.* 1991], and in this case the dependence on λ can be compensated for by the current programmability of the VHVF resistor. Furthermore, other high output conductance current configuration can be used instead of the two transistor current mirrors. Using the simple transistor model that includes the channel length modulation effect, the output conductances, g_d of mn_5 or mn_6 at constant gate to source voltage is given by

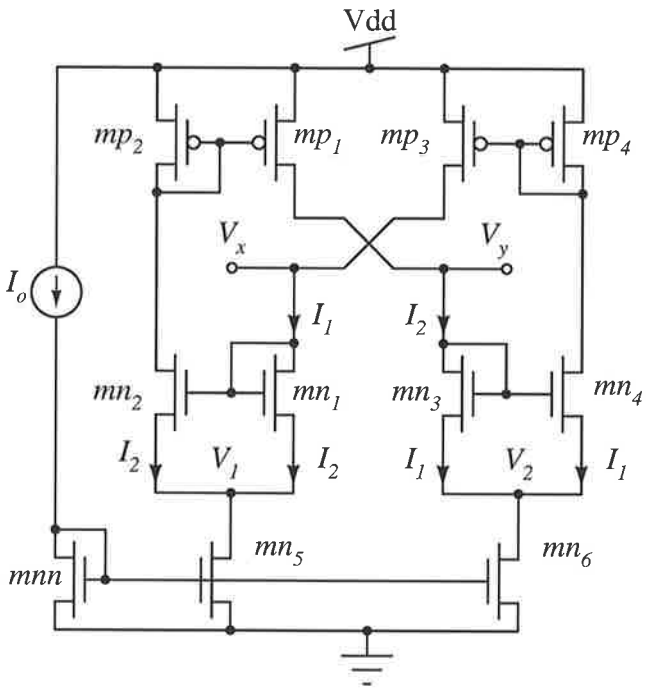

Figure 7.10. A very high value current controlled floating resistor. This schematic shows how the output conductance of MOS transistor operating in the saturation region of operation is used to implement the value high value floating resistor. The output conductance of the transistor is controlled using the bias current I_o, thus controlling the floating resistor value.

$$g_d = \frac{\lambda I_d}{(1 + \lambda V_{ds})} \simeq \lambda I_d. \tag{7.21}$$

For an $I_d = 1$ μA and $\lambda = 1$ mV^{-1} (extracted from the Level 49 model parameters at 1 μA bias current), the equivalent floating resistor is 2 GΩ.

The circuit shown in Figure 7.10 was simulated using a large value of reference current in the μA range, to demonstrate the circuit performance when transistors are operating in the saturation region. The simulation results, with the reference current I_o was swept from 7.5 μA to 20 μA in a 2.5 μA steps, are shown in Figure 7.11. The circuit shown in Figure 7.10 was re-simulated using a small bias current in the nA range, to ensure that all transistors are operating in the subthreshold region of operation. The simulation results, with I_o was swept from 500 nA to 1 μA in a 100 nA steps, are shown in Figure 7.12. Figures 7.11 and 7.12 show that the resistor exhibits very linear characteristics in saturation and subthreshold regions of operation. The frequency response of the very high value resistor is shown in Figure 7.13. The simulations show that the bandwidth of the active

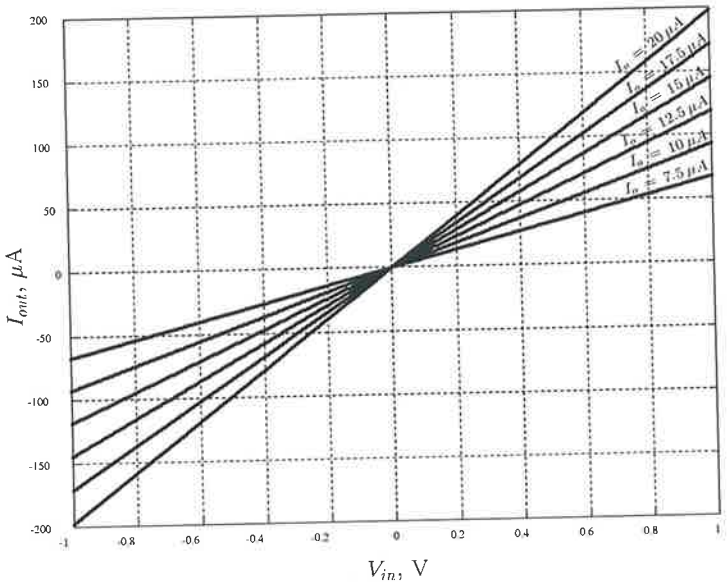

Figure 7.11. Simulation results of the current controlled very high value floating resistor with large reference current values. These simulation were conducted with the reference current I_o was swept from 7.5 μA to 20 μA in 2.5 μA steps. The simulation shows the current passing through the topology is function of the controlling current. The simulations also show that using these values of bias current the resistor value can be adjust from 5 kΩ up to 16 kΩ.

floating resistor is reduced compared to the passive floating resistor case presented earlier with constant resistance. The reduction significance is application dependence. For the targeted applications the bandwidth is still within the operational frequency range.

7.5 Statistical Modelling

To evaluate the performance of the circuit topology discussed in Section 7.2 Monte Carlo analysis was performed. This analysis provides an insight into the topology sensitivity to process parameters. This section addresses issues related to (i) threshold voltage mismatch effect on the resultant equivalent floating resistor and (ii) transistor dimension effect on the equivalent resistor value. These effects are evaluated using Level 49 model parameters for an industrial 0.25 μm CMOS process. In the following simulations two 1 MΩ passive resistors are used as input for the topology and all the transistors dimensions were set to 12 μm $\times$ 12 μm.

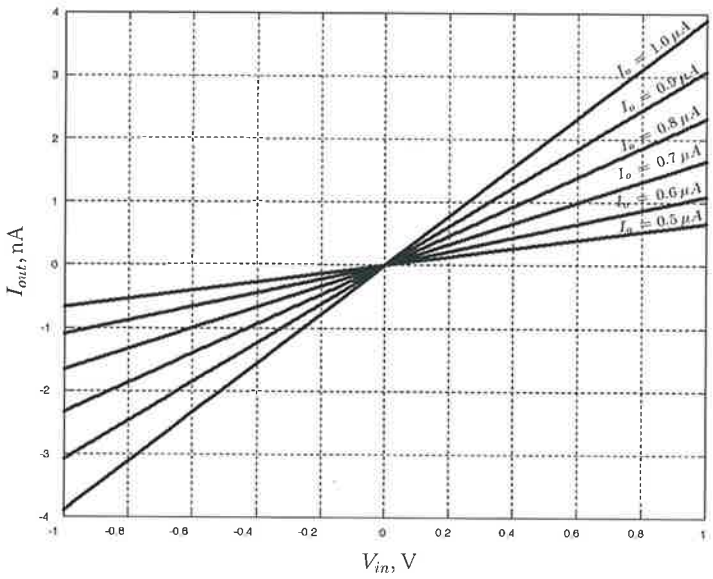

Figure 7.12. The simulation results of the very high value floating resistor with small reference current values. These simulations were conducted with the reference current I_o was swept from 500 nA to 1 μA in a 200 nA steps. These simulations also show that the current passing through the topology is function of the controlling current. These simulations also show that using these values of bias currents the resistor value can be adjusted between 2.5 MΩ and 1.25 GΩ.

Monte Carlo analysis in HSPICE simulator is used to show the effect of threshold voltage mismatch on the resistor value. The simulation was conducted by adding a small voltage to the threshold voltage calculated by the simulator. A Gaussian distribution with zero mean and a 5-millivolt standard deviation was used. The 5 mV value was chosen based on the relation between transistors area and threshold voltage mismatch measurements given by Forti & Wright [1994] and presented in Section 3.2.2. The measured mean value of the equivalent floating resistor is 1.97 MΩ and the standard deviation is 98 kΩ. The programmability of the resistor can be used to fine tune the resistor value.

Figure 7.14 shows the effect of transistors sizes on the effective value of the floating resistor. Two 500 kΩ resistors are used as inputs for the topology. The 500 kΩ resistor value was arbitrary chosen and not for any specific reason. The width and length of all the transistors in the topology were swept from 1 μm to 10 μm in 0.5 μm steps. These simulations show that the transistors sizes have an effect on the effective floating resistor value. This effect can be minimised by selecting wide transistors with moderate lengths. Furthermore, the temperature effect on the topology was evaluated. When the

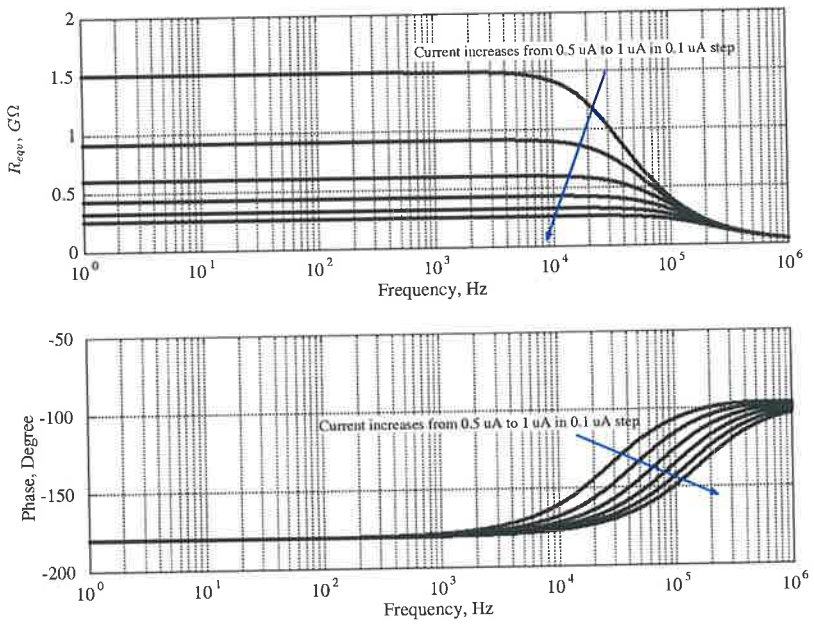

Figure 7.13. The frequency response of the very high value floating resistor with the small value of reference current. These simulation were conducted with the reference current I_o swept from 500 nA to 1 μA in 200 nA steps. These simulations show the bandwidth of operation of floating resistor is limited to a few kilohertz and does vary as function of the reference current.

temperature was swept from -50 °C to 100 °C in 12.5 °C steps. The average resistor value measured from simulation was 1.05 MΩ with a standard deviation of 7.3 kΩ, minimum value of 1.04 MΩ, and a maximum value of 1.06 MΩ. These results demonstrate the robustness of the topology against temperature and process variations.

7.6 A Design Example

To demonstrate the use of the new very high value resistor in a practical design example, the new topology was used in the design of a low frequency, current controlled, *bandpass filter* which presents a major problem in motion detection systems because of the challenging requirements [Moini *et al.* 1997]. The bandpass filter requirements are: (*i*) 100 Hz bandwidth, (*ii*) the first cut off frequency at 10 Hz while the second at 100 Hz, (*iii*) very high gain, (*iv*) very small area, (*v*) moderate to low power consumption. A bandpass filter with these requirements can be designed as shown in Figure 7.15. The lower cut-off

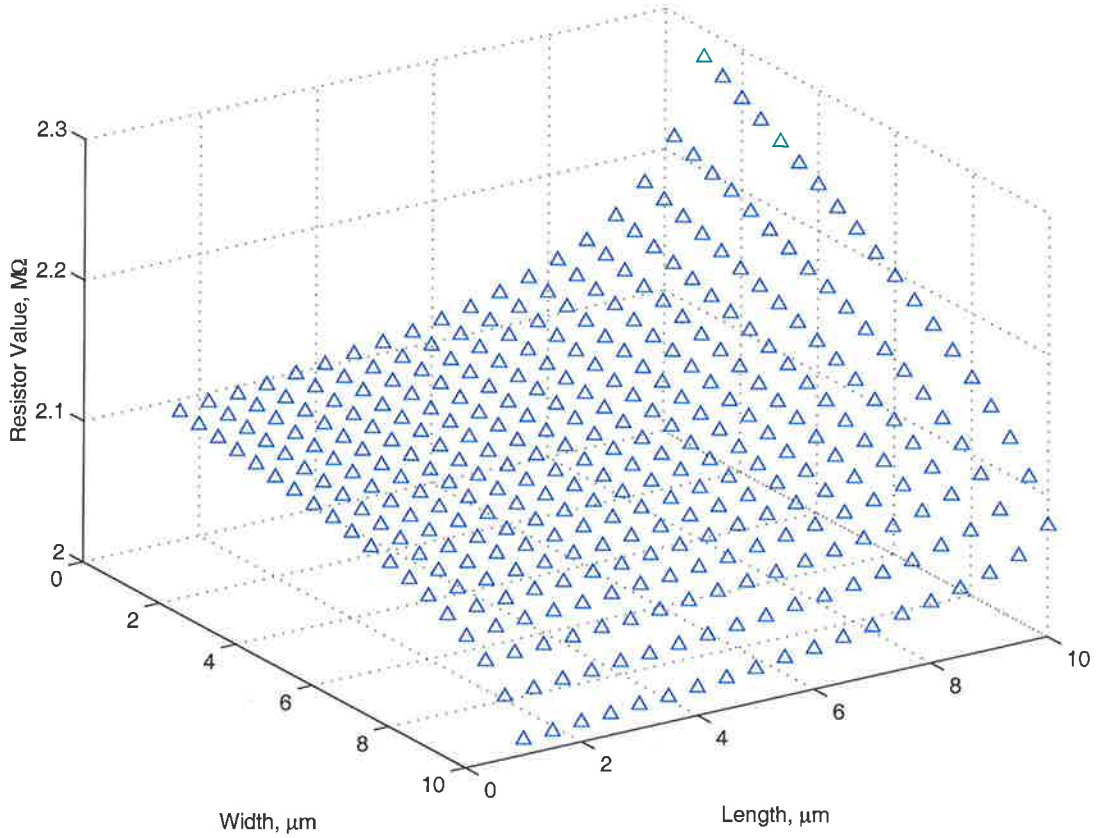

Figure 7.14. The effect of transistor width and length on the circuit topology effective floating resistance. These simulation were conducted using two passive 1 MΩ resistors as inputs to the topology, then the width and length of all the transistors in the topology were swept from 1 μm to 10 μm in 0.5 μm steps. These simulations show that the longer the transistors the higher the floating resistor value see between V_x and V_y. This is due to the added conducts of these transistors to the input resistor value.

frequency of the filter is set by the differentiator configuration and upper cut-off frequency is limited by the opamp gain, which is function of the opamp bias current. The voltage at nodes V_1 and V_2 can be written as

$$V_1 = V_{in}\frac{sRC}{1+sRC} + V_{out}\frac{1}{1+sRC} \tag{7.22}$$

$$V_2 = V_{out}\frac{1}{1+sRC}. \tag{7.23}$$

The relation between the differential inputs V_1 and V_2 and V_{out} is given as

$$V_{out} = A(s)(V_2 - V_1). \tag{7.24}$$

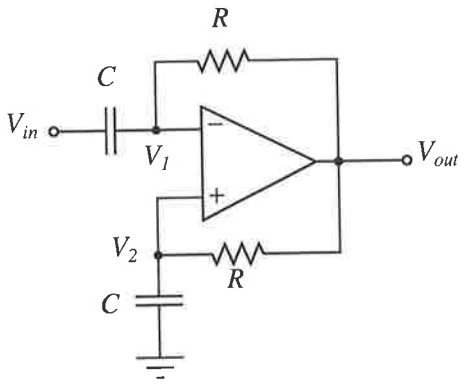

Figure 7.15. A circuit diagram of a low frequency differentiator circuit. This circuit was used to test the presented, once using two ideal resistors and another using the presented topology with two current controlled conductances – two transistors operating in the saturation region of operation.

Substituting Equations 7.22 and 7.23 in Equation 7.24, the circuit transfer characteristics can be written as

$$H(s) = -A(s)\frac{sRC}{1+sRC}, \tag{7.25}$$

where $A(s)$ is the operational amplifier gain.

Two versions of the differentiator shown in Figure 7.15 were simulated at 5 Volt supply. The first circuit uses a passive resistor, while the second uses VHVF resistors. The frequency responses of the two versions are shown in Figure 7.16. In addition, the transient analysis simulation results for the two versions are shown in Figure 7.17. The difference in the simulation results between the two versions of the differentiator is due to a larger resistance value of the VHVF resistor and the parasitic capacitance associated with the VHVF resistor terminals.

7.7 Summary

A new circuit topology to convert grounded resistors to a floating resistor is presented and discussed. The use of the new topology in the conversion of passive, voltage and current controlled resistors was demonstrated in the design of a current controlled very high value resistor in GΩ the range. The floating resistor is electrically programmable, has a small number of transistors and consumes very small amount of current from the power supply. The sensitivity of the circuit against threshold voltage mismatch was demonstrate using

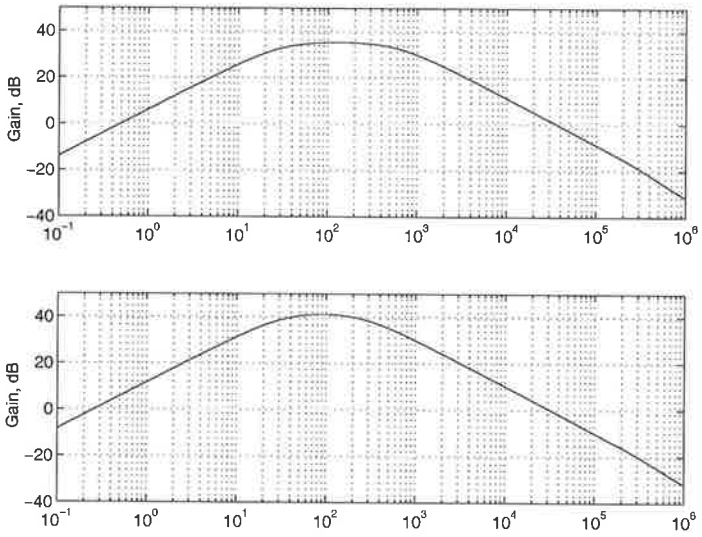

Figure 7.16. The frequency response of the bandpass filter circuit The upper panel shows the simulation results when an ideal resistor was used in the bandpass filter simulation. The lower panel shows the filter response when the passive resistors are replaced by current controlled floating resistors. The slight difference between the two simulations is due to the parasitics associated with the active floating resistors that did affect the frequency response.

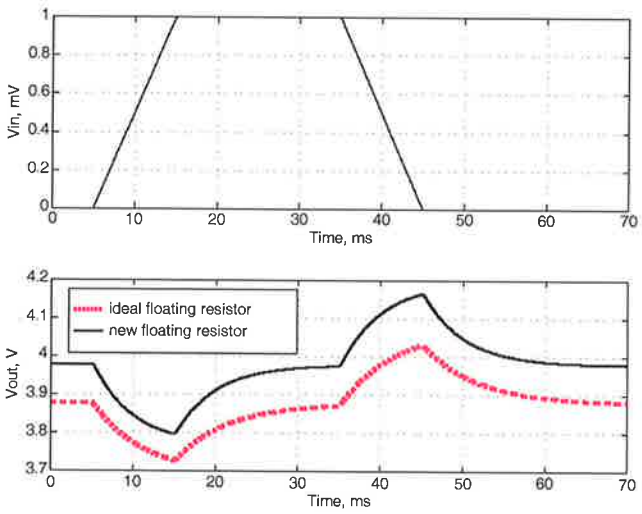

Figure 7.17. The simulation results of the bandpass filter circuit for an input pulse. The upper panel shows an input pulse has a 10 ms raise and fall time and was delayed by 5 ms. This pulse was used as an input to the filter. The lower panel shows two output simulation waveforms. The dotted line is the response when an ideal resistor was used in the simulation. The solid line is the simulation results when using the new current controlled floating resistor.

Monte Carlo analysis in HSPICE. The practicality of the new resistor is demonstrated through the design of a very low frequency bandpass filter for pacemaker and artificial insect vision applications.

In this chapter we have demonstrated that design techniques at the circuit level can reduce power in mixed signal circuits in an area efficient design that are robust to process and temperature variations. In the next chapter the circuit level will be further targeted to reduce power of the overall system by shutting down subsystem components when they are not needed. This is achieved by using a new controlled current bleeding technique to design circuits that enable the transponder part of a RFID system to either start or come-up in reply mode – the transponder starts to send information, or program mode – the transponder is set up to receive information and ready to be programmed, depending on a duration of a pulse interruption in the passive transponder supply voltage.

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Chapter 8

Program Mode Detection Circuits

IN some systems, there is a need to design circuits that serve specific purpose and deliver functions that are not common in mixed signal systems, such as the case in RFID systems. One way to reduce power in these systems is to use a circuit that *turns on* the transponder part of the system upon the reception of a coded interrogation signal. In this chapter a new technique, called bleeding is devised. This technique is used in the design of an application specific integrated circuit (ASIC) that can be used to act as a turn-on circuit in conjunction with other circuitry or to enable the transponder part of an RFID system to operate in either *reply* mode or *program* mode. The later circuit is referred to in this work as Program Mode Detection PMD circuit.

The new technique is based on the use of two dynamic analog memory cells configured in a way that one operates as a master cell, while the second as a slave cell. These configurations are used to control the start-up behaviour of the *program mode detection circuit*. A number of PMD circuits with emphases on the power performance circuit and area are presented. Measurements from fabricated designs demonstrate the principle of operation of the PMD circuits in an RFID environment context.

8.1 Introduction

This chapter discusses new techniques to design program mode detection circuits (PMD) that are needed in radio frequency identification (RFID) system. The interest in this circuit did arise as a result of interaction with the research sponsoring company – *Integrated Silicon Design Pty. Ltd.* (ISD Pty. Ltd.). The function of these circuits is to provide a digital output signal in response to an interruption period in the circuit supply voltage. The circuit can be thought of as a delay-to-digital conversion or time-to-digital conversion. However, the unique feature of the PMD circuit is that the supply voltage of the circuit is also used as the input. Up to the author knowledge such circuit functionality is not presented in the literature. In stead, circuits with partial functionality are presented in the literature. Circuits such as time-to-delay converter (TDC) [Choi 2002, Baschirotto *et al.* 1998], which is commonly used phase locked loop (PLL) design, have separate input and supply terminals. However, the design and applications of the TDC circuit are completely different from the PMD circuit discussed in this chapter.

The initial research on this circuit was conducted by ISD Pty. Ltd. as part of their ISD9660 transponder chip. Through interaction with company, it was found that the circuit presents a challenge in understanding its operation during supply voltage transients. This challenge arises from a voltage storage at some of the circuit internal nodes during supply voltage collapse which did cause the circuit to malfunction depending on the duration of the supply voltage interruption period. To overcome the memory effect at some of the circuit internal nodes a new principle called *bleeding* is devised in this chapter. The discussion of the PMD circuit is presented in terms of versions, as the first and the second versions of the circuit were designed by the company and commonly referred to by the company in terms of versions. It was therefore decided to maintain the names, as this made it easier to discuss previous versions of the PMD circuit with the company and simplified referencing the to initial work done by the company.

This chapter is organised as follows: Section 8.2 presents an overview of the ISD9664 transponder developed by ISD Pty. Ltd. This section emphases the context where and how the PMD circuit is used in a RFID system. Section 8.3 presents background research on the PMD circuit. Section 8.4 presents the bleeding principle and its application to PMD circuit design. Section 8.5 presents and discusses experimental work for one of PMD circuits discussed in Section 8.4.

8.2 ISD9664 Chip

The mixed analog-digital processing part of the ISD Pty. Ltd. transponder is called ISD9664 chip. The first 3 letters of the name are taken from the company name, 96 is the storage capacity of chip in bits, and 64 is the number of externally programmable bits. A simplified block diagram of the ISD9664 chip is shown in Figure 8.1. A detailed block and circuit diagrams of the transponder are described in [Cole & Grasso 1993]. A brief description of ISD9664 chip is as follows:

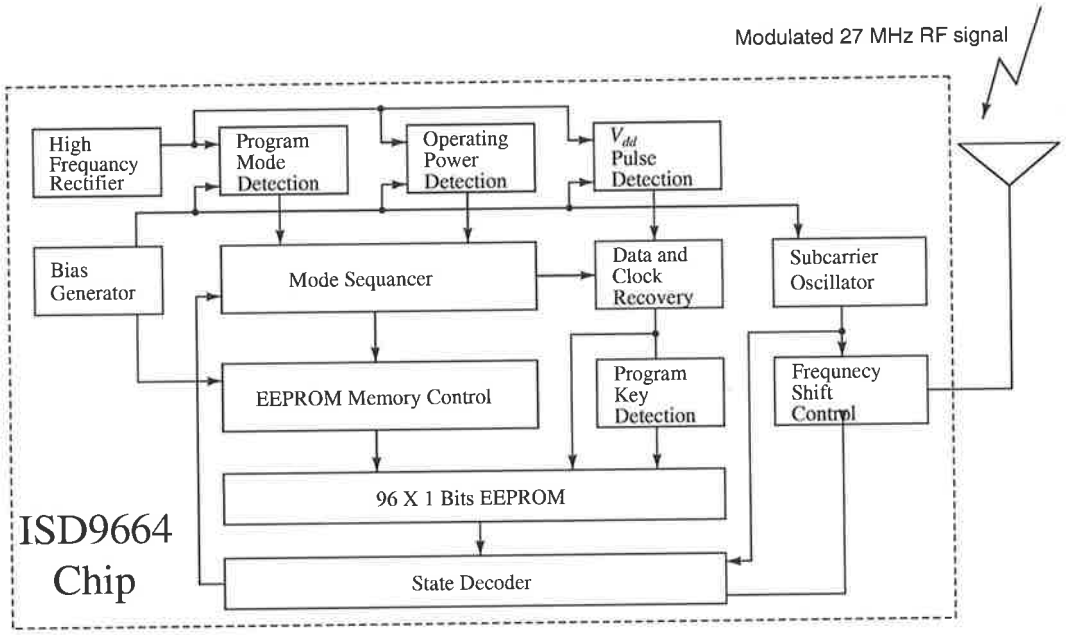

Figure 8.1. A simplified block diagram of the ISD9664 chip. This block diagram does not show all the connections between all the modules, instead it shows all the necessary connections to present the context of where program mode detection circuit fits in the transponder part of an RFID system.

- *High Frequency Rectifier:* This is a RF full-wave rectifier circuit that generates the required supply voltage for the chip operation.
- *Operating Power Detection:* This circuit enables the supply voltage for the whole chip when the rectified voltage exceeds a predefined voltage.
- *Program Mode Detection:* This circuit puts the transponder in either program or reply mode of operation depending on the duration of an interruption period of the supply voltage.

- *V_{dd} Pulse Detection:* This circuit detects any short pulse interruption on the chip supply voltage. The duration of these pulses determines whether the input data correspond to logic '0' or '1'.
- *Mode Sequencer:* This circuit provides the needed control signals during the program and reply modes of operation.
- *Data and Clock Recovery:* This circuit in conjunction with the V_{dd} Pulse Detection circuit recovers data and clock signal through detecting interruptions in the supply voltage.
- *EEROM Control:* This circuit generates the needed control signals to the EEROM circuit during the read and write modes.
- *Program Key Detection:* This circuit enable the programming of the EEROM when it receives a certain data sequence.
- *96 × 1 bits EEROM:* This is a 96 bit EEROM with a serial data interface.
- *State Decoder:* This is an address generator circuit.
- *Frequency Shift Control:* This is a frequency modulator circuit.
- *Subcarrier Oscillator:* This circuit generates the needed carrier frequency for the frequency shift control and the control signals for the state decoder circuit.
- *Bias Generator:* This circuit generates all the analog bias signals needed for the operation of the Operating Power Detection, Program Mode Detection, V_{dd} Pulse Detection, EEROM and the subcarrier oscillator circuits.

The operation of the transponder can be described as follows: when the transponder is interrogated by a 27 MHz RF signal, the transponder starts in reply mode – the transponder starts to send its identification code. If the interrogating RF signal is interrupted for a short period of time in the order of 200 μs, the transponder comes-up in program mode – the transponder is ready to be programmed. The data is read by the transponder through interruptions in the interrogating RF signal – that are translated into depressions in the transponder supply voltage. These depressions are detected by the V_{dd} Pulse Detection circuit. A logic '1' is passed to the transponder by depressing the supply voltage for a short period of time – 10 μs, while a logic '0' is passed by depressing the supply voltage for a longer period of time – 50 μs. Before data is written to the EEROM, the transponder has to receive an activation code sequence to enable programming the EEROM and

to prevent spurious overwriting of the EEROM contents by electrical interference. If the supply voltage is interrupted for a period of time more than 500 μs the transponder comes up in reply mode.

8.3 Early work on the PMD circuit

The principle of operation of the PMD circuit can be described as follows: when the supply voltage of PMD circuit rise or fall slowly (275 V/s) the circuit should come-up in reply mode, also if the supply voltage is interrupted for a period of time in the order of 500 μs the circuit should come-up in reply mode. If the circuit supply voltage was interrupted for a short period of time in the range of 200 μs the circuit should come-up in program mode. Furthermore, if the circuit supply voltage was interrupted for a long period of time in the range of 500 μs while the circuit is in program mode, the circuit should come up in reply mode. All the possible modes of operation as function of the supply voltage interruption periods are represented by the waveform shown in Figure 8.2. This waveform was used to test the operation of the PMD circuits presented in this Chapter. The following subsections discuss previous work done on the PMD circuit.

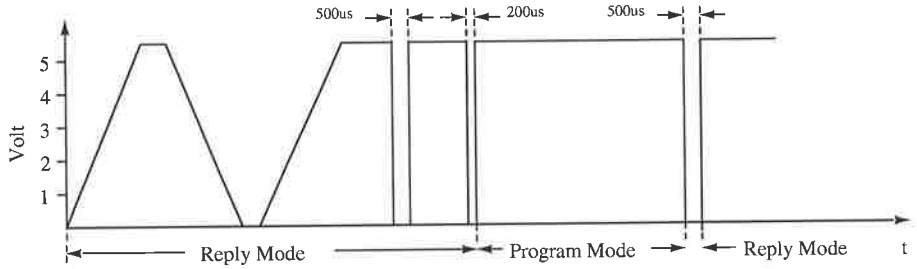

Figure 8.2. Test waveform for the PMD circuit. This waveform shows all possible supply voltages that a PMD circuit can go through. The 275 V/s slew rate and interruption periods were decided upon through discussion with the sponsoring company.

8.3.1 Early Program Mode Detection Circuit

The first version – Version-1 – of the PMD circuit [Cole & Grasso 1993] is simply a pair of cross coupled nMOS inverters with differently sized pMOS transistors loads. These loads are biased using a diode connected pMOS transistor connected to ground through a n-well resistor, as shown in Figure 8.3. The *pn* junction diode is built using a floating p-well. The operation of this circuit can be described as follows: at power-on, V_{bp} establishes

its voltage slightly more than a transistor threshold voltage below the supply voltage, hence the output of the inverter with the longest transistor length will be low, V_{or}. Thus, the other inverter output, V_{ol}, follows the supply voltage. This action is reinforced by any voltage drop across D_1 and the time needed for node V_c to charge to V_{bp} voltage. If the supply voltage is slowly decreased or interrupted for 500 μs, C_1 should discharge through the leakage current of D_1. This state of the flip-flop will always be referred to as reply mode. On the other hand, if the supply voltage is interrupted for a short period of time in range of 200 μs, node V_c should hold its potential. So, during the supply voltage restoration, node V_{or} follows the supply voltage and forces node V_{ol} to go low – program mode. By re-interrupting the supply voltage for a 500 μs, the circuit should come up in reply mode.

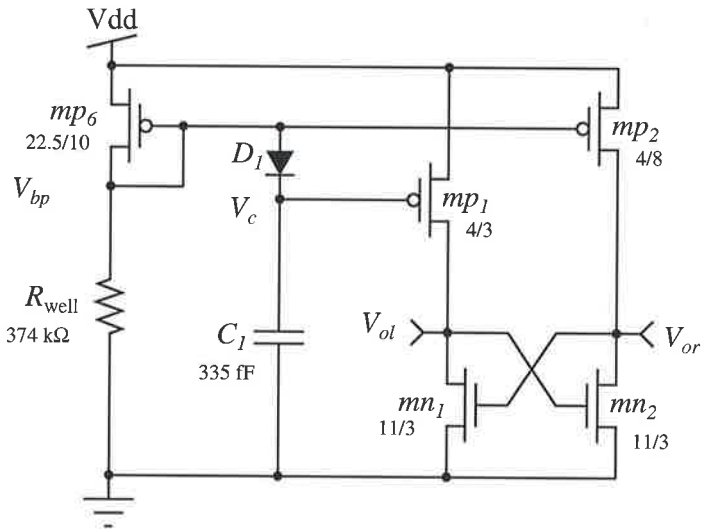

Figure 8.3. The circuit diagram of Version-1 of PMD circuit. This diagram shows the first attempt by the company to design and implement the PMD circuit. This circuit has failed due to overestimation of the diode leakage current.

The circuit shown in Figure 8.3 was fabricated in a Hughes process. Tests conducted by the company showed that the circuit was able to come-up in reply mode once energised. Furthermore, when the supply voltage was interrupted for a short period of time in order of 200 μs the circuit comes-up in program mode. However, when the supply voltage was re-interrupted for a long period of time more than 500 μs, the circuit still comes up in program mode. To get the circuit back to reply mode, a few seconds of supply interruption were needed. Upon these tests, it was concluded that the leakage current in the diode was overestimated and it is not large enough to discharge C_1 during the 500 μs interruption

period. A solution to this problem is to develop a discharge mechanism that is based on predictable discharge current as discussed in the following paragraph.

Due to the problem discussed above, a circuit that allows a predictable discharge current to discharge node V_c was developed. A bleed circuit to provide controllable discharge of node V_c was developed. This circuit is simply an nMOS transistor mn_4 in parallel with C_1. The gate terminal of mn_4 is connected to a fixed voltage as shown in Figure 8.4. This circuit was called Version-2 PMD circuit. The gate voltage of mn_4 is preserved during the supply voltage collapse using another diode, D_2, to trap the charges at its gate. The bleed current value, I_{mn_4}, can be written as

$$I_{mn_4} = \frac{S_{mn_4}}{S_{mn_5}} \frac{S_{mp_7}}{S_{mp_6}} I_{R_{\text{well}}}, \tag{8.1}$$

where S_i is the width to length ratio of transistor i. While the current passing through the well resistor, $I_{R_{\text{well}}}$, can be approximated as

$$I_{R_{\text{well}}} = \frac{V_{dd} - V_{bp}}{R_{\text{well}}}.$$

Using the transistors sizes given in Figure 8.4 in Equation 8.1 gives a 3.4 nA bleed current. Hence, the time needed to fully discharge the 335 fF capacitor is 394 μs. The residual voltage across C_1 when it is discharged for 200 μs is 2 Volts. This voltage is large enough to enable the circuit to come-up in program mode after a short interruption in the supply voltage. If the supply voltage is interrupted for 500 μs and more, C_1 will be fully discharged to ground – hence the circuit comes-up in reply mode.

The circuit shown in Figure 8.4 was also fabricated by the sponsoring company in the Hughes process. Test results showed that the circuit comes up in reply mode at startup as expected. However, when the circuit supply voltage is interrupted for a short period of time the circuit still comes up in reply mode. At this stage, the problems with PMD circuit were introduced to the author to investigate and understand the circuit operation under all power supply conditions.

8.4 New PMD circuits

Hardware debugging of the fabricated PMD circuits was not possible due to limited access to the PMD circuit internal nodes, especially the vital nodes such as V_c, V_{bp}, V_{ol} and V_{or}. Also, due to incompatibility between the provided Hughes process model parameters by the company and known SPICE model parameters, HSPICE Level 28 model parameters

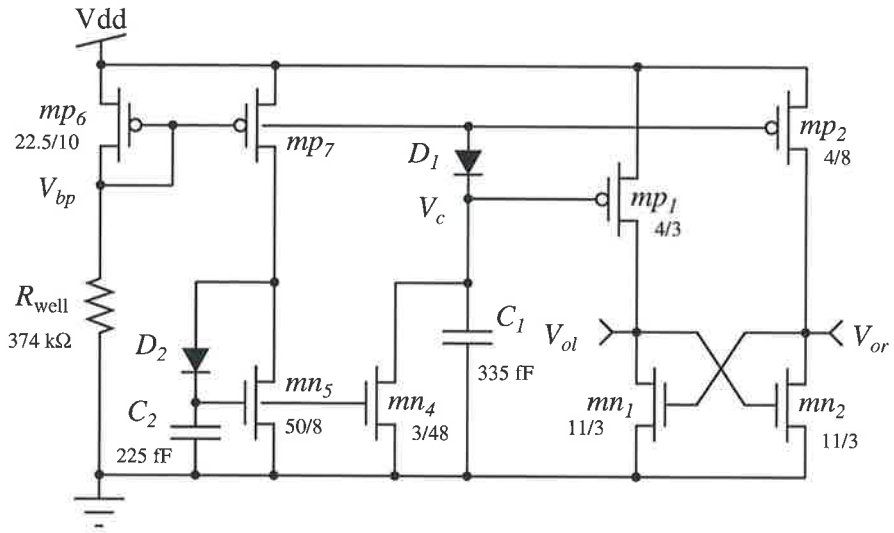

Figure 8.4. The circuit diagram of Version-2 of PMD circuit. This is the second design of the PMD circuit. The circuit did also fail due to the charge storage at V_{or} and V_{ol}.

for Orbit Semiconductor 1.2 μm double poly, double metal n-well standard CMOS process were used. The circuit was redesigned using Orbit Semiconductor model parameters. Versions-1 and -2 of the PMD circuit were simulated. The simulation results for Version-1 PMD circuit are shown in Figure 8.5. These simulations are consistent with the test reported by the company as discussed in Section 8.3.1. The simulations show that the diode leakage current is very small and will not allow the discharge of C_1 to ground in 500 μs. The time it takes C_1 to discharge using a diode leakage current of 100 fA is about 13 seconds.

Version 2 of the PMD circuit was also simulated using the previously mentioned model parameters. The simulated bleed current was 0.8 nA instead of design value of 3.4 nA. The difference is traceable to the fact that the 3.4 nA was calculated using simple model parameters and did not take into account second order effects such as channel length modulation and the subthreshold operation of the transistors. Thus to obtain the 3.4 nA bleed current, the width to length ratio (in microns) of mn_4 was changed from 3/48 to 3/18. The simulation results shown in Figure 8.6 show that during the supply interruption period, the voltage at V_{ol} does not fully discharge to ground. This is due to trapped charges at the gate of mn_2. These charges disturb the balance of the cross coupled inverters in favour of the reply mode.

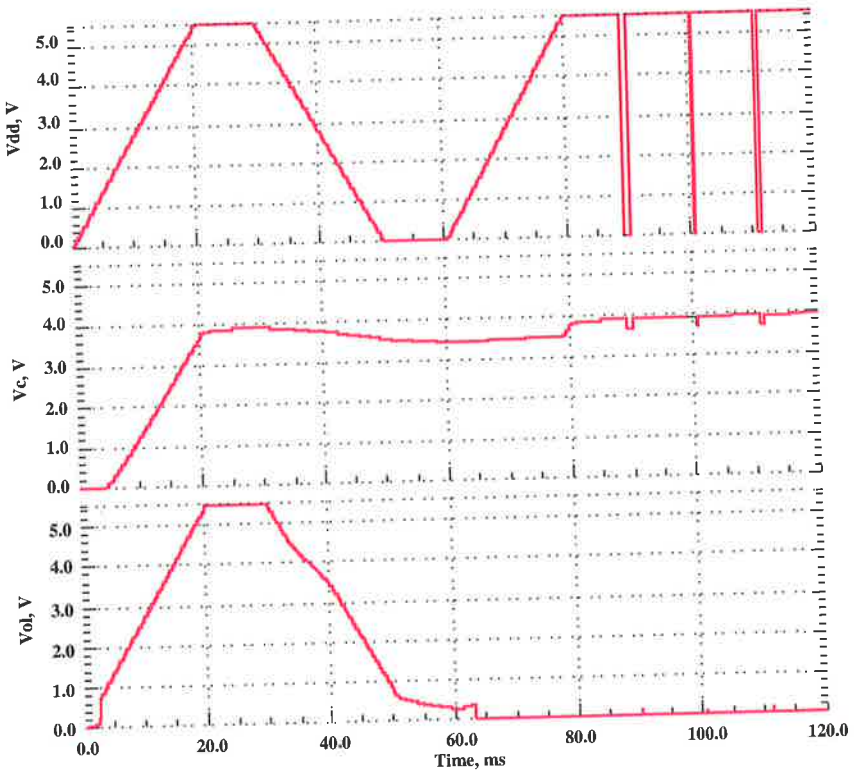

Figure 8.5. Simulation results for Version-1 PMD circuit. These simulations show why the PMD circuit failed to function as expected, which is due to overestimation of the diode leakage current during the design phase.

8.4.1 New Program Mode Detection Circuits

The solution to the trapped charge problem at the gate of mn_2 can be solved using another controlled bleed current source at the gate of mn_2. However, when the circuit comes up in program mode, similar trapping of charges will occur at the gate of V_{or}, hence another controlled bleed current source had to be added between V_{or} and ground. The two introduced bleed circuits at the gates of mn_1 and mn_2 are shown in Figure 8.7. This circuit was called Version-3 PMD circuit. The simulation results of this circuit are shown in Figure 8.8. These simulations show that the gates of mn_1 and mn_2 are fully discharged to ground during the supply voltage interruption. Hence, the PMD circuit is operating according to the design specification.

As the PMD circuit is used as part of a passive transponder, it was decided to simulate Version 3 of PMD circuit including the on-chip rectifiers. To simplify the simulation, it was decided to model the rectifiers as two diodes in series with the circuit supply voltage and a large capacitor, $C_{V_{dd}}$, in parallel with circuit supply terminals as shown in

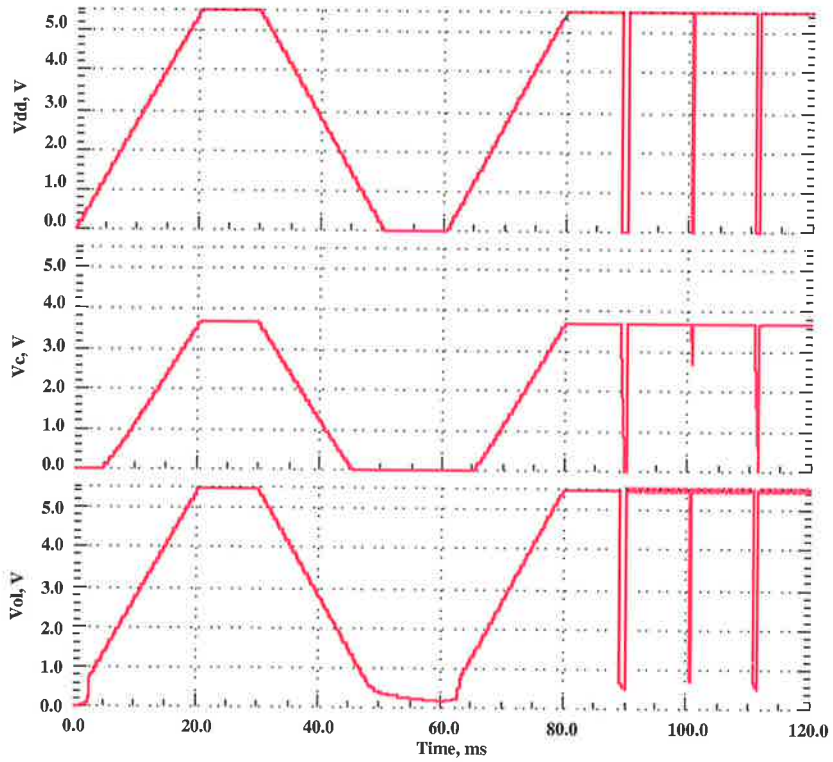

Figure 8.6. Simulation results for Version-2 PMD circuit with the new transistors adjustments. These simulations show why the Version-2 of the PMD circuit did fail to operate as expected. The reason is due to the charge storage at V_{ol} and V_{or}. The circuit had to be redesigned using Orbit Semiconductor model parameters.

Figure 8.9 to model the total capacitance between the supply terminals. The simulation results show that the circuit comes up in reply mode regardless of the duration of the supply interruption period. The circuit malfunction is due to the same reason that caused Version 2 of the PMD circuit to malfunction. This problem can be solved by either (i) fully discharging the supply voltage to ground during each interruption of the supply voltage; (ii) initialising V_{ol} and V_{or} to the same voltage; or (iii) increasing the bleed currents at V_{ol} and V_{or}. These techniques are evaluated in the following subsections.

8.4.2 PMD Circuits with a Supply Voltage Bleed

As mentioned earlier, as a result of the charge storage on the supply voltage terminals, the PMD circuit cannot come up in program mode. A direct approach to solve the problem is to fully discharge the circuit supply voltage to ground. This can be achieved in a number of methods:

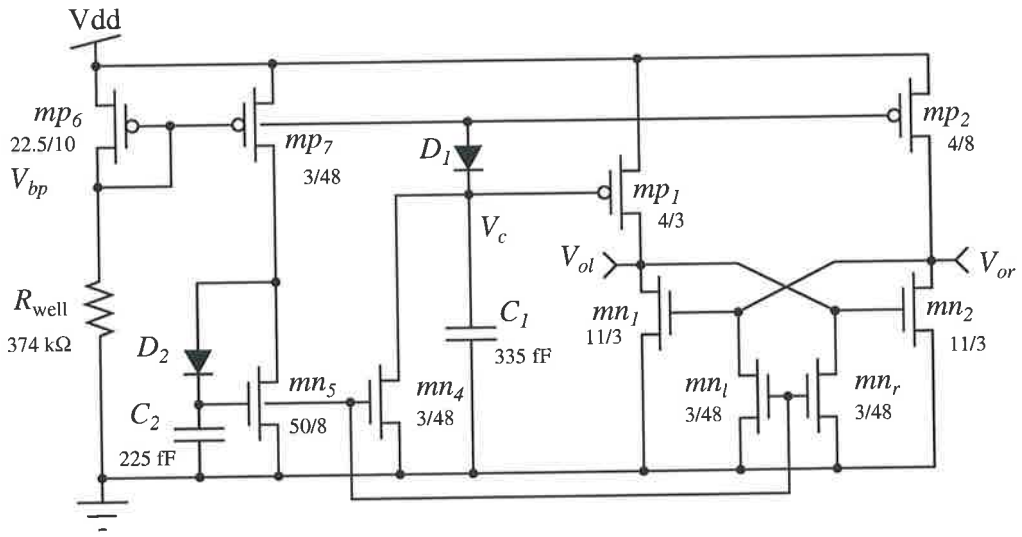

Figure 8.7. The circuit diagram of Version-3 of PMD circuit. This version of the PMD circuit did operate as expected using the test waveform shown in Figure 8.2.

- *Static Bleed:* In this approach another bleed circuit is used to discharge the load capacitance $C_{V_{dd}}$, This is achieved by using an nMOS transistor, $mn_{V_{dd}}$ with its drain and source terminals are connected to the supply terminals and its gate is connected to either V_n or V_c as shown in Figures 8.10 and 8.11. Connecting the gate of $mn_{V_{dd}}$ to V_c causes the load capacitance to discharge in a short period of time. However, the static current through this transistor is large – in the order of 9 μA. A better approach is to use V_n to control the discharge current through $mn_{V_{dd}}$. This approach did result in a much smaller static current in the range of 2 μA. The simulation results of the circuit shown in Figure 8.10 are shown in Figure 8.12. Even though, this is not the best option as this drains high current and might have the potential of bistable state under some bias conditions, the option was presented as a possibility because it requires a minor modification to the circuit layouts from the company point of view.

- *Dynamic Bleed:* This method also uses an nMOS transistor between the supply terminals with its gate is switched by an inverter. This inverter uses a preserved supply voltage and uses V_{bp} as an input. The V_{bp} node was used to drive the inverter because it is the only node in the circuit that is fully discharged to ground during the supply voltage interruption. The inverter output can also be used to fully discharge V_{ol} and V_{or} to ground upon the interruption of the supply voltage as shown in Figure 8.13. The simulation results of this circuit are shown in Figure 8.14. These

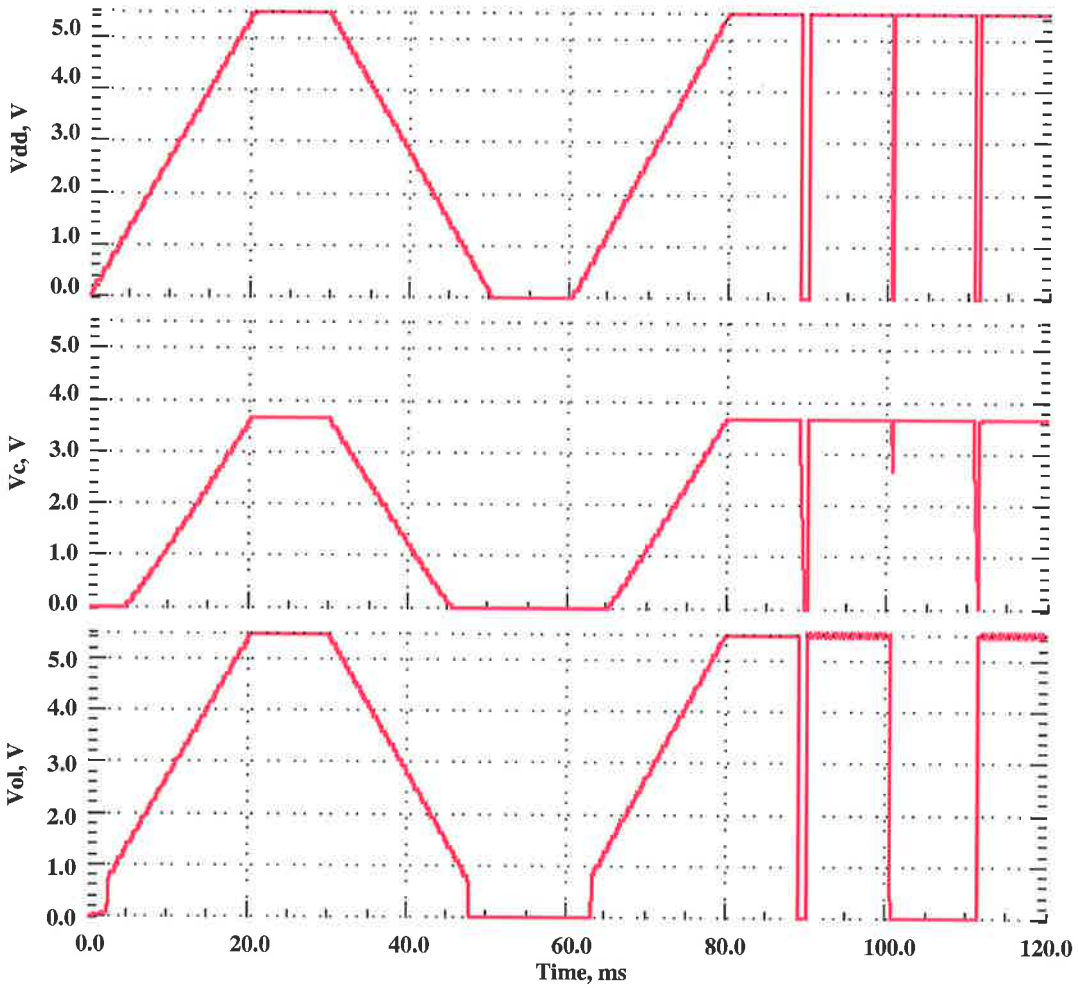

Figure 8.8. The simulation results of Version-3 PMD circuit. The upper panel shows the supply voltage used for simulating the PMD circuit. The middle panel shows the voltage at node V_c. The simulations show that node V_c was fully discharged to ground during long interruption periods in the power supply, however, during short interruptions node V_c does not fully discharge to ground, causing the needed imbalance to cause the circuit to come up in program mode. The lower panel shows the voltage at node V_{ol} as function of time and shows that during the short interruption in the supply voltage V_{ol} is low, hence V_{or} (not shown) will be forced high, because of the cross coupled structure of the PMD circuit.

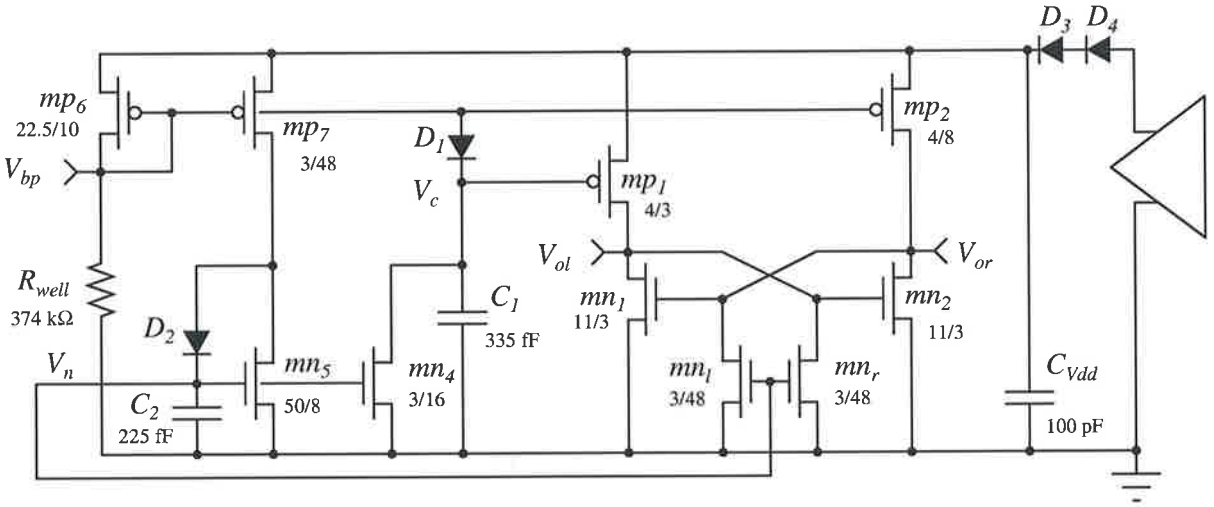

Figure 8.9. The circuit diagram of Version-4 of PMD circuit. This circuit is similar to Version-3 PMD circuit with the addition of two diodes connected in series with the supply voltage to model the on chip rectifiers and to include the capacitive loading effect between the supply voltage terminals. This circuit did fail to function due to the same reasons that caused Version-2 PMD to malfunction which is the charge storage at V_{ol} and V_{or} and the circuit supply terminals.

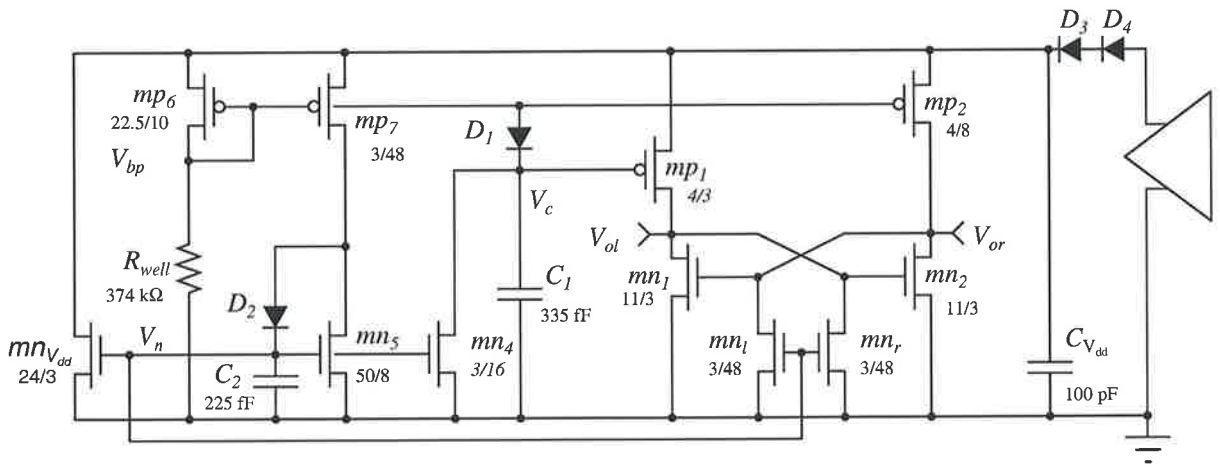

Figure 8.10. The circuit diagram of a PMD circuit that uses node V_n to statically bleeding the supply capacitance. One approach to discharge the supply terminals of the PMD circuit is to introduce a static bleed current $mn_{V_{dd}}$ between the supply voltage terminals as shown in this diagram and biasing this bleed circuit using node V_n.

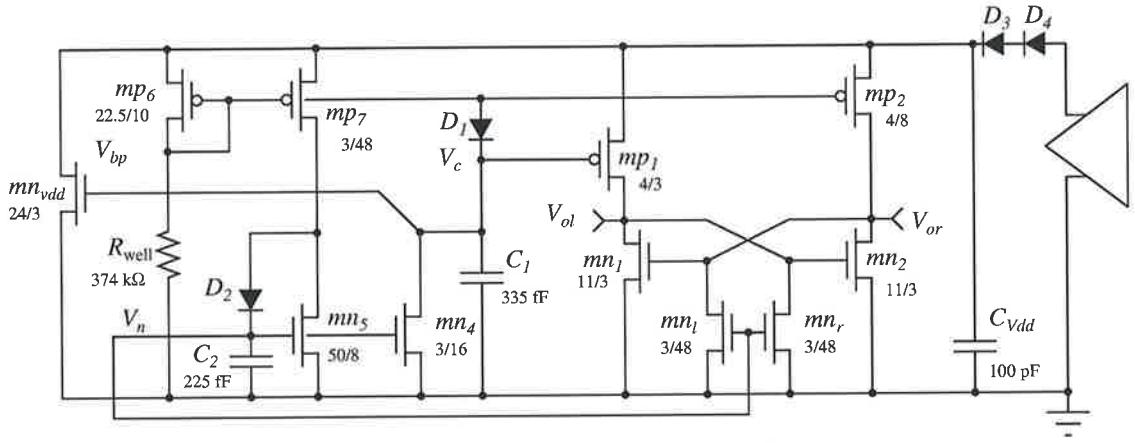

Figure 8.11. The circuit diagram of the PMD circuit that uses node V_c to statically bleed the supply capacitance. Another approach to discharge the supply terminals of the PMD circuit is to introduce a static bleed current $mn_{V_{dd}}$ between the supply voltage terminals as shown in this diagram and biasing this bleed circuit using node V_c. Using this approach results in a larger static and hence more power dissipation during the circuit operation.

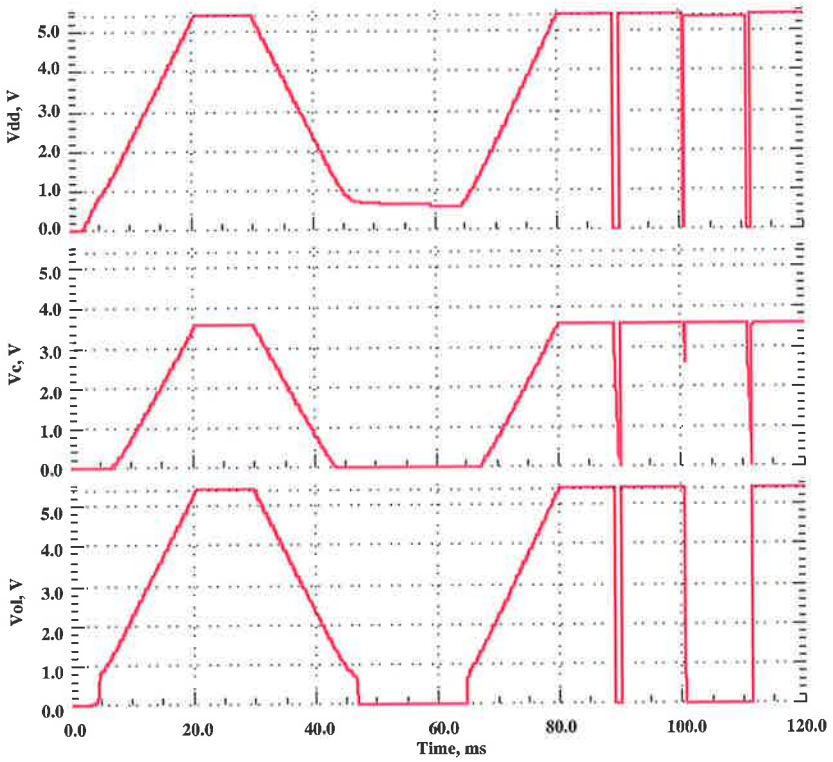

Figure 8.12. The simulation results of the PMD circuit shown in Figure 8.10. These simulations show how the PMD circuit with the rectifier model and capacitive loading were included. This circuit did function according to our test waveform and come up in program mode during a short interruption period in the supply voltage.

simulations show that the dynamic bleed is effective and resulted in less power as no static current is drawn from V_{dd}.

8.4.3 PMD Circuit with Node Reset

Rather than fully discharging the supply voltage to ground, as discussed in the Section 8.4.2, a technique similar to the dynamic bleed discussed above can be used to reset both V_{ol} and V_{or} to ground without the need to reset the supply voltage. Another variant of this technique is to use a transistor between V_{ol} and V_{or} and short-circuit these nodes together during the supply voltage interruption period. The circuit diagram for the first approach is shown in Figures 8.15, while the dashed line in the figure represent the second approach. The simulation results of these circuits are not presented.

8.4.4 Symmetrical PMD Circuit

Even though it is was demonstrated that the above designed PMD circuits are working as expected, these circuits will malfunction when temperature effect is taking into consideration for a number of reasons. Firstly, the voltage across D_1 is temperature sensitive because it is function of the reverse saturation current. Hence the voltage difference between V_{bp} and V_c is not independent of temperature. Secondly, the difference between V_{bp} and V_{dd} will decrease as function of temperature at a rate of -5 mV/°C. Hence, the initial voltage across C_1 increases with the increase in temperature, requiring a larger bleed current to discharge V_c, V_{ol} and V_{or}. Thirdly, due to the difference between V_{bp} and V_{dd} the voltage difference across R_{well} will increased. Hence, the reference current will also increase, resulting in increasing the bleed current that discharges nodes V_c, V_{ol} and V_{or}.

A new PMD circuit that is robust against temperature variations can be designed by ensuring that the circuit operation rely on relative parameters rather than the absolute value of these parameters. This is achieved by having a symmetrical circuit structure as shown in Figure 8.16. This circuit operation is similar to the previously discussed PMD circuits. The only addition is diode D_3 and capacitor C_3. These two elements will balance the load effect of D_1 and C_1 and result in circuit operation that depends only on the length ratios of mp_1 and mp_2. This circuit was simulated at temperatures starting from -50 °C to 100 °C in 50 °C steps as shown in Figure 8.17. These simulations show that the new symmetrical PMD circuit is robust against temperature variations and does function at wide temperatures range.

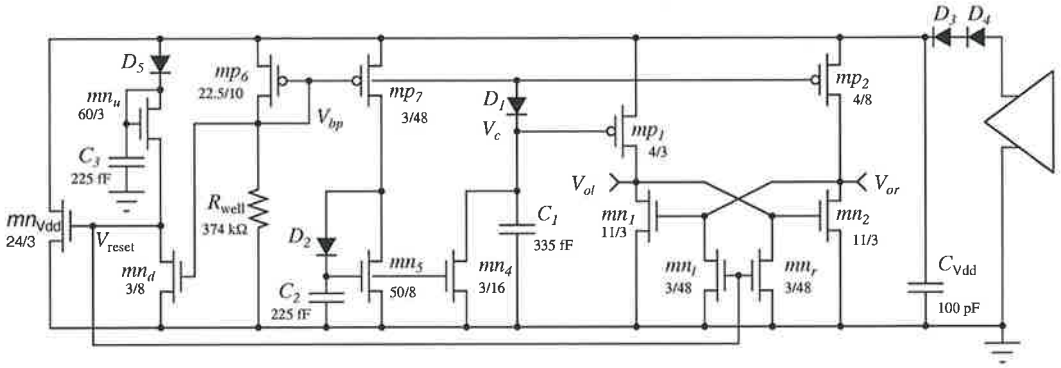

Figure 8.13. The circuit diagram of the PMD circuit that uses a dynamic bleed. In this circuit an inverter with bootstrapped load is used to turn on the bleed current during the supply voltage interruption.

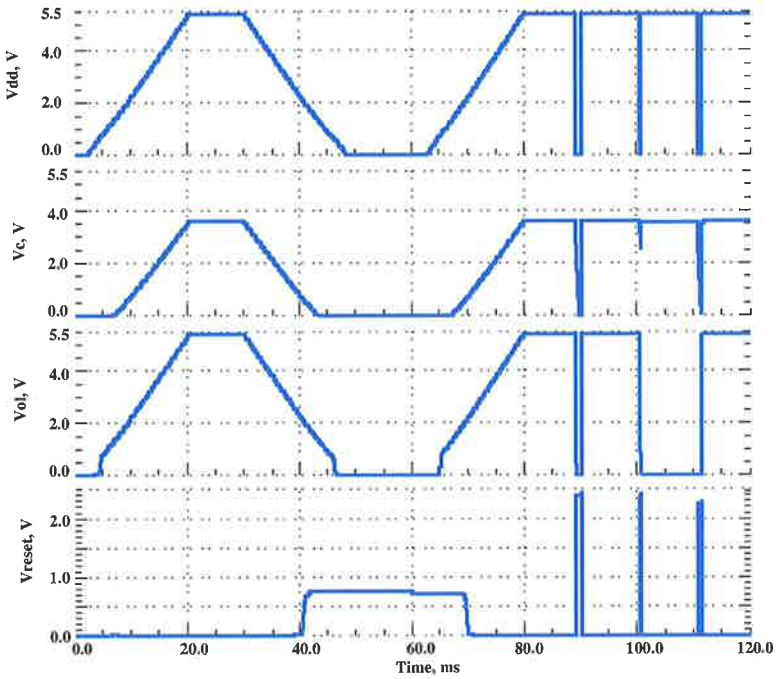

Figure 8.14. The simulation results of the PMD circuit shown in Figure 8.13. These simulations show how that the dynamic bleed operation. The upper panel shows the supply voltage to the circuit before the diodes. The second panel from the top shows the voltage at node V_c. The third panel from the top shows the output voltage at V_{ol} and shows that the circuit comes up in program mode during a short interruption period in the supply voltage. The last panel shows the reset voltage at the output of the bootstrapped inverter. This output is used to switch the bleed current. For slow variation in the power supply the bleed current is not trigger, once a fast interruption of the power supply terminals, the bleeding of the supply terminals is trigger and rapidly discharged.

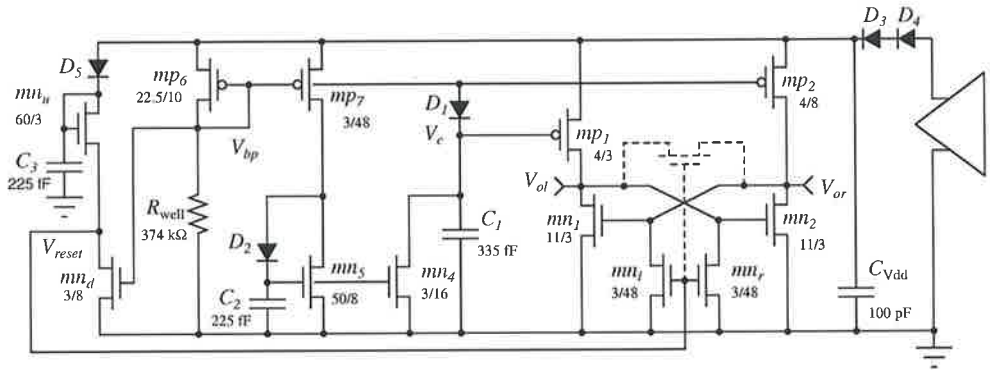

Figure 8.15. The circuit diagram of the PMD circuit that uses a dynamic approach to reset the voltage at V_{ol} and V_{or}. In this circuit shows how the dynamic bleed can be used to reset nodes V_{ol} and V_{or} to remove the charge stored at these nodes during supply voltage interruption. The transistor in dashed line represents the second approach with mn_l and mn_r are remove from the circuit and the reset voltage from the bootstrapped inverter is applied to it.

The circuit robustness against process variation was also considered by using Monte Carlo analysis. The number of iterations used for the Monte Carlo analysis is 50. The circuit was simulated by adding an additional voltage to the threshold voltages of all the transistors in the circuit. A Gaussian distribution with zero mean and 5 mV standard deviation was used. The mismatch in the resistor value was not considered in these simulations. This is due to the fact such resistor will have a wide process variation and from the author's point of view should be replaced by either a more controllable resistor or perform trimming on the resistor after circuit fabrication. The circuit did pass all the 50 Monte Carlo iterations and did come up in the right modes of operation based on the duration of the pulse interruptions in the power supply. Furthermore, special consideration is needed when laying-out this circuit to ensure better matching of the ideally matched transistors such as mn_1 and mn_2, mp_1 and mp_2, mn_4 and mn_5. Hence, the use of common centroid or interdigitated structures for these transistors pair is highly recommended.

8.5 Experimental Work

The static version of the PMD circuit shown in Figure 8.11 was implemented as part of the ISD9664 chip. The preferred option to test this circuit as a separate module and get access to the circuit internal nodes such as V_c, V_{ol} and V_{dd}. This option was not possible

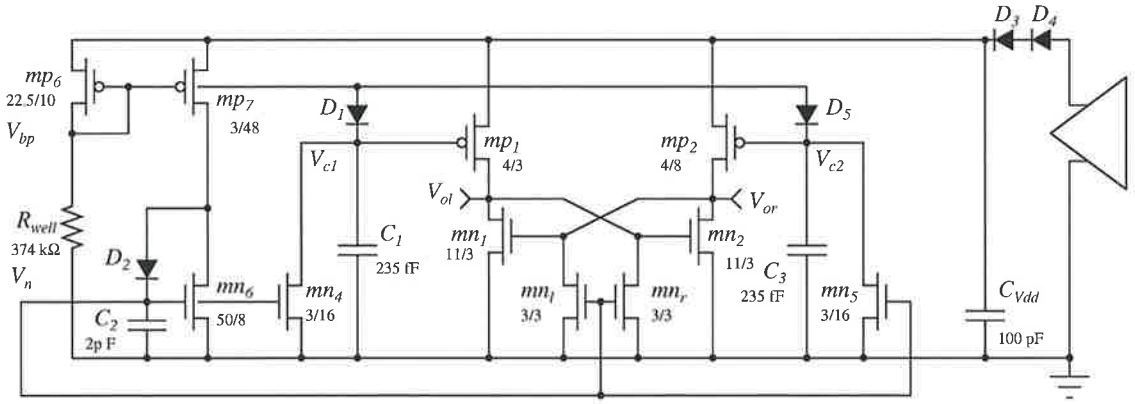

Figure 8.16. A fully symmetrical PMD circuit with fully isolated terminals from supply coupling. This structure results in a balance effect on the gates of mp_1 and mp_2 to isolate these nodes from the diode voltage difference at different temperatures due to the temperature dependence of the reverse saturation current of D_1. This circuit is very robust to circuit variation as it relies on relative parameters between circuit components rather than the absolute value of these parameters.

because the company needed a functional product very quickly and they took the responsibility of fabricating and testing the circuit. Even though, the selected PMD circuit for implementation from the author's point of view does not represent the best circuit in terms of power saving, the circuit was chosen by the sponsoring company as the version shown in Figure 8.11, which represents a minor modification of Version 2 of the PMD circuit. Hence this represented less risk from the company point of view. The functionality of the full chip was verified under RF measurements setup by the company employees and documented in internal reports [Pope 1996, Grasso 1996]. The measurement setup used a DAC – digital to analog converter and a controlled RF attenuator made of a double balanced mixer that was connected via a 4 Watt power amplifier to an antenna. The used DAC programming waveform is shown in Figure 8.18. Unfortunately, the corresponding rectified voltage for the fabricated chip is not available. This voltage could not be calculated as it is function of a number of parameters such as the distance between the interrogator and the transponder, the quality factor of the interrogator antenna and the transponder antenna and the efficiency of the integrated rectifiers. Measuring these parameters is beyond the scope of this work. However, the measurement results indicate that the PMD circuit is 'functional' from the company point of view.

One observation about the waveform shown in Figure 8.18 is that after the 200 μs interruption of the interrogating RF power, the rise time of the DAC had to be decreased

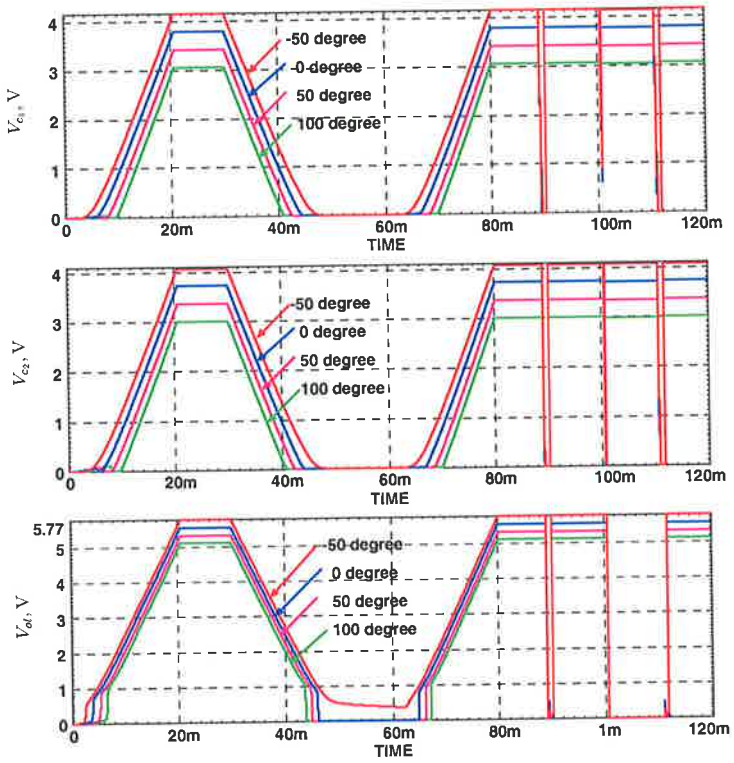

Figure 8.17. Simulation results of a fully symmetrical PMD circuit with the circuit temperature was swept from -50 °C to 100 °C in 50 °C steps. These simulations show that the fully symmetrical PMD circuit is robust to temperature variations and did function at a very wide temperature range.

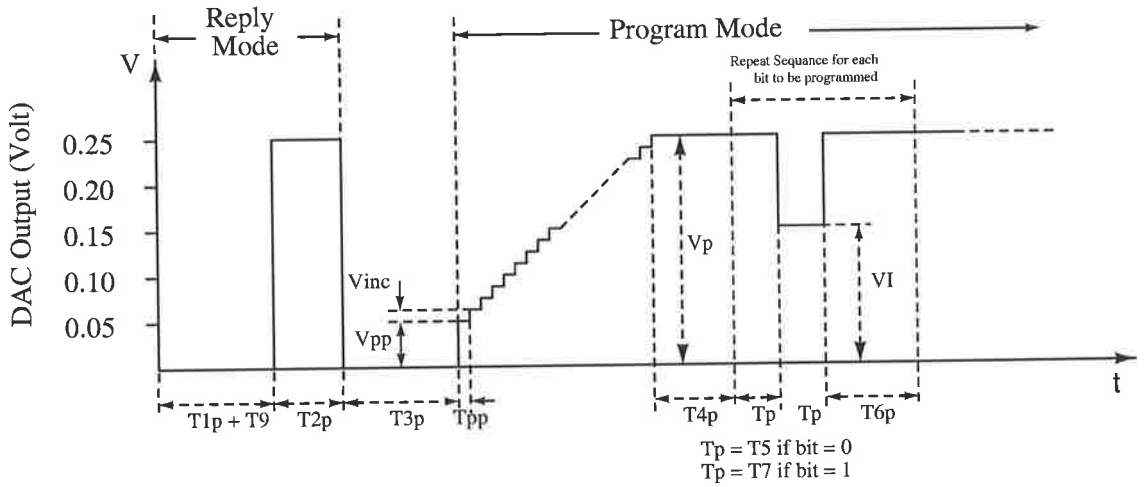

Figure 8.18. The output of the analog to digital converter that was used to control the RF attenuator for measuring the PMD circuit within RF environment. The values of the parameters used in this figure are given in Table 8.1. This waveform was used to test the PMD circuit shown in Figure 8.11.

Table 8.1. Parameter values. Values for the variables displayed in Figure 8.18 are tabulated.

Legend Name	Value
T1p	18 ms
T2p	200 μs
T3p	200 μs
T4p	25 ms
T6p	25 ms
T7p	500 ms
Tpp	90 μs
T9	1 ms
Vpp	50 mV
Vinc	20 mV
Vl	16 mV

to enable the PMD circuit to come up in program mode. Investigating the need to reduce the rise time through measurement is not possible as access to the chip rectified supply voltage and other internal nodes is not possible. However, it is believed that the need to reduce the rise time is due to capacitive coupling from the chip supply voltage rail to node V_{bp}, resulting in improving the rise time at that node. As there is a setup time needed by the cross coupled inverters to resolve their state as a function of the supply voltage. This resulted in V_{bp} and V_c having a fast rise time interruption signal caused the circuit to malfunction when the rise time of the interruption pulse is comparable to the setup time of the cross coupled inverters. For this reason, it is believed that the person who conducted the measurement managed to start the circuit in program mode by trial and error. Inspecting the ISD9664 chip layouts, showed that node V_{bp} is biasing other circuits such as the Operating Power Detection circuit, hence supporting the previous conclusion. To confirm the previous conclusion, the PMD circuit was simulated with different values of coupling capacitors between the supply voltage and V_{bp} as shown in Figure 8.19. This figure shows only the simulation results during the rise time transition of a short pulse interruption period in the circuit supply voltage. The simulations show that the voltage at node V_{bp} was very well established before the cross coupled inverters are able to resolve their states. The solutions to this problem is discussed in the following paragraph.

The first solution to the above problem is to reduce the rise time of the pulse interruption circuit in order to give the cross coupled inverters enough time to establish their states before the full restoration of the supply voltage. The second solution is to improve

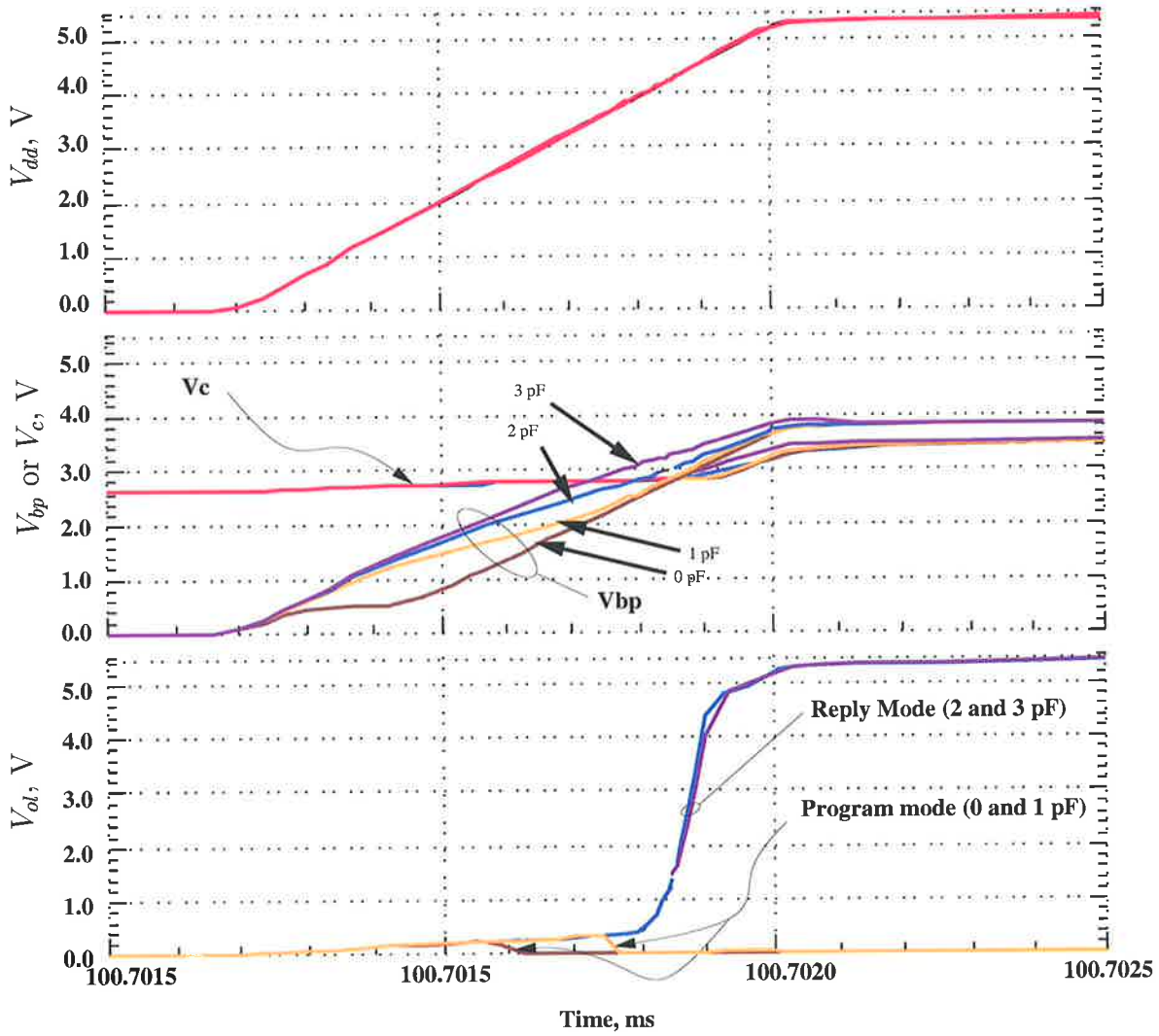

Figure 8.19. The simulation results of the PMD circuit with different values of coupling capacitors between the supply voltage and V_{bp}. These simulation were conducted using different values of coupling capacitors between the supply voltage and V_{bp}. The capacitor value was swept from 0 to 3 pF in 1 pF steps (Every panel has four overlapping curves). The upper panel shows the supply voltage waveform applied to the circuit before the two diodes in series. The middle panel shows the voltage at node V_c and V_{bp}. It can be seen that the voltage at V_{bp} did vary as function of the coupling capacitor value. At high values of coupling capacitance between V_{bp} and ground, the PMD circuit did malfunction because the voltage at node V_{bp} was very well established before the cross coupled inverters are able to resolve their states. Hence the gate to source voltages of mp_1 and mp_2 will not be able to decide the state of the cross coupled inverters. The bottom panel shows V_{ol} output as function of the coupling capacitance between V_{bp} and ground. These simulations show that circuit did come up in the wrong mode of operation at large coupling capacitor values.

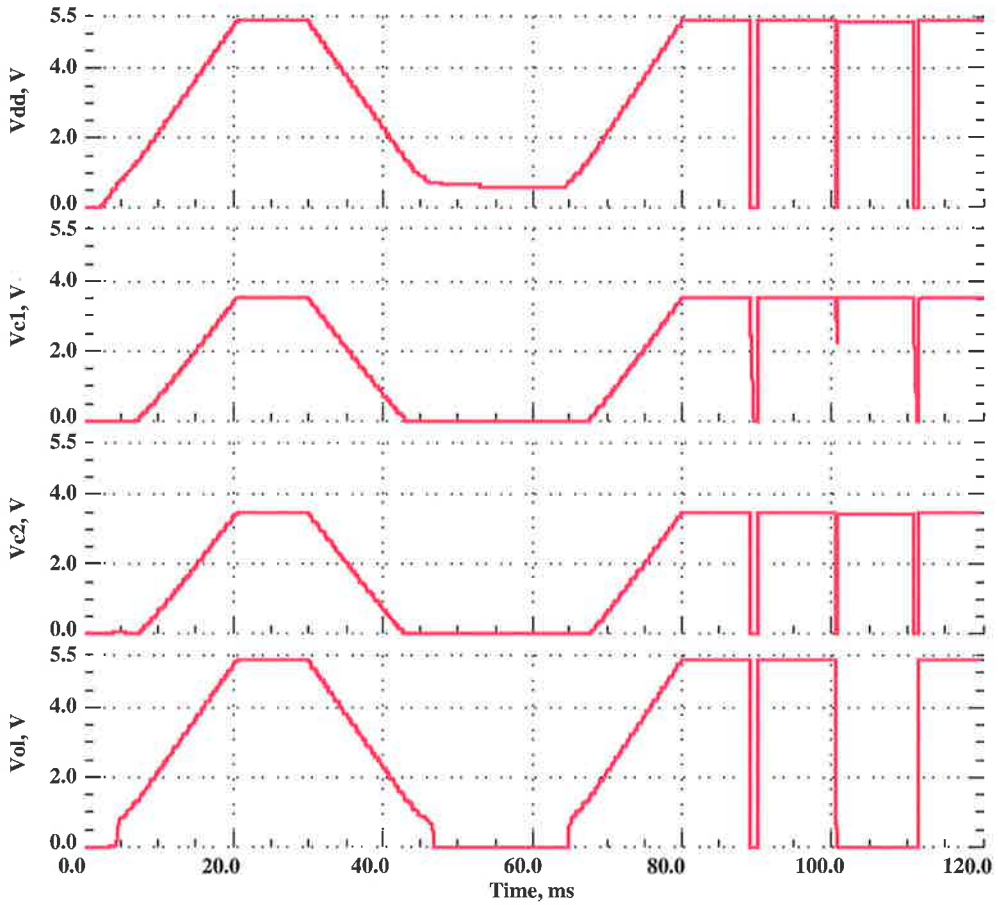

Figure 8.20. The simulation results of a fully symmetrical PMD circuit with different coupling capacitors from the supply voltage to V_{bp}. These simulations show that the capacitive coupling at V_{bp} in case of the fully symmetrical PMD circuit has no effect on circuit operation.

the circuit symmetry and isolate the gates of mp_1 and mp_2 from node V_{bp} as shown by the proposed circuit in Figure 8.16. This circuit was simulated as shown in Figure 8.20 with the same values of coupling capacitance used in the simulations of Figure 8.19. The simulation results show the effectiveness of the new symmetrical PMD circuit to capacitive coupling at node V_{bp}.

8.6 Summary

From the above discussion a new current bleeding principle was developed and employed in the design of six different practical PMD circuits. These circuits were designed to overcome the problem of unwanted charge storage at some of the circuit internal nodes

and the supply voltage bus. One of the designed PMD circuits that uses a static bleed technique was implemented as part of a commercial product by the company. However, the implemented version revealed a problem with the PMD circuit operation when fast rise time interruption pulse is used. One solution to the problem was found by trial and error by the person who tested the circuit through reducing the rise time of the interruption pulse. The second solution is through isolating the gates of mp_1 and mp_2 from node V_{bp} and improving the circuit symmetry as shown in Figure 8.16. This circuit overcomes the problems that arise as a result of charge storage at some of the circuit internal nodes and the supply voltage in addition to the capacitive coupling between the supply voltage and node V_{bp}. The discussed circuits lend themselves to low power by scaling the reference current passing through R_{well}.

In this chapter a number of PMD circuits were designed taking into account the environment at which these circuits operate in. A comparison between the discussed circuits can be made upon area and power consumption. In general all the circuits have roughly the same area. However, the static power dissipation of some of the designed circuits is quite high as it is the case with the circuit shown in Figure 8.10, while the static version shown in 8.11 has lower power dissipation compared to the previous circuit. For the dynamic versions, these circuits dissipate much less power and they are more efficient in collapsing the supply voltage, when large capacitance between the supply terminals does exist.

In summary the current bleeding technique was developed and employed in designing practical PMD circuits. Problems related to PMD circuits malfunction were investigated and techniques to overcome these problems were presented and discussed. Experimental results verified the operation of one version of the PMD circuit. Upon these results, a new problem was identified. Solutions to this problem were discussed and verified through simulations.

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Chapter 9

Conclusions and Directions

IN this chapter an extended summary of the work undertaken in this research is presented. Also recommendation for future research and directions that could be undertaken and we finish with some concluding remarks.

In this research a survey of common modules that are needed in mixed mode analog-digital system are presented. Based on the survey, a number of basic analog building blocks were identified that are common to mixed analog-digital systems and to the targeted application, which is in the area of radio frequency identification systems. Then the research concentrated on these modules and presented new design techniques that target power reduction at various design levels. The main focus of this research is power reduction at the circuit level, however, in some of the presented techniques power reduction was achieved at other levels including fabrication process, architectural and algorithmic design levels. These techniques result in low power consumption and area efficient designs and can result in an overall improvement in mixed analog-digital systems.

Throughout this work we have carried out sensitivity modelling of the circuits using a first order assumption of variation only in threshold voltage (V_{th}). This is usually a good assumption as V_T variations are known to be the most dominant in CMOS processes. However, future work may be carried out to extend the sensitivity analysis to include variations in the intrinsic transconductance parameter β and the body effect factor γ.

In this chapter a summary of the research outcomes are presented and the research contributions are highlighted for each chapter.

9.1 Summary and Future Directions

In the following paragraphs a summary and recommendations for each chapter is presented.

- **Controlled Gain Amplifiers:** In standard low cost CMOS technologies, a digital inverter from an analog circuit designer point of view is a very high gain amplifier when it is biased in the middle of its dc characteristic. The very high gain of the amplifier is function of second order effects that are not controllable by fabrication foundry. In the face of the amplifier high gain, a stable operating point is not possible. In Chapter 2, new controlled conductance devices are used to design controlled gain amplifiers with stable operating points. The amplifier circuit that uses a series transistor configuration is a true low power amplifier with a moderate dynamic range of operation. A matched bias circuit to provide a stable operating point for the low power amplifier when used in an AC amplifier design was also discussed. These circuits were implemented in silicon and their operation was verified. The measurements show the effectiveness of the proposed techniques and good agreement with the presented analysis. Furthermore, measurements showed that

the designed circuit exhibits a small input offset voltage. This offset is due to the difference in the βs of the nMOS and the pMOS transistors.

Further research in this area can be in the utilisation of the controlled gain amplifier in the design of algorithmic type analog-to-digital converter (ADC) and determination of the dynamic range limitations of these types of ADCs as function of the amplifier gain accuracy and dynamic range.

- **Digital Trimming of Operational Amplifiers:** Operational amplifiers are basic building blocks in many mixed analog-digital applications. The input offset voltage in these circuits limits their use in applications such as comparators when the amplitude of the input signal is comparable to the input offset voltage. In the literature, a large number of techniques are used to either reduce or cancel the input offset voltage. Some of these techniques require the use of switched capacitors while others require the generation of precise analog signals. The use of a switch capacitor requires control and oscillator circuits, while generation of precise analog signals to control other circuits is problematic in a digital environment. Chapter 3 discussed new design techniques to digitally trim the input offset voltage based on statistical understanding of the input offset voltage variation in common CMOS technologies. These techniques are technology independent because they rely on the relative difference of parameters on the same substrate. Furthermore, some of the presented techniques do not require modification of the differential amplifier structure as the trimming is performed on the input buffer circuit rather than on the amplifier itself. The analysis presented in that chapter showed that the input offset voltage can be reduced to less than 1 mV using only seven programmable terminals. Furthermore, the offset voltage can be trimmed further if other weighting schemes are used. Experimental results showed the effectiveness of the proposed techniques and good agreement with the presented analysis. Furthermore, the presented analysis showed that the input offset voltage can be trimmed down to 100 μV in best cases and up to 1.6 mV in the worst case using only a 5 bit binary weighting scheme. The new trimming techniques can compensate for the input offset voltage in the amplifier structure and for the mismatch that can occur in the introduced circuitry. Further work is to incorporate these new techniques in an auto-zero input offset voltage cancellation scheme by an algorithm similar to the one discussed in Section 3.3.3. The use of the new trimming techniques in auto-zero cancellation will reduce the area requirements and achieve better offset voltage cancellation with better noise immunity as the control is performed digitally.

Further research on this topic can be to expand on the digitally trimmed arms and modify the technique to provide equally spaced trimming of the input offset voltage. This can be done by firstly linearising the logarithmic function, and secondly using other weighting schemes that use a base of less than two.

- **New Schmitt Trigger Circuits:** Schmitt trigger circuits have been around since Otto Schmitt invented his original prototype using vacuum tubes. Many circuits have been proposed in the literature to mimic the original prototype. Unfortunately, the aspects of low power and low voltage in these circuits, to the best of the author's knowledge, have not been addressed. In Chapter 4 two new families of Schmitt trigger circuits were presented and discussed. The first family has an infinite input impedance, the second has a finite input impedance. A member of the first family is a true low power Schmitt trigger circuit with a wide hysteresis width. In all of these new families, the hysteresis adjustment through an electrical signal was also discussed. A comparison between the commonly used Schmitt trigger circuits and the new low power circuit developed in this work revealed its true low power characteristics and driving capability in comparison with other Schmitt trigger circuits presented in the literature. The experimental results are consistent with the designed and simulated characteristics of the circuit. Further work can be to precisely measure the current through the Schmitt trigger circuit and compare it to commonly used Schmitt trigger circuits through physical implementation.

  The new low power Schmitt trigger circuit can be used in the design of low power integrator oscillators as discussed in Appendix D. In that appendix, the design procedure for this type oscillator was briefly discussed. Furthermore, a new technique to extend the integration voltage of the integrator oscillator was discussed and verified through simulation. The numerical example presented in Section D.3 showed that an increase in the oscillation period by a factor of two as a result of using this technique is possible. On the other hand, the increase in the oscillator period can be used to reduce the required capacitor size. Incorporating the low power Schmitt trigger circuit discussed in Section 4.2 in the integrator oscillator design, results in an oscillator with low power characteristics and lower frequency of operation as the hysteresis width of this Schmitt trigger circuit is larger than the commonly used Schmitt trigger circuits. The operation of the new extended mode integrator oscillator that uses five integrators was verified experimentally and demonstrated the principle of operation with good agreement with the designed and simulated values.

Further research in this area would be to use a customised digital division scheme in conjunction with extended mode integrator oscillator. This would allow the design of much low frequency integrator oscillators with small area.

- **Analog Circuit Design using Neuron MOS:** Neuron-MOS device (νMOS) is a more intelligent device than a mere switching device, because it calculates the weighted sum of all input signals at the gate level, and controls the 'ON' and 'OFF' states of the transistor based on the result of the weighted sum operation. Most circuits designed using this device use digital signals to achieve certain functions. In Chapter 5 a general model was derived for the neuron-MOS and the key design parameters for the design of analog and digital circuits were identified. Based on these key design parameters a number of new controlled gain amplifier circuits were designed. The gain of these circuits is precisely defined by capacitor ratios rather than technology specific parameters. Furthermore, the neuron-MOS device was also used in the design of new Schmitt trigger circuits with switching points as a function of capacitor ratios. Experimental results of the amplifier and Schmitt trigger circuits showed very good agreement with the presented analysis, and verified the principle of operation of these circuits. Also the measurement showed that the effect of the nMOS and pMOS transistor βs on the circuit characteristics. This effect appeared as an offset voltage in case of the amplifier circuit and as shift in the hysteresis width in case of the Schmitt trigger circuit. Also the measurements showed that the effect of charges trapped on the floating gate is minimal and was not an issue in the used fabrication process. However, it could be an issue in other fabrication processes.

  Future research in this area can also be in mixed analog and digital circuit designs. In the digital domain, application of neuron MOS in threshold logic and sequential circuits are good examples of research areas that may possibly benefit from neuron MOS devices. In the analog domain, designing more complex analog circuits such as sigma-delta modulators with weighted feedback or weighted feed forward paths are also good examples.

- **Novel Low Power Ripple Through Gray Code Counters:** In portable mixed analog-digital applications, there is always a need to minimise the digital noise on the common supply bus as noise from the digital circuits can couple to the analog circuits through the power supply rail, causing the analog circuits in some cases to malfunction. The digital noise can be reduced through reducing the transients on the common power supply rail and through reducing the digital activity of the digital

circuits. The first is achieved by using digital circuits with low power characteristics, while the second, in case of digital counters, is through using counting circuits that has minimal number of transition to achieve the required number of states. In counting circuits, unit step sequences are an ideal choice as they deliver the required number of states using minimal number of transitions. To design a counting circuit that can be used in many applications, it was decided to use Gray code sequence. This sequence is also a unit step sequence and commonly known as a reflected code. The common techniques to design Gray code counters are (i) using a binary counter then performing an XOR operation between the adjacent bits to generate Gray code sequence or (ii) using a state machine. In Chapter 6 new formulas for generating Gray code sequences in relation to clock signal transitions are derived. The new formulas show that it is possible to obtain a binary counting sequence in addition to a Gray code counting sequence at no extra cost. Furthermore, the derived formulas are expandable to any number of bits. In terms of hardware, the counter can be extended to any number of bits without the need for any additional combinational circuits. Implementation of formulas using an optimised static JK flip-flop circuit was discussed. In addition, implementation through dynamic circuits, and issues related to clock skew were also addressed. Experimental results of a 4 bit Gray–3 bit binary counter using an optimised static JK flip-flop was verified experimentally through circuit fabrication.

Future research in this area would be to modify the formulas to allow parallel generation of the Gray code sequence. A possible approach is to use pipelined approach for the counter design. This would improve the speed of the counter and break the dependency between the modules. Also, investigation of the use of Gray-binary counters in the design of a Wilkinson type ADC and their effect on improving the differential and integral non-linearities of these types of ADCs would be fruitful.

- **A Novel Topology for Grounded–to–Floating Resistor Conversion:** A new circuit topology to convert most grounded resistors to an equivalent floating resistor is presented and discussed. The value of the resulting floating resistor equals the sum of the two grounded resistors. The new topology can be used to convert either passive, active grounded resistors or active grounded conductances. The new topology is used in the design of a current controlled very high value floating resistor in the GΩ range. This was achieved by utilising the output conductance of two matched transistors operating in the subthreshold region and biased using a 500 nA current. The practicality of the new topology is demonstrated through the design of a very

low frequency bandpass filter for artificial insect vision and pacemaker applications. Simulation results using Level 3 and Level 13 in HSPICE showed a THD of less than 0.5% for a 2 V_{pp} input signal in a 5 Volt 1.2 μm CMOS technology. Statistical modelling and temperature effects on the new topology are also addressed.

Further work in this research is the use of the bandpass filter in the design of a programmable center frequency, programmable bandwidth bandpass delta-sigma modulator. The presented filter lends itself for such application because of the electrical programmability of the resistor.

- **Program Mode Detection Circuits:** In the targeted application, a special circuit called program mode detection (PMD) is needed. This circuit has an output determined by the duration of an interruption period in the power supply. As the circuit output state is determined during the supply voltage transient, the operation of the circuit is uncommon in that the supply rails are used as inputs and the power up terminals at the same time. The sponsoring company designed a number of PMD circuits, however, none of them operated according to the design specifications. In Chapter 8 an investigation of these circuits was carried out. Based on the investigation, a number of new solutions were proposed based on a controlled bleed current technique. The circuit modelling took into account the effect of the rectifiers used in powering up the circuit. One of the proposed solutions was implemented by Integrated Silicon Design Pty. Ltd. Even though the implemented circuit did work under the conditions specified by the circuit test procedure, it did not work within the specification set during the circuit design. Further investigations showed the 'malfunction' of the circuit is due parasitic capacitances in the bias circuit that were introduced during the circuit layout process. As the author has no role in modifying the PMD circuit layout, a solution was outlined for the problem and discussed in this chapter. Statistical and temperature modelling of the new solution showed the robustness of the new circuit to process and temperature variations.

  Future research in this area can be on the implementation of the low power version of the PMD circuit and the proposed solution and in verification of its principle of operation.

9.2 Research Contributions

This section highlights the original contributions in this research that led to novel design methodologies for low power mixed signal systems and new design techniques applicable

to standard low cost CMOS technologies. These original contributions are summarised and listed below.

- **Controlled Conductance Devices:** Three new techniques to control the conductance of MOS transistors have been devised. The three technique are (*i*) Series Transistor Configuration (STC), (*ii*) Parallel Transistor Configuration (PTC) and (*iii*) Current Mirror Transistor Configuration (CMC). These techniques are used in designing controlled gain amplifier and bias circuits with stable operating points.

- **A New AC Coupling Technique:** A new technique to design an *AC* coupled amplifier circuit with very high input impedance in the order of giga-ohms with quick recovery from overload. Also a well matched biasing circuit with the STC amplifier circuit that allows the generation of a well defined operating point.

- **New Digital Trimming Techniques for Operational Amplifiers:** Three new techniques to digitally trim differential amplifiers have been devised. Some of these techniques require modification of the amplifier architecture to perform the trimming while other can be applied through an input buffer circuit. A relation between the number of digital trimming bits and the achieved offset voltage cancellation is derived and demonstrated through measurements.

- **A New Technique for Modulated Hysteresis Schmitt Trigger Circuits:** A simple and effective new technique to modulate the hysteresis width of Schmitt trigger circuits has been devised. This technique is presented through the design of two novel families of Schmitt trigger circuits. Some of these circuits have very small short circuit current and a wide hysteresis width using only 5 to 6 transistors. The proposed circuits offer low power feature, wide hysteresis with good fan-out. The techniques were verified through measurements.

- **New Techniques for Analog Circuit Design using Neuron MOS Transistor:** New techniques for designing controlled gain amplifier and Schmitt trigger circuits using Neuron MOS transistors have been devised. The characteristics of these circuits are a function of capacitor ratios. In contrast to switched capacitor circuits technique, where the circuit characteristics are also set using capacitor ratios, the presented techniques result in continuous time circuits and do not require a controlling clock. Simulations and measurements from circuit fabrication verified all the presented techniques.

- **A New Technique for Gray Code Generation:** A novel technique for Gray and binary code generation using new recurrent formulas in relation to a clock signal transition has been devised. It is demonstrated through the formulas and hardware implementation that the binary and Gray code lengths can be extended from N bits to $N + 1$ bits by adding one single circuit module without the need for any combinational logic. Based on the formulas and an optimised low power JK flip-flop it is demonstrated that the new formulas and designs usefully reduce switching activity on the power supply rails.

- **A Novel Topology to Convert Grounded Resistors to a Floating Equivalent:** A novel topology that facilitate the conversion of most grounded resistors or conductances to an equivalent floating resistor has been devised. The topology uses current mirrors connected in a special way to achieve the required cancellation. The topology is used in the design of a new current controlled floating active CMOS resistor. This resistor was used in the design of a very low frequency bandpass filter in the order of 100 Hz for artificial insect vision and pacemaker applications.

- **A New Controlled Current Bleeding Technique:** A new controlled current bleeding technique that relies on using two dynamic analog memory cells has been devised. The first analog cell stores a predefined analog voltage across a capacitor, while the second cell stores the value of a discharge current that is used to bleed a capacitor charge during the supply voltage interruption period. The practicality and effectiveness of the new technique was demonstrated through the design of an application specific integrated circuit (ASIC) for RFID systems to facilitate control and communication over a serial communication link. The new technique was verified through simulations and measurements from circuit fabrication.

9.3 Closing Comments

New design techniques for low power mixed analog-digital circuits were presented and discussed. The proposed techniques are applicable to a wide range of mixed analog-digital applications. The effectiveness of the proposed techniques and their performance was evaluated through circuit simulation and fabrication. Both measurements and simulations showed that the proposed techniques are applicable to standard low-cost CMOS technologies without the need to use either a specialised process or an optimised process. As the performance of the presented techniques is based on relative device parameters, such an approach results in robust designs and allow the portability and migration of

mixed analog-digital designs between standard CMOS processes with minimal amount of effort. It is hoped that the work presented in this thesis provides useful techniques that can be used in mixed analog-digital systems design and results in performance improvements in these systems.

Appendix A

Three Dimensional VLSI Packaging Study

THIS chapter reviews the state-of-the-art in 3D VLSI packaging technology. A number of bare dice and MCM stacking technologies are now emerging to meet the ever increasing demands for low power consumption, low weight and compact portable systems. Technical issues such as silicon efficiency, complexity, thermal management, interconnection capacity, speed and power are shown to be critical in the choice of 3D stacking technology, depending on the target application.

A.1 Introduction

As the complexity of portable electronic systems increases, such as in the shift from the mobile phone towards the Interactive Mobile Multimedia Personal Communicator (IM^3PC) paradigm, greater demands are being placed on the production of low power, low weight and compact packaging technologies for VLSI integrated circuits. Likewise many aerospace and military applications are following this trend. In order to meet this demand, many new 3D packaging technologies are now emerging where either bare dice or MCMs are stacked along the z-axis, resulting in dramatic improvement in compactness. As this z-plane technology results in a much lower overall interconnection length, parasitic capacitance and thereby system power consumption can be reduced by as much as 30% [Sheng *et al.* 1992].

Section A.2 will discuss the advantages of 3D packaging technology and its effect on system performance. Section A.3 will provide a brief discussion of the different vertical interconnection methods used in 3D packaging, while section A.4 will address the limitations of the 3D technology. Sections A.5 and A.6 will provide a discussion and a conclusion, respectively.

A.2 Advantages of 3D Packaging Technology

The following subsections discuss briefly how 3D packaging technology enhances system performance and provides performance factors that cannot be achieved using conventional packaging technologies.

A.2.1 Size and Weight

By replacing single chip packages with a 3D device, substantial size and weight reductions are achieved. The magnitude of these reductions depends, in part, on the interconnection capacity, which will be discussed in subsection A.2.7, thermal characteristics, and robustness required. It has been reported that 40-50 times reduction in size and weight is achievable using 3D technology compared to conventional packaging. As an example, volume and weight comparisons between TI's 3D bare dice packaging and discrete and planar packaging (MCM) are presented in Tables A.2.1. It is evident from these tables that a 5-6 times reduction in volume is possible over MCM technology and a 10-20 times reduction over discrete packaging technology. Moreover, a 2-13 times reduction in weight is also achievable compared to MCM technology and a 3-19 times reduction compared to

Table A.1. 3D Mass memory volume and weight comparisons. These comparisons are between other technologies and Texas 3D technology in terms of cm^3/Gbit and $grams^3$/Gbit [Crowley 1993a].

	Type	Capacity	Discrete	2D	3D	Discrete /3D	2D /3D
Weight	SRAM	1 Mbit	1678	783	133	12.6	5.9
		4 Mbit	872	249	41	21.3	6.1
	DRAM	1 Mbit	1357	441	88	15.4	5.0
		4 Mbit	608	179	31	19.6	5.0
		16 Mbit	185	69	69	16.8	6.2
Volume	SRAM	1 Mbit	3538	2540	195	18.1	13.0
		4 Mbit	1588	862	145	10.9	5.9
	DRAM	1 Mbit	2313	1542	132	17.5	11.6
		4 Mbit	862	590	113	7.6	5.2
		16 Mbit	363	227	113	3.2	2.0

discrete components. All of these reductions result from eliminating the overhead weight and size associated with conventional technologies. Furthermore, in the case of the Aladdin parallel processor [Terrill 1995], the reduction in size and volume against the Cray X-MP benchmark was by 666 and 2,700 times respectively.

A.2.2 Silicon Efficiency

One of the main issues in packaging technology is the chip footprint, which is the printed circuit board area occupied by the chip [Ladd 1993] as defined in Figure A.1. In the MCM case, the footprint is reduced by 20-90% because of the use of bare dice. 3D packaging results in more efficient utilisation of silicon real estate, which is referred to as 'silicon efficiency.' A comparison between 3D technology and other packaging technologies in terms of silicon efficiency is shown in Figure A.2, where 3D technology exceeds 100%.

A.2.3 Delay

Delay refers to the time required for a signal to travel between the functional circuit blocks in a system. In high speed systems, the total delay time is limited primarily by the time of flight, which is defined as the time taken for the signal to travel (fly) along

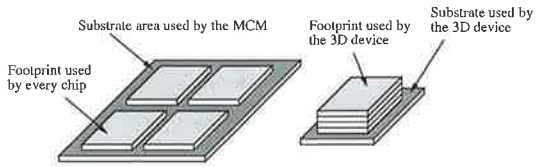

Figure A.1. 3D packaging technology silicon efficiency. This graphical illustration the silicon efficiency of 3D packaging technology compared to MCMs technology.

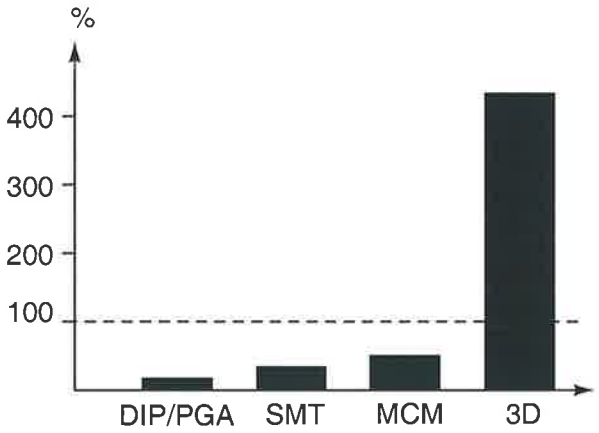

Figure A.2. Silicon efficiency comparison between 3D packaging technology and other conventional packaging. This diagram shows that 3D packaging technology can be up to 400% more efficient than other conventional packaging technologies [Ladd 1993].

the interconnect [Doane 1993a]. The time of flight, t, is directly proportional to the interconnect length. So reducing the delay requires reducing the interconnect length which is the case when using 3D packaging, as shown in Figure A.3. The resultant reduction in interconnect length, results in a reduction of the interconnect associated parasitic capacitance and inductance, hence reducing signal propagation delays. For example, the signal delay as a result of using MCMs is reduced by about 300% [Doane 1993a]. Furthermore, the delay would be less in case of 3D technology because the electronic components are in close proximity to each other, as shown in Figure A.3.

A.2.4 Noise

Noise in general can be defined as unwanted disturbances superimposed upon a useful signal, which tend to obscure its information content. In high performance systems, noise management is a major design issue. Noise can limit the achievable system performance by degrading edge rates, increasing delays, and reducing noise margins and can cause false

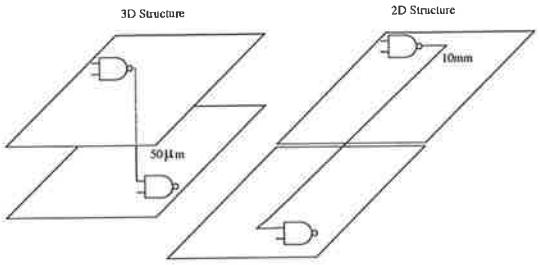

Figure A.3. A comparison between the wiring lengths in 2D and 3D structures. This graph shows how the wires length in 3D structures are greatly reduced compared to 2D structures [Lakhani *et al.* 1996].

logic switching. The noise magnitude and frequency are closely tied to the packaging and interconnect scheme used. In a digital system four major sources of noise can be identified as: (*i*) *Reflection noise*, (*ii*) *Crosstalk noise*, (*iii*) *Simultaneous switching noise* and (*iv*) *Electromagnetic interference (EMI)* [Doane 1993b]. The magnitude of all of these noise sources depends on the rise time of the signals passing through the interconnect. The faster the rise time, the worse the noise. The role of 3D technology in reducing noise is in the reduction of interconnection length, and hence reduction of the associated parasitics which translate into performance improvements. On the other hand, the noise could be problematic in a system if the used 3D technique does not address the noise. For example, if the interconnections have not got a uniform impedance along the line or its impedance does not match the source and destination impedance, there is the potential for reflection noise. Furthermore, if the interconnects are not spaced enough there is also a potential for crosstalk noise. While in relation to simultaneous noise it would be reduced because of the shortened interconnects and the reduction of the associated parasitics, so producing less simultaneous noise for the same number of interconnections.

A.2.5 Power Consumption

In an electronic system the energy dissipated, E, on the interconnect parasitic capacitance, C, is given by , $E = CV^2$, where V is the voltage swing across the parasitic capacitances. Moreover, the power consumed by the interconnects is the energy per transition, times the number of transitions per second, f, so Power, $P = fCV^2$. As the parasitic capacitance is proportional to the interconnection length, the total power consumption is reduced because of the reduced parasitics. For example, let us say that 10% of the system power consumption is dissipated in the interconnects when mounted on a PWB. If the product was implemented using MCM technology, the power consumption will be reduced by

a factor of 5. Hence, the product would consume 8% less power than the PWB-base product [Doane 1993c]. Furthermore, when such a product is implemented using 3D technology the saving will be much more because of the reduced interconnect length and the associated parasitics.

A.2.6 Speed

The power saving achieved using 3D technology can allow the 3D device to run at a faster rate of transitions per second (frequency) with no increase in power consumption. In addition, the reduction in parasitics (capacitances and inductances), size and noise of a 3D device, allow for higher transitions per second which would increase the overall system performance. For example, the Aladdin parallel processor, achieved 35,000 and 10,800 in MIPS and FLOPS per unit volume improvement over the Cray X-MP as a result of integration using 3D MCM technology [Terrill 1995].

A.2.7 Interconnect Capacity

The interconnect capacity (also called connectivity) is a measure of the amount of wiring available in a technology. One description of interconnect capacity is the available length of wiring interconnects per unit area of the module[8] [Turlik 1994, Doane 1993d].

Even though the interconnect capacity for 3D packaging depends on the interconnection technique used for packaging, it can be classified between the thin film and the wafer scale integration (WSI) technologies as shown in Figure A.4. Moreover, in 3D technology, through-vias can be used instead of wires to connect components on different planes, as shown in Figures A.3 and A.5, enabling connection of more components without using long wires, and hence, low propagation delays and good signal integrity.

A.3 Vertical Interconnections in 3D Electronics

Vertical Interconnections [Crowley 1993b, Ehrmann *et al.* 1995] refer to the interconnections needed to route power, ground, and signals to the layers within the 3D Module. The following subsections will describe briefly the different types of vertical interconnections.

[8]The interconnect capacity I_c is defined (when vias are small or are not placed on a uniform grid) as $I_c = \frac{1}{W_p} N_w$, where W_p is the wiring pitch, N_w is the number of signal wiring or interconnect layers.

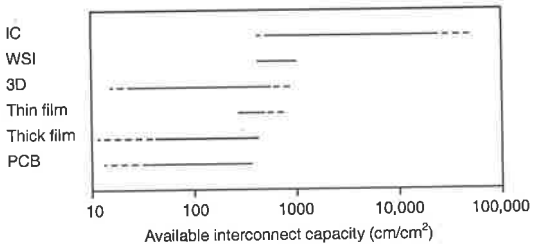

Figure A.4. Available interconnect capacity for different technologies (cm/cm^2). This graph shows that interconnect capacity can be as wafer scale integration technology [Turlik 1994, Moravec *et al.* 1993].

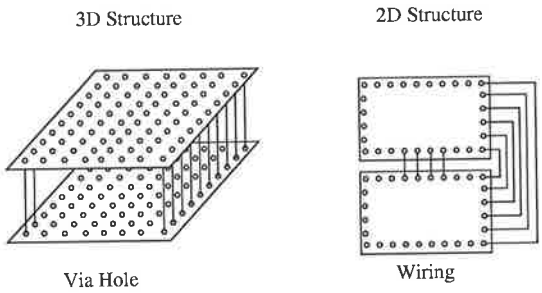

Figure A.5. A comparison between 3D and 2D structures in terms of the possible number of interconnections assuming one routing layer for the 2D structure. This graph shows the number interconnection is greatly increased compared to 2D structures. [Lakhani *et al.* 1996].

A.3.1 Periphery Interconnection between Stacked ICs

The following subsections will list interconnection techniques used to interconnect stacked chips using the stack periphery.

Stacked Tape Carrier

Stacked tape carrier is a method for interconnecting ICs using TAB technology. This method could be divided further into stacked TAB on PCB and stacked TAB on lead-frame as illustrated by the schematic diagram shown in Figure A.6. The TAB on PCB method is used by Intel Japan [Mita *et al.* 1994] and Matsushita Electric Industrial Company [Hatada *et al.* 1986, Hatada *et al.* 1987, Hatada 1990]. In Matsushita's case, they used this approach for designing high density memory cards. The second method is used by Fujitsu in designing DRAM chips [Mizukoshi *et al.* 1992, Crowley 1993c].

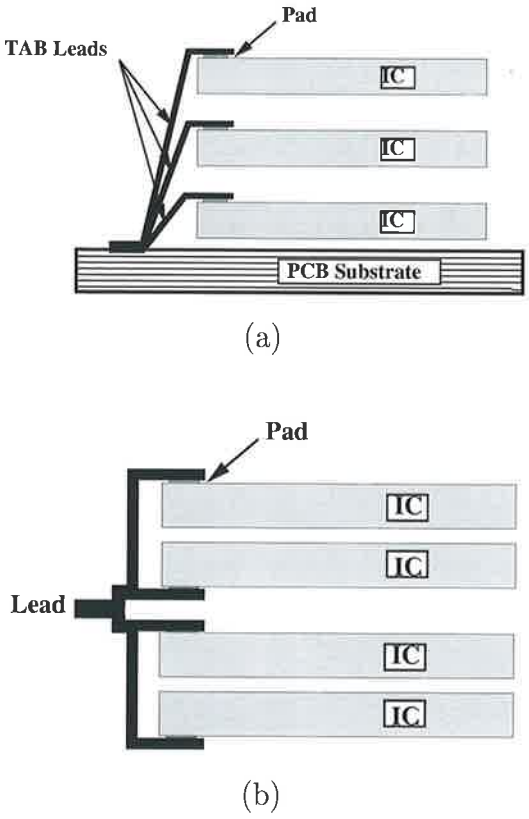

Figure A.6. Stacked tape carrier vertical interconnect. Two variants of the stacked tape carrier vertical interconnect. (a) Stacked TAB on PCB. (b) Stacked TAB on Leadframe.

Solder Edge Conductors

Solder edge conductor bonding is a process where vertical interconnections between ICs are performed by soldering edge conductors. There are three variants of this method as follows:

- *Solder dipped stacks to create vertical conductors on edge:* In this approach the leads of the stacked ICs that are to be connected, are brought into contact using a static molten solder bath and simultaneously soldered. A schematic diagram on how such interconnections are performed is shown in Figure A.7.a. This method is used by Dense-Pac for designing high density memory modules [Forthun 1992, Forthun & Belady 1992, Eide 1990].

- *Solder-filled holes in chip carriers and spacers:* In this approach the vias are filled with a conductive material to interconnect the stacked IC using carriers and spacers as shown in Figure A.7.b. This method is used by Micron Technology in designing

DRAM and SRAM chips [Fox *et al.* 1991]. A similar technique was developed and patented by Hughes Electronics [Hayden *et al.* 1996].

- *Solder connections between plated through-hole:* In this approach the IC leads are brought by TAB then interconnected using a small PCB called a PCB frame, which has vias through it. The vertical interconnections are achieved using these vias and by stacking these frames using solder joint bonding technique as shown in Figure A.7.d. Hitachi has developed this method and used it in the design of high density DRAMs [Miyano *et al.* 1993].

Thin Film Conductors on Face-of-a-Cube

Thin film is a layer of conductive material either sputtered or evaporated onto a substrate in a vacuum to form conductors. Thin film conductors on face-of-a-cube is a method where vertical interconnections are performed on the cube face. There are two variants of this method as follows:

- *Thin film 'T-connects' and sputtered metal conductors:* This method was jointly developed by Irvine Sensors and IBM. In this method, after the I/O signals are rerouted to one edge of the chip, a thin film metal layer is patterned on the surface of the stacked chips. Then, two processes, called lift-off photolithography and sputter-deposition, are performed on the face of the stack to form pads and buslines, creating what is called 'T-connections' [Minahan *et al.* 1992] as shown in Figure A.8.

- *Direct laser write traces on epoxy cube face:* In this method, the interconnect pattern on the sides of the cube is generated by laser trimming. This pattern is designed to intersect with the IC's wires cross section on the face of the cube [Coello-Vera *et al.* 1995, Cahill *et al.* 1995] as shown in Figure A.9. This method is used by Thomson-CFS DOI for high density memories [Coello-Vera *et al.* 1995], micro-camera [Larcombe *et al.* 1994, Stem *et al.* 1995], medical applications and smart munitions [Val 1994, Cahill *et al.* 1995].

An Interconnection Substrate Soldered to the Cube Face

In this method a separate substrate is soldered to the face of the cube as will be explained by the following variants of the method:

- *Array of TAB leads soldered to bumps on silicon substrate:* This method was developed and used by Texas Instruments in the design of very high density memories [Terrill & Beene 1996, Frew 1990, Bruns *et al.* 1992]. The vertical interconnections are achieved by rerouting the memory chip I/Os for TAB bonding. Then, a group of 4-16 of these chips is laminated in to form the 3D stack. These stacks are placed on a silicon substrate and aligned such that the TAB leads on the bottom of the stack contact the solder bumped pads on the substrate as shown in Figure A.10.

- *A flip-chip bonded to faces of the stack:* In this method, before MCMs are stacked their interconnection leads are brought to the side to a metallic pad. Then an IC is bonded to these metallic pads using flipchip technology as shown in Figure A.11. This approach was used by Grumman Aerospace corporation to develop surveillance technology for military applications [Schmitz *et al.* 1987, Crowley 1993d].

- *PC boards soldered on two sides of TSOP packages.* In this approach, two PCBs are soldered on two sides of stacked TSOP packages to perform the vertical interconnections. Then, the PCB leads are configured to form a dual in line package (DIP) as shown in Figure A.12. This method is used by Mitsubishi in designing high density memories [Tabaru & Uemura 1993].

Folded Flex Circuits

In the folded flex circuits, bare dice are mounted and interconnected on a flex type material, then folded to form a 3D stack [Fillion *et al.* 1995] as shown in Figure A.13. This method is reported by General Electric, Harris and MicroModule Systems.

Wire Bonded Stacked Chips

The 'wire bonded stacked chips' method uses a wire bonding technique for the vertical interconnections. There are two variants for this approach:

- *Wire bonded to an MCM substrate directly:* In this approach, stacked chips are wire bonded to a planar MCM substrate using wire bonding technology as shown in Figure A.14. This approach was used by Matra Marconi Space for a high density solid state recorder [Massenat 1993] and by nChip in the design of high density memory modules [Tuckerman *et al.* 1994].

- *Wire bonded to a substrate through an IC:* In this approach, there is a mother and a daughter chip. The mother chip will act as a substrate for the daughter chip, where interconnections from the daughter chip go to pads on the surface of the mother chip substrate as shown in Figure A.15. Voltonic USA has used this technology in some medical applications [Rochat 1995].

A.3.2 Area Interconnection between Stacked ICs

An area interconnection is a method where vertical interconnections are not bonded to the periphery of the stacked elements, as will be illustrated by the following variant of this method:

Flip-chip Bonded Stacked Chips without Spacers

In this approach the stacked ICs are flipped and interconnected to either a substrate or another chip using the solder joint technology. This technique was used by a lot of companies, some of these companies are IBM company in the design of ultra-high-density components [Howell *et al.* 1995], Fujitsu for stacking a GaAs chip on a CMOS chip technology [Sekine *et al.* 1994] and Matsushita which developed a new 'micro-bump bonding method' [Hatada *et al.* 1988] and used by Semiconductor Research Center, Osaka, Japan for thermal heads and an LED printer head [Fujimoto *et al.* 1989].

Flip-chip Bonded Stacked Chips with Spacers

This approach is similar to the above approach except that spacers are used to control the distance between the stacked chips. This technique was developed and used by University of Colorado and University of California, San Diego to fix a glass containing a ferroelectric liquid crystal on the top of the VLSI chip [Lin *et al.* 1995, Lee 1994] as shown in Figure A.16.

Microbridge Springs and Thermomigration Vias

Microbridge springs method involves the use of microsprings to achieve the vertical interconnections between stacked ICs, as shown in Figure A.17. This method was developed and used by Hughes in the design of 3D parallel computers for real time data and image processing and avionics for F-14, F-15, F/A-18, AV-8B, B-2 aircrafts [Crowley 1993e]. The same technique can be used for MCMs and is also relevant to the methods presented in section A.3.4.

A.3.3 Periphery Interconnection between Stacked MCMs

This is a method where vertical interconnections between stacked MCMs are realised on the stack's periphery. There are three main variants of this method as follows:

Solder Edge Conductors

This is similar to the solder edge conductor for ICs, discussed in section A.3.1. However, in this case the vertical interconnections are performed between MCMs rather than ICs. There are two variants of this method:

- *Solder dipped stacks to create vertical conductors on edge:* This technique is similar to the solder dipped stacks to create vertical conductors on edge technique discussed in section A.3.1 with the exception that MCMs are used to form the stack. This technique was used by Trymer in the development of a guidance system for hyper-velocity projectiles [Schroeder 1992, Schroeder 1993].

- *Solder leads on stacked MCMs:* After each MCM is packaged separately they are stacked with the leads formed to allow stacking as shown in Figure A.18, then soldered for permanent mounting. Matsushita Electronic Components has used this method in the design of high density SRAMs and DRAMs by using 2-8 layer stack. This method is referred to as 'Stacked QFP- format MCMs' because the leads on the bottom board are formed as a quad-flat pack package [Crowley 1993f].

Thin Film Conductors on Face-of-a-Cube

- *HDI-thin film interconnect laminated to side of stack:* The vertical interconnects are realised along the sides of the stack using the same HDI process used in the substrate. The sides are laminated then patterned using a chemical process called 'electroplated photoresist.' A schematic diagram of this method is shown in Figure A.19. This technique was developed and used by General Electric in the design of high density memories and other application specific integrated circuits (ASICs) [Saia *et al.* 1994, Eichelberger & Wojnarowski 1991].

- *Direct laser write traces on epoxy cube face:* This method of interconnection is similar to the one discussed in section A.3.1 except that MCMs are used in the stack instead of ICs. Thomson-CFS is the company who developed for both MCMs and ICs stacking and called it 'MCM-V^{TM}'.

Blind Castellation Interconnection

In this approach a semicircular or crown-shaped metallised surface (Castellation) is used for making vertical interconnections between the stacked MCMs as shown in Figure A.20. This method was used by Harris and CTS Microelectronics in the design of high density memory modules [Palmer & Newton 1993, Vitriol & Palmer 1993, Knopf 1996].

Wire Bonded Stacked MCMs

This approach is similar to the wire bonded stacked chips technique discussed in section A.3.1, except MCM-Ds are used in the stack. This approach was developed and used by CENG for designing a 1 Gbit mass memory module [Massit & Nicolas 1995].

A.3.4 Area Interconnection between Stacked MCMs

This is a method were interconnection between stacked MCMs are not bonded to the stack periphery. Such methods provide higher interconnection density between stacked elements. The following are variants of such vertical interconnections:

Arrays of Contacts between MCMs with through hole vias

In this method, an array of contacts are used to provide the vertical interconnections between stacked MCMs. There are six variants of this method as follows:

- *Fuzz buttons in plastic spacer and filled vias in substrate:* In this method MCMs are stacked with an intermediate layer called the spacer or fuzz buttons board [Pan *et al.* 1995]. This layer has a precision plastic spacer to provide clearance for chip and bond, and fuzz buttons to provide interconnection by applying a mating force on the stacked MCMs as shown in Figure A.21. Fuzz buttons are physically made of fine gold 'wire wool' and the integrity of a contact made by the contact of two of these wool pads is surprisingly good. This method is developed by E-Systems and used by E-Systems and Norton Diamond Film for stacking MCMs with diamond substrates [Schaefer *et al.* 1993, Moravec *et al.* 1993] and also used by Irvine Sensors in a low cost compact DSP [DeCaro *et al.* 1994].

- *Elastomeric[2] connectors with electrical feedthroughs:* The vertical interconnections in this method are implemented by a combination of 'electrical feedthroughs' and elastomeric connectors. The 'electrical feedthroughs' are premanufactured elements[3] that are mounted into a laser structured substrate by an embedding technique.

A schematic diagram of this method is shown in Figure A.22. This method was developed by the Research Center of Microperipheric Technologies at the Technical University of Berlin [Ehrmann *et al.* 1995, Ehrmann *et al.* 1995]. In addition, Texas Instrument has used a variant of this method in the design of a high performance parallel computer called 'Aladdin Parallel Processor' [Terrill 1995].

- *Compliant anisotropic conductive material:* This method uses an anisotropic conductive material that is electrically conductive through its thickness, but nonconductive in its length and width. A spacer is used to provide additional interconnections, clearance for wirebond loop height, and cooling channel height as shown in Figure A.23. This method was developed and used by AT&T in the design of a 1 GFLOP multiprocessor array using 3D MCM technology [Segelken *et al.* 1992].

- *Microbridge springs and thermomigration vias:* Refer to section A.3.2 for the technique description.

- *Solder balls array on top and bottom of substrate layers:* This method involves using a solder balls array on the top and bottom of a substrate to provide the vertical interconnect. The bottom balls are used to interconnect the stacked MCMs to a PCB by applying pressure on the stack, while the top solder joints are used to provide interconnection between the stacked MCMs as shown in Figure A.24 [Crowley 1993g, Lin 1992]. This method has been patented by Motorola but has not been used in production.

[2]An elastomer is a plastic material that at room temperature can be stretched repeatedly to at least twice its original length and, upon release of the stress, will return with force to its approximate original length.

[3]These elements are small silicon strips taken from a processed wafer, carrying straight, parallel conductor lines inside a polymer dielectric on both sides, then cut into strips orthogonal to the metal fibres.

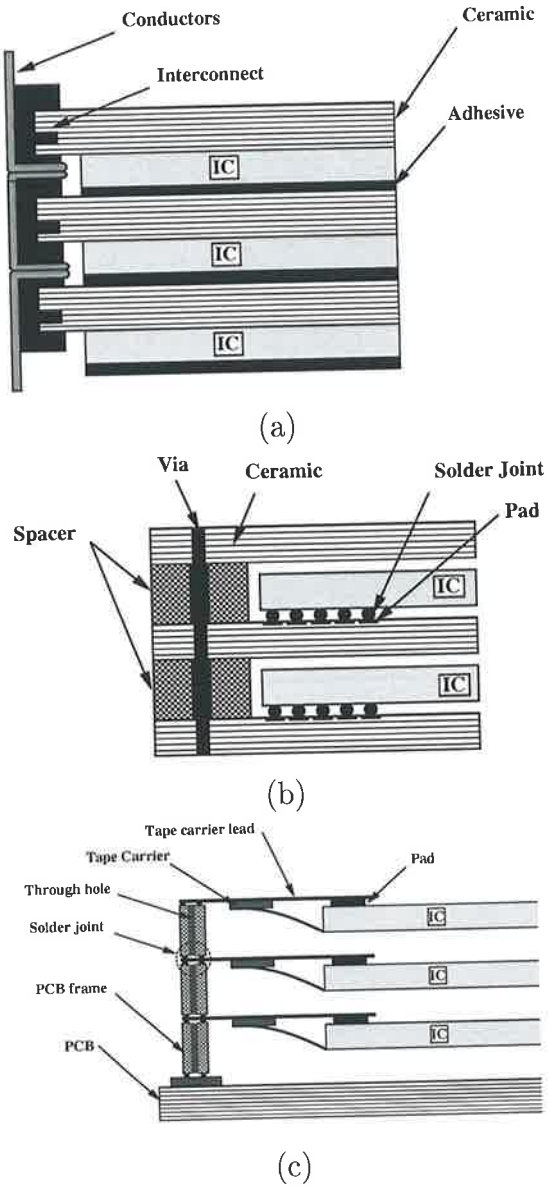

Figure A.7. Solder edge conductors vertical interconnections. This graph shows three variants of the solder edge conductors vertical interconnections. (a) Solder edge contacts. (b) Solder filled via. (c) Stacked PCB leadframes.

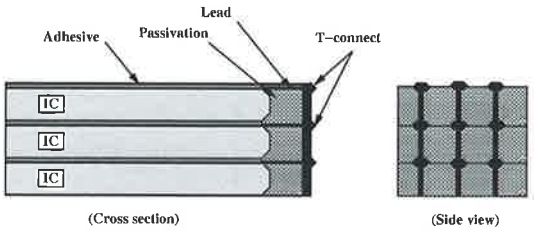

Figure A.8. A thin film metal "T-connects" for vertical interconnections. This graph shows a side and a cross sectional view of T-connects vertical interconnections.

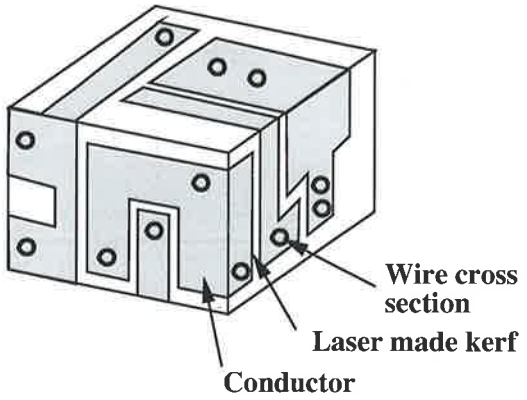

Figure A.9. Direct laser writing process. This graph shows how direct laser writing process is used to implement vertical interconnections for 3D structures.

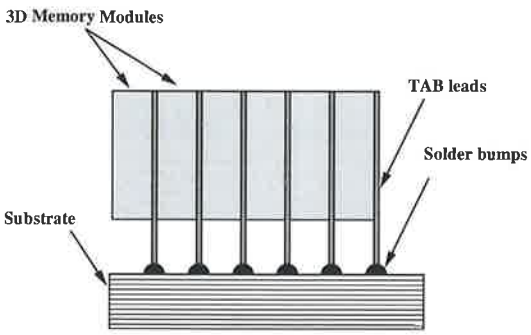

Figure A.10. TAB leads soldered to bumps. This graph shows Texas Instruments array TAB leads soldered to bumps on a silicon substrate.

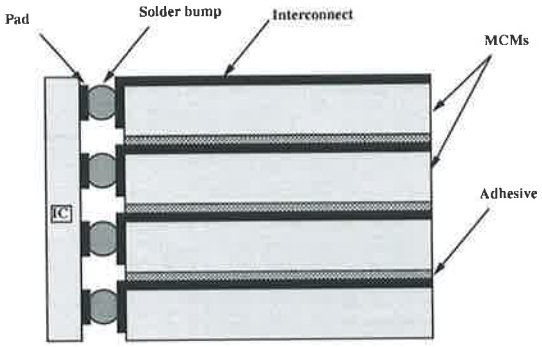

Figure A.11. Flip bonded chip to stacked MCMs. The graph shows a vertical interconnection method where a chip is flip bonded to the side of the stacked MCMs.

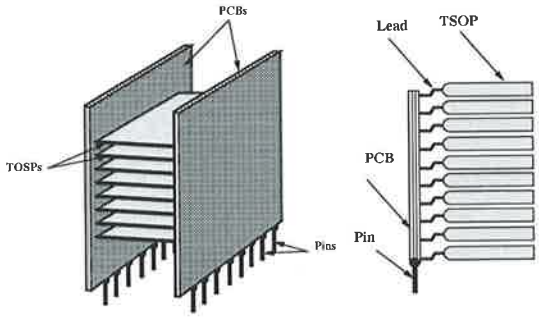

Figure A.12. PCB solder to TSOPs. The left diagram shows a PCB solder to TSOPs. The right diagram shows a cross sectional view of the left schematic.

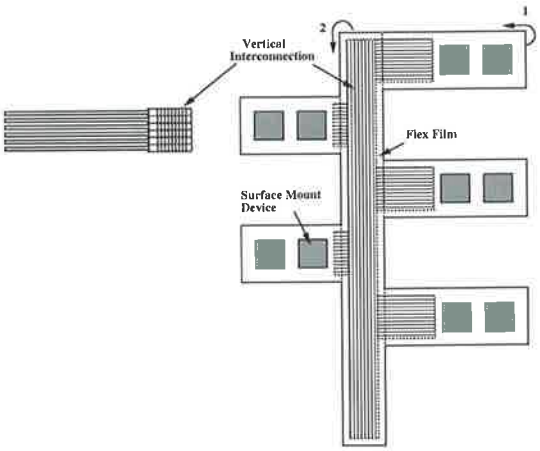

Figure A.13. Flex type vertical interconnects. The schematic diagram shows how ICs are stacked and interconnected using a flex type material.

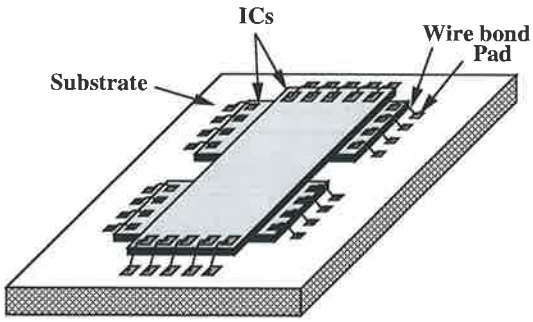

Figure A.14. Wire bonding interconnection. The diagram shows a vertical interconnection approach using wire bonding techniques.

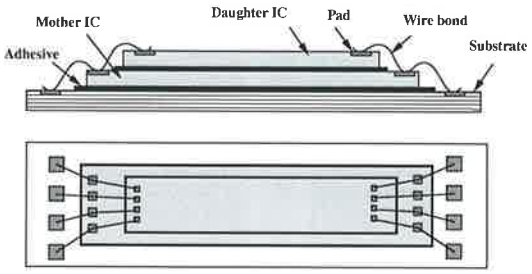

Figure A.15. Stacked chips interconnected using wire bonding. The upper schematic diagram of two chips stacked and interconnected using wire bonding. The lower diagram shows a top view of the upper schematic diagram.

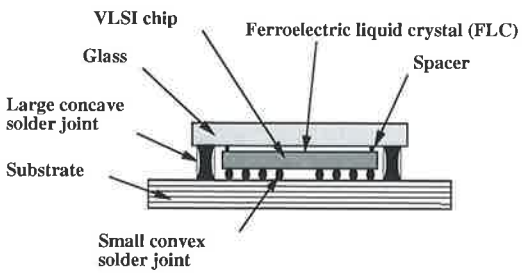

Figure A.16. Stacked chips using flip-chip technology. The schematic illustrates how two chips are stacked using flip-chip technology.

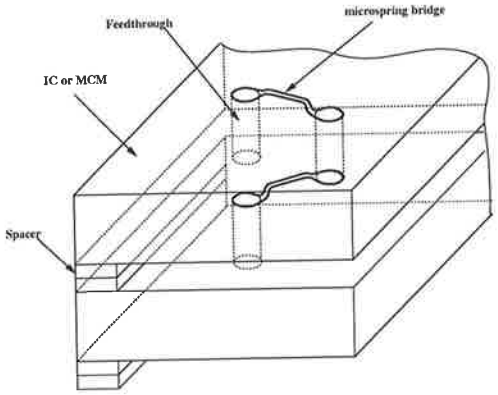

Figure A.17. Microspring interconnection. The schematic illustrates the use of Hughes' microspring for vertical interconnection.

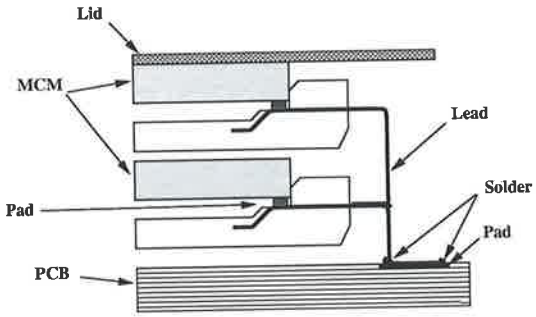

Figure A.18. Solder leads on stacked MCMs. The diagram illustrates a soldered leads vertical interconnection method on stacked MCMs. This method is a variant of the solder edge conductors method discussed in section A.3.1.

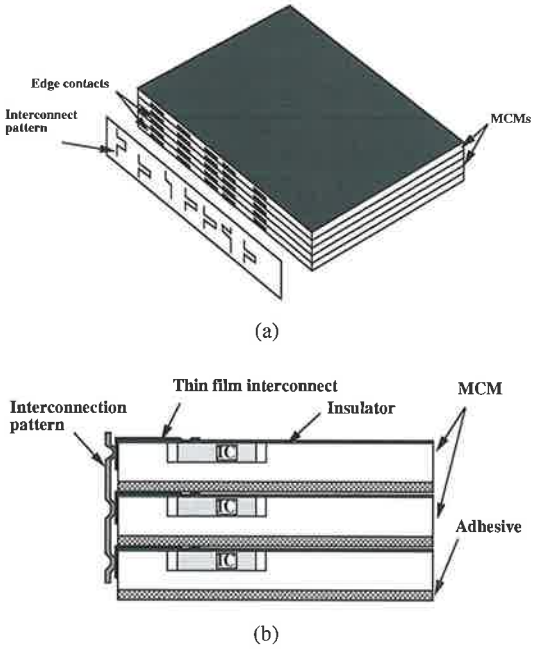

Figure A.19. Edge interconnection on the sides of the cube The (a) diagram illustrates GE method for stacking MCMs with edges interconnected on the sides of the cube. (b) Shows a cross sectional view of (a).

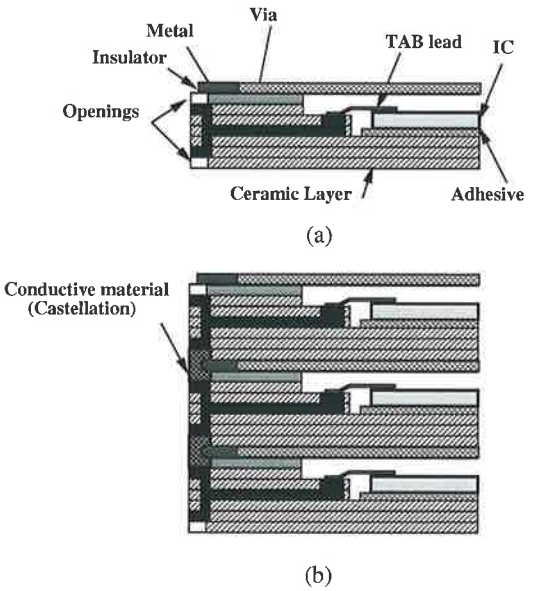

Figure A.20. Blind castellation vertical interconnection. The (a) schematic diagram illustrates an MCM stacking with the blind castellation method. (b) A schematic diagram of three MCMs stacked using the blind castellation method.

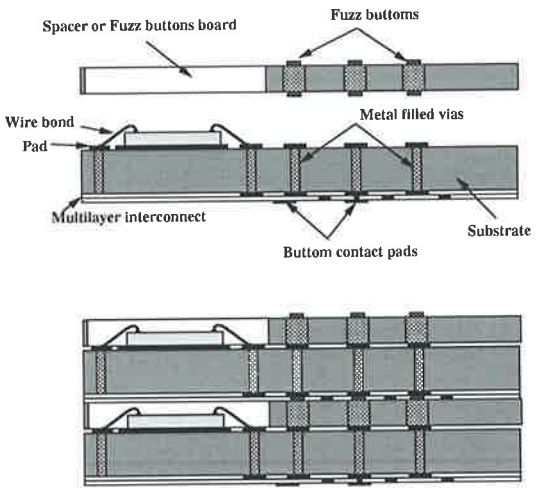

Figure A.21. Array contacts between MCMs. The upper schematic diagram shows an arrays of contacts between MCMs with through-hole vias. The lower diagram how two MCMs are stacked by applying a mating force.

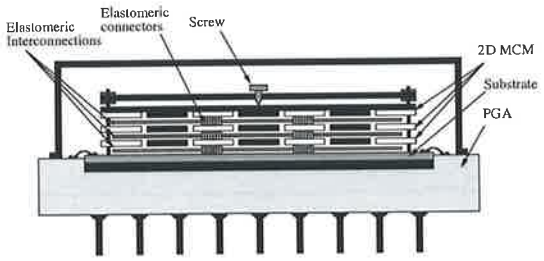

Figure A.22. A schematic diagram of TUB stacking technology. This diagram shows the uses of elastomeric material for vertical connections [Ehrmann *et al.* 1995].

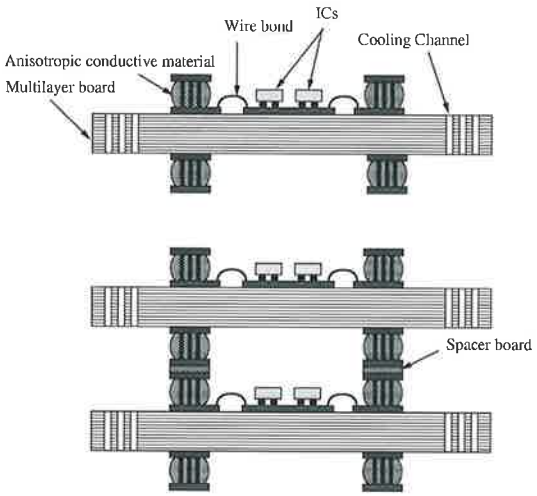

Figure A.23. Vertical interconnections using anisotropic conductive material. The upper schematic diagram illustrates vertical interconnection using an anisotropic conductive material. The lower diagram shows 2 MCMs stacked using this method.

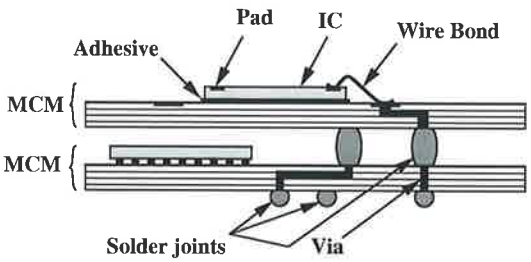

Figure A.24. Solder balls for area interconnect stacking. The diagram illustrates how to stack MCMs using solder balls arrays on top and button of substrate layers.

- *Stacked silicon wafers with filled vias:* In this method, vertical interconnections are formed using vias etched through the entire wafer and then filled with metal. The bottom side of the filled via contacts the top surface of a metal pad on the adjoining wafer as shown in Figure A.25. The filled vias are connected by applying pressure on the stack. This method was developed and used by Micron Technology for high density data storage using stacked non-diced wafers. Another wafer stacking approach was used by Lockheed Missiles & Space Company in the design of infrared signal processors [Pearson 1994, Malek & Pearson 1993]. However, in Lockheed approach the stacking is achieved by flip-wafer and achieving the interconnection using solder joints.

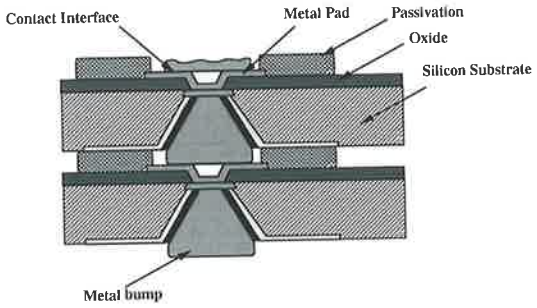

Figure A.25. Wafer scale stacking. The diagrams illustrates how two wafers are stacked using filled vias method.

A.4 Limitations of 3D Packaging Technology

The 3D technology offers advantages for all types of electronic assemblies, including those for computer, military, automotive and telecommunication applications. However, there are trade-offs which need to be taken into account when using 3D technology in system design. These trade-offs are discussed in the following subsections.

A.4.1 Thermal Management

As the demand increases to build high performance systems, trends in electronic package design have moved toward larger circuit chips, higher number of I/O ports, increased circuit density, and improved reliability. Greater circuit density means increased power density (W/cm^2). The power density has increased exponentially over the past 15 years and it appears that it will continue to do so in the near future. As it is the case with

devices fabricated using 3D technology, the power density is high, so thermal management should be considered carefully in these devices and it could be used to distinguish between packaging technologies. The thermal management in 3D technology has been addressed in at two levels. The first level is at the system design level by trying to evenly distribute the thermal energy across the 3D device surface [Borden *et al.* 1995]. The second level is at the packaging level. This is achieved through one or a combination of the following approaches. Firstly, by using low thermal resistance substrates such as diamond [Moravec *et al.* 1993, McDonald *et al.* 1995] or Chemical Vapour Deposition CVD diamond [Lu 1994]. Secondly, by using forced air or liquid coolant to reduce the 3D device temperature. Thirdly, by using a thermally conductive adhesive and implementing thermal vias [DeKenipp *et al.* 1995] between the stacked elements to extract the heat from inside the stack to its surface. Even though, these methods are effective, however, it is believed thermal management will be more challenging with increased circuits densification.

A.4.2 Design complexity

Advances in interconnection technology have played a key role in allowing continued improvement in integrated circuit density, performance, and cost. Over the last 20 years, circuit density has increased by a factor of approximately 10^4. According to Gordon Moore, CEO of Intel, integrated circuits will roughly double in density every device generation. One generation lasts about 18 months, resulting in a straight-line on a log scale as shown in Figure A.26 [Kelly *et al.* 1995]. As a result, feature size and resolution of geometries used in production follow the same trend with feature size reductions of about 20% per component generation. At the same time, increased functional integration has lead to larger chip sizes, which has required materials development for increased wafer size and equipment development for handling larger wafers.

Currently, more integrated circuits are packaged together in 2D and 3D forms. In both cases that would increase the complexity of the overall system. A large number of systems have been implemented using the 2D form, and have demonstrated that such complexity can be managed. However, a fewer number of systems and devices have been implemented using 3D technology, proving nevertheless that such devices or systems are manageable, although complex. The increased in complexity can be managed by designing and developing software to cope with the increasing system complexity.

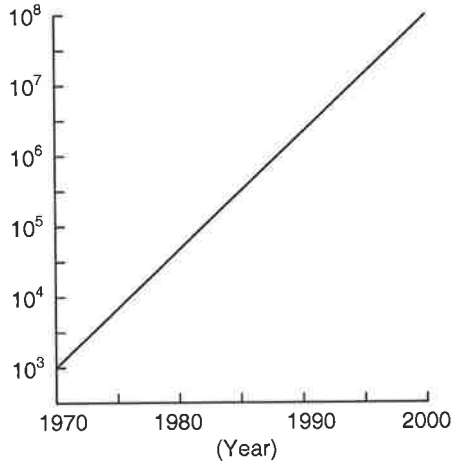

Figure A.26. Moore's Law for active element density. The y-axis refers to the number of transistors per unit area.

A.4.3 Cost

With the emergence of any new technology, there is an expected high cost involved in using it. As it is the case with the 3D technology, the cost involved for the time being is high, due to the lack of infrastructure and the reluctance of manufacturers to change to new technologies for reasons associated with risk factors. Moreover, such cost is function of the device complexity and the needed requirements. Further more, the non-returnable engineering (NRE) cost is also very making it even harder to use 3D technologies.

A.4.4 Time to Delivery

'Time-to-Delivery' is the time needed to fabricate a product. As expected the 'time to delivery' is function of the system complexity and requirements. In case of 3D packaging technology, this time can be than the time taken by any other packaging technologies discussed before. An inquiry to some manufacturers who provide 3D packaging, revealed that the 'time-to-delivery' is 6-10 months, depending on the size and complexity of the 3D device which is 2-4 times longer than the time needed for MCM-D technology.

A.4.5 Design Software

Design software is one of the problems facing 3D technology. Most manufacturers use their own design tool kits, which give the designers the ability to implement their design in accordance with the vendor's manufacturing requirements, while allowing the designers to

Table A.2. Institutions active in 3D packaging. This table lists most of the companies and institutions working in the area of bare die and packaged die stacking 3D packaging [Crowley 1993h].

Bare Die stacking		Packaged Die stacking	
Standard ICs	**Custom ICs**	**Standard Package**	**Custom Package**
Actel	IBM	Mitsubishi	CTS
Implex	Irvine Sensors	Thomson-CFS	Dense-Pac
Matsushita (MEI)	Fujitsu	Samsung Electronics	Grumman
Thomson-CFS	Hughes	Texas Instruments	Harris
Hitachi & Intel	Texas Instruments	nChip, Inc.	Hitachi
Valtronic, Inc.	Matsushita	NEC Corp.	Motorola
AT&T		Irvine Sensors	RTB Technology
		Cray Research, Inc.	Staktek
		Harris	Trymer

focus on the design without getting involved with manufacturing and interfacing details. However, most of these design kits are not fully integrated or implemented in softwares that are easily accessible. Hence, for some of the manufacturers there is a need to port their design rules into available softwares or to buy their software. In the first case, there is a time and risk involved, while in the second the cost involved is the main issue, adding to the cost of 3D device fabrication.

A.5 Discussion

Three dimensional packaging technology enhances most aspects of electronic systems such as size, weight, speed, yield and reduces power consumption. Moreover, due to the systematic elimination of faulty ICs during the assembly process of a 3D device, the yield, reliability and robustness of the end device will be high compared to a discrete implementation of such device. Currently, 3D packaging is limited by a number of factors. Some of these limitations such as thermal management are a result of densification, others are due to technological limitations, such as via diameter, line width, via pitch, and line spacing. It is expected that the effect of such limitations will decrease with the advances in packaging technology.

The main issues in 3D packaging are the quality, the length and the number of vertical interconnections used to interconnect the ground, power and I/O signals between the

Table A.3. Institutions active in 3D packaging. This table lists most of the companies and institutions working in the area of MCM and wafer stacking 3D packaging.

MCM stacking	Wafer stacking
Custom Modules	**Custom Wafers**
AT&T	Mass Memory Technology
Raytheon (E-Systems)	Hughes
General Electric	ATT
Hughes	NTT and Thomson-CSF
Matra Marconi Space	General Electric &
Matsushita (MACO)	USAF Philips Lab.
Motorola	
Honeywell and Coors	
RCMT@Berlin Uni	
Lockheed	

stacked chips or MCMs. As seen from the above discussion, these issues have been investigated by a lot of companies and manufacturers who have developed different techniques. From our research point of view, the technology which provides the largest number and the highest quality vertical interconnections should be favoured, such as the ones described in sections A.3.4 and A.3.2. Another important issue that has risen as part of this study is the accessibility to manufacturers who provide 3D technology. Even though many companies are active in 3D research and technology, few offer standard 3D products and even fewer provide access to their packaging technology. As part of this study, the issue of accessibility has been addressed by establishing links with manufacturers who provide 3D packaging technologies.

As seen from the above discussion, there are four distinct methods of stacking electronic circuits. Tables A.2 and A.3 provide a summary of most of the companies working in the area of 3D packaging, classified according to the type of elements to be stacked. Some of these companies are not mentioned in the report, however, they are listed for completeness. Moreover, Tables A.4 to A.7 summarise the companies working in the area of 3D packaging with their technology applications, accessibility to us, countries, and the vertical interconnection methods used in their packaging techniques.

A.6 Conclusions

Significant savings in power consumption, weight and physical volume can be achieve by adopting the 3D packaging approach. A number of emergent bare dice and MCM stacking approaches have been reviewed. The choice of 3D technology depends largely on the application. For stacking memory ICs, where the power dissipation is low and all the ICs are of matched size, 'pancake' bare die stacking produces the most efficient results.

For the special case of *area* rather than *peripheral* connections (ie. a regular array connected to a processor on a pixel-by-pixel basis), 'loaf' rather than 'pancake' bare dice stacking is preferable. The reason for this is that loaf stacking avoids the need for through-substrate-vias and hence saves silicon space and cost.

Bare dice stacking techniques that require little or no silicon post processing and have the fewest number of fabrication process steps are the most attractive. The number of steps required for bare die stacking varies dramatically from vendor to vendor from the order of 5 to 50 steps!

In summary, bare dice technology is most suitable when dealing with repetitive stacking of identical ICs. When dealing with a range of ICs of different sizes, the MCM stacking approach tends to be the most efficient in terms of cost and complexity. The most efficient, in terms of physical volume, appears to be the technique where thin MCM flex boards are stacked and then potted in epoxy. This technique also is advantageous for large volume production, where reel-to-reel flexboard can be utilised, many units can be potted in parallel and the resulting strip can then be sliced up. In cases where military/aerospace standards disallow organic materials (such as epoxy), particular attention for robustness and heat-sinking is required, then the various ceramic MCM stacking techniques can be employed. In this case the fuzz button approach appears to be the most widely used, due to its ability for high density vertical interconnect (about a factor of 3 better the surface mount connectors).

Finally, 3D stacking techniques place upon the system designer more demands in terms of thermal and crosstalk modelling – also design for testability and a carefully structure test procedure are crucial. Vendors that thoroughly address simulation and test issues, and that focus on reducing the number of fabrication steps of their stacking technology will meet the demands of the system designer.

Table A.4. Evaluation of companies according to their method of periphery interconnection between stacked ICs.

Company	Application	Country	Interconnection Technique
Matsushita	Memories	Japan	Stacked TAB carrier (PCB)
Fujitus	Memories	Japan	Stacked TAB carrier (leadframe)
Dense-Pac	Memories	USA	Solder dipped stacks to create vertical conductors on edge
Micron Technology	Memories	USA	Solder filled holes in chip carriers and spacers
Hitachi	Memories	Japan	Solder connections between plated through hole
Irvine Sensors	Memories/ASICs	USA	Thin film 'T-connects' and sputtered metal conductors
Thomson-CFS	Memories/ASICs	France	Direct laser write traces on epoxy cube face
Mitsubishi	Memories	Japan	PC boards soldered on two sides of TSOP packages
Texas Instruments	Memories/ASICs	USA	Array of TAB leads soldered to bumps on silicon substrate
Grumman Aerospace	ASICs	USA	A flip-chip bonded to faces of the stack
General Electric	ASICs	USA	Folded flex circuits
Harris	ASICs	USA	Folded flex circuits
MCC	ASICs	USA	Folded flex circuits
Matra Marconi	Memories	France	Wire bonded to an MCM substrate directly
Voltonic	ASICs	USA	Wire bonded to a substrate through an IC

Table A.5. An evaluation of companies which provides area interconnection between stacked ICs.

Company	Application	Country	Interconnection Technique
Fujitsu	ASIC	Japan	Flip-chip bonded Stacked Chips without spacers
University of Colorado & UCSD	Optoelectronic	USA	Flip-chip bonded Stacked Chips with spacers
Hughes	ASIC	USA	Microbridge springs and thermomigration vias

Table A.6. An evaluation of companies which provides periphery interconnection between stacked MCMs.

Company	Application	Country	Interconnection Technique
Matsushita	Memories	USA	Solder leads on stacked MCMs
General Electric	ASIC	USA	HDI-thin film interconnect laminated to side of stack
Harris	Memories	USA	Blind castellation interconnection
CTS Microelectronics	Memories	USA	Blind castellation interconnection
Trymer	Guidance Systems	USA	Solder dipped stacks to create vertical conductors on edge

Table A.7. An evaluation of companies which provides area interconnection between stacked MCMs.

Company	Application	Country	Interconnection Technique
Raytheon (E-Systems)	ASIC	USA	Fuzz buttons in plastic spacer and filled vias in substrate
Technical University of Berlin	ASIC	Germany	Elastomeric connectors with electrical feedthroughs
AT&T	ASIC/ multiprocessor array	USA	Compliant anisotropic conductive material
Hughes	ASIC/avionics	USA	Microbridge springs and thermomigration vias
Motorola	Not in Use	USA	Solder balls on top and bottom of substrate layers
Micron Technology	Memories	USA	Stacked silicon wafers with filled vias
Lockheed	ASIC/ IR processors	USA	Stacked silicon wafers with filled vias

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Appendix B

Symmetrical Level 13 Model Parameters

This appendix lists the modified Level 13 model parameters for Orbit Semiconductors 2 μm double poly, double metal process. In these model parameters, the pMOS transistor model was changed to match the nMOS transistor parameters.

```
*
*PROCESS=ORBIT
*RUN=n53b
*WAFER=09
*Gate-oxide thickness= 407 angstroms
*Geometries (W-drawn/L-drawn, units are um/um) of transistors measured were:
* 3.0/2.0, 6.0/2.0, 18.0/2.0, 18.0/5.0, 18.0/25.0
*Bias range to perform the extraction (Vdd)=5 volts
*DATE=2-May-1995
*
*NMOS PARAMETERS
*
.MODEL nfet NMOS LEVEL=13 VFB0=
+ -8.29007E-01,-1.35771E-02,-1.81384E-01
+  7.70786E-01, 0.00000E+00, 0.00000E+00
+  1.06507E+00, 1.18533E-01, 6.35911E-01
+ -1.44389E-02, 1.37074E-01, 8.51944E-02
+ -3.91561E-03, 2.29739E-02,-3.26690E-03
+  5.64701E+02,1.06254E-000,3.70459E-001
```

```
+  4.86784E-02, 5.94004E-02,-4.42670E-02
+  5.60664E-02, 3.49094E-01,-1.71555E-01
+  1.25518E+01,-2.07815E+01, 5.34046E+01
+  8.06272E-04,-1.27494E-02, 4.73834E-03
+  6.44543E-04,-2.31663E-03,-3.49284E-03
+  1.19246E-03,-1.01329E-02, 3.32873E-02
+ -1.47002E-03, 2.03770E-02,-2.66934E-02
+  5.46897E+02, 2.76101E+02, 1.15054E+02
+  1.93278E+00, 6.86714E+00, 6.02697E+01
+ -1.75164E+00, 3.82394E+01, 1.43570E+01
+  2.23408E-03, 2.73114E-02, 1.44605E-02
+ 4.07000E-002, 2.70000E+01, 5.00000E+00
+ 6.76125E-010,6.76125E-010,4.37628E-010
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 18.8,    3.587400e-04,    5.001400e-10,    1e-08,    0.8
+ 0.8,    0.500184,    0.406471,    0,0
*
* Gate Oxide Thickness is 407 Angstroms
*
*
*PMOS PARAMETERS
*
.MODEL pfet PMOS LEVEL=13 VFB0=
+ -8.29007E-01,-1.35771E-02,-1.81384E-01
+  7.70786E-01, 0.00000E+00, 0.00000E+00
+  1.06507E+00, 1.18533E-01, 6.35911E-01
+ -1.44389E-02, 1.37074E-01, 8.51944E-02
+ -3.91561E-03, 2.29739E-02,-3.26690E-03
+  5.64701E+02,1.06254E-000,3.70459E-001
+  4.86784E-02, 5.94004E-02,-4.42670E-02
+  5.60664E-02, 3.49094E-01,-1.71555E-01
+  1.25518E+01,-2.07815E+01, 5.34046E+01
+  8.06272E-04,-1.27494E-02, 4.73834E-03
```

```
+  6.44543E-04,-2.31663E-03,-3.49284E-03
+  1.19246E-03,-1.01329E-02, 3.32873E-02
+ -1.47002E-03, 2.03770E-02,-2.66934E-02
+  5.46897E+02, 2.76101E+02, 1.15054E+02
+  1.93278E+00, 6.86714E+00, 6.02697E+01
+ -1.75164E+00, 3.82394E+01, 1.43570E+01
+  2.23408E-03, 2.73114E-02, 1.44605E-02
+ 4.07000E-002, 2.70000E+01, 5.00000E+00
+ 6.76125E-010,6.76125E-010,4.37628E-010
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 18.8,    3.587400e-04,    5.001400e-10,    1e-08,    0.8
+ 0.8,    0.500184,    0.406471,    0,0
*
*N+ diffusion::
*
.MODEL PC1_DU1 R
+ RSH=18.8 COX=0.000359 CAPSW=5e-10 W=0 DW=0
*
*P+ diffusion::
*
.MODEL PC1_DU2 R
+ RSH=68.5 COX=0.000208 CAPSW=8.01e-11 W=0 DW=0
*
*METAL LAYER -- 1
*
.MODEL PC1_ML1 R
+ RSH=0.05 COX=2.6e-05 CAPSW=0 W=0 DW=0
*
*METAL LAYER -- 2
*
.MODEL PC1_ML2 R
+ RSH=0.03 COX=1.3e-05 CAPSW=0 W=0 DW=0
```

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Appendix C

A Statistical Analysis of MOS Mismatch

One of the biggest problems facing the analog designer is process variation during circuit fabrication. As a result the performance and sometimes the functionality of an analog circuits is affected. Reducing these process variations at the fabrication level is beyond the circuit designer's reach, however the effect of these variations can be reduced through proper circuit design and thorough characterisation of the process to be used for fabrication. Statistical data on a process variation for a CMOS technology from a foundry is usually not provided. Instead, *global process parameters* are commonly provided as *skew parameters*. However, these parameters are useful for digital designers to calculate the performance and yield of their digital circuits. While, in the case of analog designers, it is important not to design circuits that rely on absolute process parameter values, but rather the relative difference of the process parameters. Hence local process variations are more important than global process variations from an analog designer's point of view.

The following paragraphs present a *statistical analysis* approach to reduce the effect of process variations on the MOS transistor drain current due to local and global process variation. The analysis shows briefly that the random error variation in CMOS processes can be reduced by increasing the MOS transistor size, assuming uncorrelated errors.

Shyu *et al.* [1984] report on the random error effect in matched MOS capacitors and current sources, classifying the random error effects into four categories as follows:

- *Random Errors Due to Edge Effect:* This effect is due to random length and width variations of the MOS transistor as a result of fabrication process. The relative current error due to the local and global random variation of this effect assuming a simple transistor model is given by

$$\left.\frac{\Delta I}{I}\right|_e = \sqrt{\left(\frac{\sigma_{g_L}^2}{\overline{L}^2} + \frac{\sigma_{g_W}^2}{\overline{W}^2}\right) + \frac{2d_e}{\overline{L}\overline{W}}\left(\frac{\sigma_{l_L}^2}{\overline{L}} + \frac{\sigma_{l_W}^2}{\overline{W}}\right)}, \tag{C.1}$$

where $\overline{L}$ and $\overline{W}$ are the nominal transistor length and width, respectively. σ_{g_W} and σ_{g_L} are the standard deviation of the $\overline{W}$ and $\overline{L}$ due to global variation, respectively. σ_{l_W} and σ_{l_L} are the standard deviation of the W and L due to local variation, respectively. d_e is the is correlation radius of the local length variation.

Equation C.1 shows that the error in the drain current due to edge effect random errors can be reduced by increasing the device size.

- *Random Errors Due to Surface-State-Charge and Ion-Implanted-Charge Effects:*

  The adjustment of a MOS transistor threshold voltage is usually carried out using ion-implantation, where charges are used to shift the threshold voltage which is analytically given by

$$\overline{V}_T = \phi_{MS} + 2|\phi_F| + \frac{\overline{Q}_D}{\overline{C}_{ox}} - \frac{\overline{Q}_{ss}}{\overline{C}_{ox}} + \frac{\overline{Q}_{ii}}{\overline{C}_{ox}}, \tag{C.2}$$

  where $\overline{V}_T$ is the nominal threshold voltage, ϕ_{MS} is the gate-semiconductor function difference, ϕ_F is the Fermi potential in the bulk, $\overline{C}_{ox}$ is the nominal oxide capacitance per unit area. $\overline{Q}_D, \overline{Q}_{ss}$ and $\overline{Q}_{ii}$ are the nominal space charge, surface state charge and ion implanted charge densities per unit area, respectively.

  The relative current error due to both local and global variations of Q_{ss} and Q_{ii} is given by

$$\left.\frac{\Delta I}{I}\right|_q = \frac{2}{\overline{C}_{ox}(V_{gs} - \overline{V}_T)}\sqrt{\left(\sigma_{g_{q_{ss}}}^2 + \sigma_{g_{q_{ii}}}^2\right) + \frac{4d_q^2}{\overline{L}\,\overline{W}}\left(\sigma_{l_{q_{ss}}}^2 + \sigma_{l_{q_{ii}}}^2\right)}, \tag{C.3}$$

  $\sigma_{g_{q_{ii}}}$, $\sigma_{l_{q_{ss}}}$ and $\sigma_{l_{q_{ii}}}$ are the standard deviations of the global surface-state charge, global ion-implanted charge, local surface state charge and the local ion-implanted charge, respectively. d_q is the correlation radius of local charge variation, $\overline{C}_{ox}$ is the nominal oxide capacitance per unit area and V_{gs} is the gate to source voltage.

  Equation C.3 shows that the random errors due to surface state charge and ion implanted charge effects can also be reduced by increasing the transistor size.

- *Random Errors Due to Oxide Effects:* The random fluctuation of the oxide thickness has an effect on the transistor drain current by affecting the gain factor and the threshold voltage. The relative current error due to both local and global variations of the oxide thickness is given as

$$\left.\frac{\Delta I}{I}\right|_{ox} = \frac{1}{\overline{t}}\left[1 + \frac{2(Q_D - \overline{Q}_{ss} + \overline{Q}_{ii})}{\overline{C}_{ox}(V_{gs} - \overline{V}_T)}\right]\sqrt{\sigma^2_{g_{ox}} + \frac{2d^2_{ox}\sigma^2_{l_{ox}}}{\overline{L}\,\overline{W}}} \tag{C.4}$$

where $\overline{t}$ is the nominal gate oxide thickness, and V_{gs} is the gate to source voltage. $\sigma_{l_{ox}}$ and $\sigma_{g_{ox}}$ are the local and the global standard deviation of the oxide thickness, respectively. Equation C.4 shows that the relative current error due to oxide effect decreases with oxide thickness increase. However, according to Equation C.3, the relative error current will increase as a result on increasing the oxide thickness per unit area. Therefore, the reduction of the random errors due to surface state charge effects and oxide thickness are process dependent an has less dependence on the transistor area.

- *Random Errors Due to Channel Mobility Effects:* This effect is a result of the random impurity scattering and lattice scattering mechanisms. The effect of channel mobility on the relative current error due to local and global variations is given as

$$\left.\frac{\Delta I}{I}\right|_{\mu} = \frac{1}{\overline{\mu}}\sqrt{\sigma^2_{g_\mu} + \frac{4d^2_{l_\mu}\sigma^2_{l_\mu}}{\overline{L}\,\overline{W}}}, \tag{C.5}$$

where $\overline{\mu}$, σ_{g_μ} and σ_{l_μ} are he nominal channel mobility, the global and local standard deviations of the channel mobility, respectively. d_{l_μ} is the correlation radius of the local mobility variation.

Equation C.5 shows that the relative current error due to channel mobility variation is reduced by increasing the channel mobility. The same conclusion can also be obtained based on Equation C.3. However, this parameter is process dependent and cannot be used by the circuit designer to improve device matching. In the other hand, this conclusion can be employed by the circuit designer in selecting a fabrication process for a choice between different process options.

In conclusion, the statistical analysis of the different process parameters shows that by increasing the transistor size a better matching can be obtained.

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Appendix D

Very Low Frequency, Low Power Oscillators

D.1 Introduction

Oscillators are basic building blocks in a wide range of analog and digital applications. They can be classified in a number of ways. For example, they can be classified according to their frequency of oscillation as high, medium and low oscillators, or according to the output waveform type as square-wave, sine-wave, etc. The oscillator type discussed is this chapter is the integrator oscillator. This scillator consists of two switched current sources, a capacitive load and a dual voltage reference comparator. The combination of the switched current sources and the capacitive load forms an integrator. As the dual reference comparator in the design of the integrator oscillator can be replaced by a Schmitt trigger circuit. This type of oscillator we referred to as a 'Schmitt–oscillator,' or a integrator-oscillator. A simplified schematic diagram of the Schmitt-oscillator is shown in Figure D.1. An extra inverter is needed at the Schmitt trigger output to obtain the right phase at the input terminals of the switched current sources.

In RFID systems, the interest ranges from very low frequency oscillators (2 – 50 Hz) up to high frequency oscillators. The high frequency type is used in the generation of the carrier frequency needed for communication between the transponder system and the interrogator, while the use of very low frequency pulse oscillator is unique in the design of passive transponder systems to allow the detection of multiple transponders in the same field. This is achieved by exploiting the frequency diversity between different oscillators in different transponders to control the reply and silent durations of the transponders within the excited field.

Schmitt-oscillators are commonly used in CMOS technology because: (1) they are very well suited for integration; (2) they have a simple structure, (3) the frequency of oscillation can be adjusted and tuned using an electrical signal to form a voltage controlled or a current controlled oscillator, (4) they have a wide dynamic range of operation and (5) they do not require a startup circuit.

In this Appendix, a brief analysis of the Schmitt-oscillator is presented in Section D.2. A new technique for designing a Schmitt-oscillator is discussed and its application in the design of a new variant of the Schmitt-oscillator is discussed in Section D.3. Section D.4 presents experimental results for conventional type Schmitt-oscillator and the new oscillator.

D.2 Schmitt-Oscillators

The principle of operation of the Schmitt-oscillator shown in Figure D.1 can be described as follows. Assuming a zero charge across C_L, the voltage at the input of the Schmitt trigger circuit, V_C, is low, hence the output of the Schmitt trigger is high, forcing S_{ch} to switch 'ON' and S_{disch} to switch 'OFF.' Hence, C_L starts to charge linearly using current I_{ch}. Once the voltage at V_C reaches the Schmitt trigger V_{HL}, which is the input voltage at which the output of the Schmitt trigger switches from high to low, the output of the Schmitt trigger switches very rapidly from high to low, complementing the states of S_{ch} and S_{disch}. Now, C_L starts to discharge using I_{disch}. Once the voltage across C_L reaches the Schmitt trigger V_{LH}, which is the input voltage at which the Schmitt trigger output switches from low to high, the output of the Schmitt trigger changes its state. Then, the cycle continues with an initial voltage across C_L equal to V_{LH}. The oscillation frequency, f_o, of this oscillator can be written as

$$\frac{1}{f_o} = C_L V_{HW} \left(\frac{1}{I_{ch}} + \frac{1}{I_{disch}} \right), \tag{D.1}$$

where V_{HW} represents the hysteresis width of the Schmitt trigger circuit which is defined as the difference between V_{HL} and V_{LH}. To obtain a fully symmetrical square waveform from the oscillator the charging and discharging currents should be equal. i.e. $I_b = I_{ch} = I_{disch}$. So Equation D.1 can be written as

$$f_o = \frac{1}{T_o} = \frac{I_b}{2C_L V_{HW}}. \tag{D.2}$$

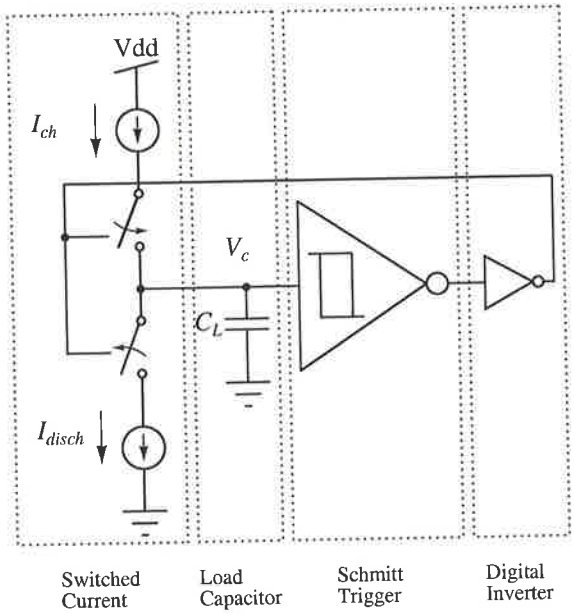

Figure D.1. Conventional integrator oscillator. This schematic shows a conceptional circuit diagram of an integrator-oscillator. The combination of switching current sources and the load capacitor forms the integrator and the Schmitt trigger is used to provide the required two switching points.

The highest frequency Schmitt-oscillator can deliver is obtained by maximising the ratio of I_b to $C_L V_{HW}$. It has been reported that an oscillation frequency in the range of 1 GHz can be achieved [Banu 1988, Razavi 1996]. Even though the challenge in most applications is in the design of high frequency oscillators, there is another challenge, namely the design of very low frequency oscillators. The low frequency limit is bounded by the smallest controlled current that can be generated on chip and the largest practical capacitor size that can be integrated on chip. For example, if the hysteresis width of the Schmitt trigger is 5/3 Volt, the smallest control current that can be generated is 1 nA and the largest practical capacitor size is set to 10 pF, using Equation D.2, the lowest obtainable oscillation frequency is 30 Hz. To obtain a lower frequency value either the current limit or capacitor size has to be stretched. An alternative solution is to use a digital frequency divider circuit. However, the use of a digital divider is costly in terms of silicon area as the average number of transistors in such circuits is around 20-24 transistors [Weste & Eshraghian 1985]. The solution proposed in this work is to extend the integration voltage of the integrator to be rail-to-rail [Al-Sarawi *et al.* 1997]. This technique is discussed in detail in Section D.3.

D.3 Extended Mode Schmitt-Oscillator

A new technique for designing a very low frequency oscillators is described through the design of a new variant of the Schmitt-oscillator called 'Extended Mode Schmitt Oscillator' and is referred to as EMSO. The EMSO has an oscillation period larger than the conventional Schmitt-oscillator, when using the same bias current and an equivalent capacitor size. This is achieved through using N integrators instead of one to extend the integration voltage from rail-to-rail rather than restricting it to the Schmitt trigger hysteresis width, as will be shown in the following analysis.

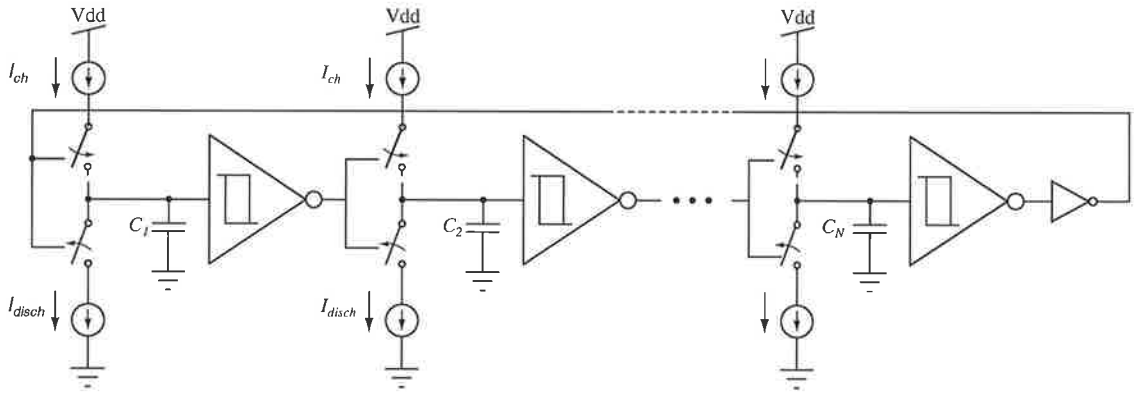

Figure D.2. Extended mode integrator oscillator (EMSO). This circuit diagram shows an N stages extended mode oscillators. Each stage is composed of an integrator and a Schmitt trigger circuit.

The new oscillator architecture is shown in Figure D.2. The oscillation frequency of the new oscillator as a result of using N integrators can be found using the resultant integration times, T_{o_e}, during the charging T_{ch} and discharge T_{disch} phases of the integrators. Firstly, during the charging period C_1 to C_N will be charging to V_{dd} using the constant current source I_{ch}. However, C_{i+1} will start charging when the voltage across C_i reaches the Schmitt trigger V_{LH} voltage. So, the charging times T_{ch} as function of the capacitor values can be written as

$$T_{ch} = \frac{V_{LH}}{I_{ch}} \sum_{i=1}^{N} C_i. \tag{D.3}$$

Secondly, using the same procedures the discharge time can be written as function of the Schmitt trigger V_{HL} voltage as

$$T_{disch} = \frac{V_{dd} - V_{HL}}{I_{disch}} \sum_{i=1}^{N} C_i. \tag{D.4}$$

So, using Equations D.3 and D.4, and assuming that $I_b = I_{ch} = I_{disch}$ and using the definition of the hysteresis width V_{HW} as the difference between V_{HL} and V_{LH} to simply the results. The oscillation period of the new oscillator T_{o_e} can be written as

$$T_{o_e} = \frac{2V_{HW}}{I_b} \left[\frac{V_{dd}}{2V_{HW}} + \frac{1}{2} \right] \sum_{i=1}^{N} C_i. \tag{D.5}$$

To show the increase in the oscillation period as a result of using the extended mode technique, Equation D.5 can be rewritten in terms of Equation D.2, with the assumption that $\sum_{i=1}^{N} C_i$ equals C_L in conventional Schmitt-oscillator. Hence, oscillation period of the EMSO, T_{o_e}, can be written in terms of ocillation period of the conventional Schmitt-oscillator T_{os} as

$$T_{o_e} = T_{os} \left[\frac{V_{dd}}{2V_{HW}} + \frac{1}{2} \right]. \tag{D.6}$$

Equation D.6 shows that the oscillation period of the EMSO will always be larger than the oscillation period of the conventional Schmitt-oscillator. For example, if the same values of I_b and V_{HW} in the example discussed in Section D.2 with C_T is set to 10 pF are used in calculating the oscillation frequency of EMSO, the resultant oscillation frequency is 15 Hz. So, the oscillation frequency is half that obtained using the conventional Schmitt-oscillator. This difference in frequency can be translated in terms of area reduction of the capacitor size needed, i.e. only a 5 pF capacitor is needed to obtain a 30 Hz oscillation. The true saving as a result in using this technique is less than 50% due to the overhead of using other Schmitt trigger circuits and switched current sources. So, the optimum number of integrators that are needed to still extend the integration voltage of the integrators from rail-to-rail is two. In general the saving is well above 25% and depends on the supply voltage and the hysteresis width of the Schmitt trigger circuit.

Commonly used Schmitt trigger circuits do consume a large amount of current from the power supply [Dokic 1984, Wang 1991, Bundalo & Dokic 1989]. By using the very low power Schmitt trigger circuit discussed in Section 4.2, the overall power can be reduced dramatically as the maximum switching current of this Schmitt trigger circuit is less than 1 μA at 5 Volt supply.

D.4 Experimental Results of Extended Mode Schmitt-Oscillator

The measurements presented in the following subsections were obtained from chips fabricated using a 2 μm double poly, double metal n-well process through MOSIS.

D.4.1 Schmitt-Oscillator Measurements

Schmitt-oscillator that use the low power Schmitt trigger circuits discussed in Section 4.2 is designed and implemented in the previously mentioned fabrication process. The schematic diagram of this oscillator is shown in Figure D.3. The measurements of this oscillator are shown in Figure D.5. The oscilloscope photograph shows the output waveform and the voltage drop across a 10 kΩ resistor connected between the supply voltage source and the chip global supply terminal. The oscillation frequency of this oscillator as function of the supply voltage was also measured as shown in Figure D.6. The bias circuit for biasing this oscillator is shown in Figure D.4.

D.4.2 Extended Mode Schmitt Oscillator Measurements

To demonstrate the principle of operation of the EMSO discussed in Section D.3 an EMSO that uses 5 integrators was designed and implemented. The load capacitance for every integrator was chosen to be 0.8 pF, resulting in a total capacitance of 4 pF. The circuit diagram of the fabricated oscillator is shown in Figure D.7. The size of the fabricated oscillator is 0.048 mm^2 excluding the reference bias circuit. The reference current circuit used in biasing this oscillator is the reference bias circuit that is shown in Figure D.4.

A special start-up mechanism was incorporated in the oscillator to guarantee the oscillator start-up and to synchronise the initial conditions across all the capacitors. This start-up circuit is simply an nMOS transistor across every capacitor with the gates of these nMOS transistors tied together and controlled externally. For a fully integrated oscillator, a monostable multivibrator can be used to generate a high pulse for a small period of time to initialise the voltage across the capacitor. This approach was not adopted in the current implementation as the interest is in testing the principle of operation and the functionality of the oscillator. The bias current of 3.65 nA at 3 Volt supply was measured using a Keithley 236 source-measure unit.

The measured output waveforms at 3 Volt supply are shown in Figure D.8. The upper part of the photo shows the voltage drop across a 10 kΩ resistor that is connected between

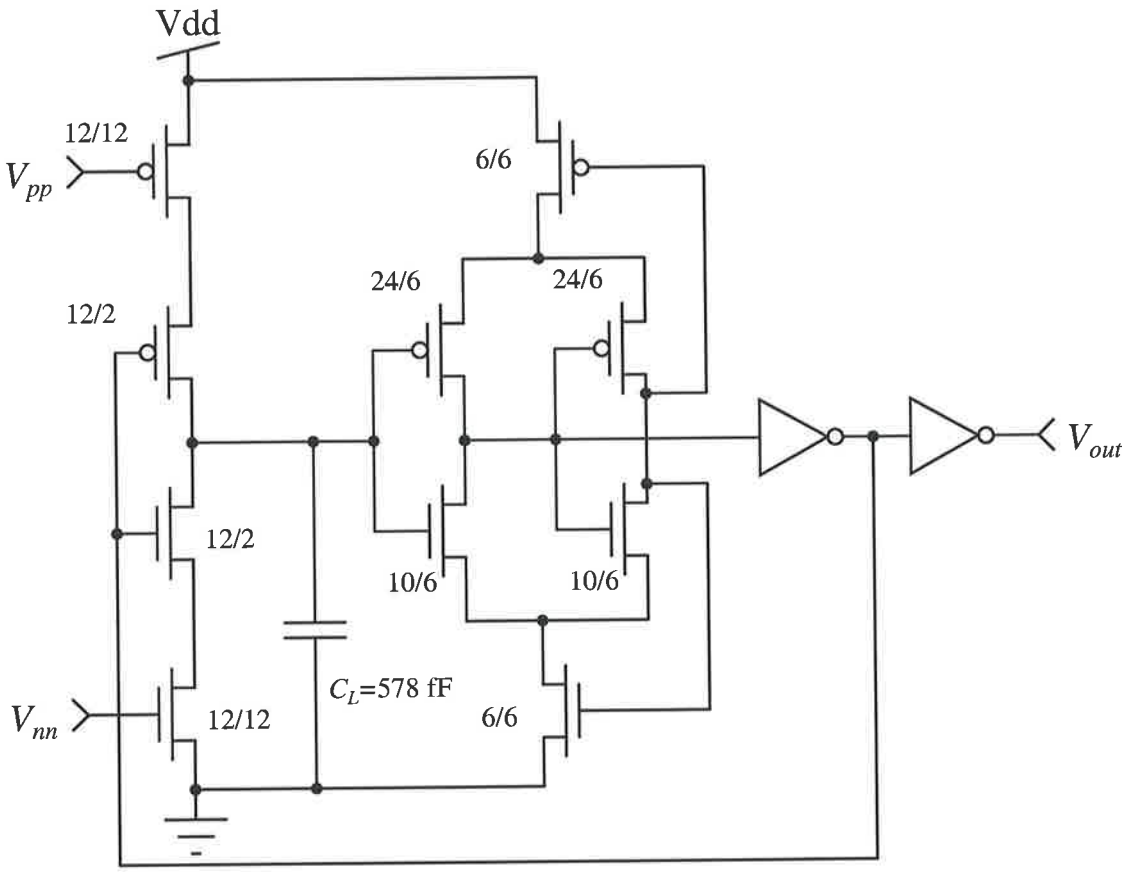

Figure D.3. Circuit diagram of a conventional Schmitt-Oscillator. This circuit uses the low power Schmitt trigger discussed in Section 4.2.3.

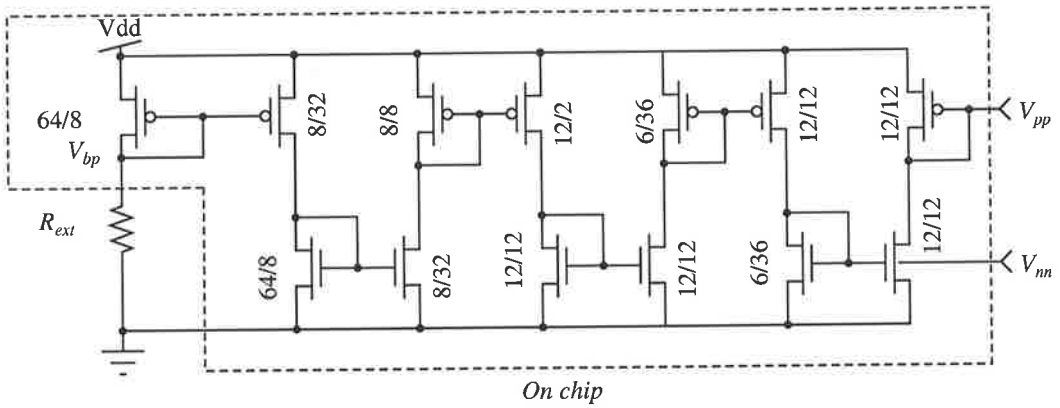

Figure D.4. Circuit diagram of the bias circuit used in biasing the different types of oscillators. This bias circuit is composed of a multistage current scalling current mirror to generate the required bias current for the fabricated oscillators. For this circuit it was decided to use an external bias resistor to generate the reference current.

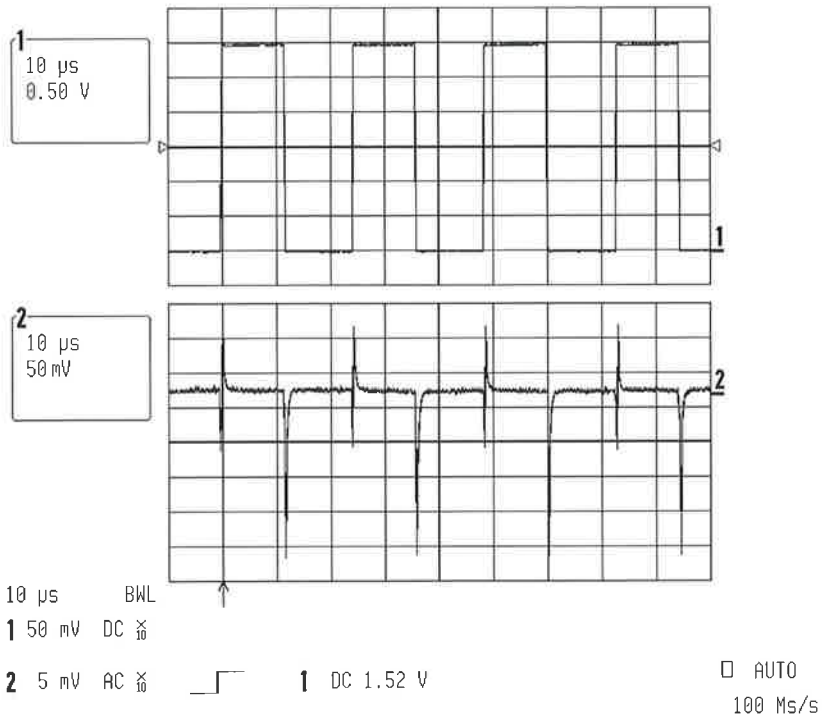

Figure D.5. An oscilloscope photograph of the measured output of the conventional Schmitt-Oscillator (Screen dump from the LeCroy 9360 Oscilloscope). The upper photograph shows the output voltage waveform of the oscillator. The measured oscillation frequency as function of the supply voltage is reported in Figure D.6. The lower graph shows the voltage drop across a 10 kΩ resistor connected between power supply source and the chip global supply voltage.

the voltage source and the chip global supply voltage, while the lower waveform shows the output voltage of the oscillator. The voltage drop across the resistor shows five glitches, these glitches corresponding to the current drawn by the integrators in the oscillator. Also Figure D.8 shows that the total current is modulated by the oscillator output. This is specific to the current implementation and needs to be investigated. The average current drawn from the power supply at 3 Volt supply can be calculated as (18.2 mV/2)/10 kΩ, resulting in 960 nA. Furthermore, the measured oscillation frequency as a function of the supply voltage across four chips is shown in Figure D.9. As can be seen from this figure, the oscillation frequency is inversely proportional to the supply voltage. This inverse relation is due to the following factors. Firstly, it is due to the new oscillator structure, resulting in an oscillation frequency that is function of the supply voltage (as can be seen from the analytical expression for the oscillation frequency given in Equation D.5). Secondly, it is

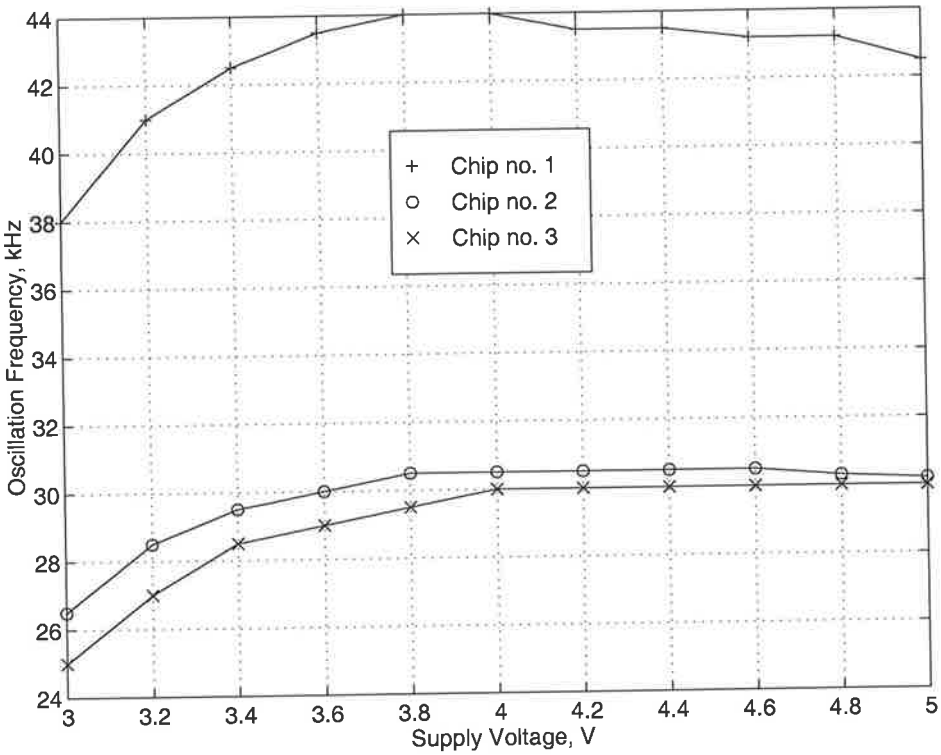

Figure D.6. The measured frequency variation of the conventional Schmitt-Oscillator as function of the supply voltage. These measurements show that the oscillation frequency of the conventional Schmitt-oscillator is dependent on the supply voltage up to 3.8 V and saturates after that voltage. This is due to the fact that bias current will increase with the increase in the supply volage hence resulting an increase in the oscillator frequency, this increase will be cancelled by the increase in the Schmitt trigger hystresis width.

due to the increase in the hysteresis width of the Schmitt trigger circuit as function of the supply voltage. Thirdly, as the supply voltage increase the bias current generated by the reference bias generator increases. Hence increasing the oscillation frequency. The resultant of these effects explains the decrease in the oscillation frequency as function of the supply voltage measured in Figure D.8.

D.5 Summary

In this work the design parameters for the integrator type oscillator and the trade-off between these parameters were identified. In the design of this type of oscillator, it was found that the main current 'hungry' component is the Schmitt trigger circuit and the

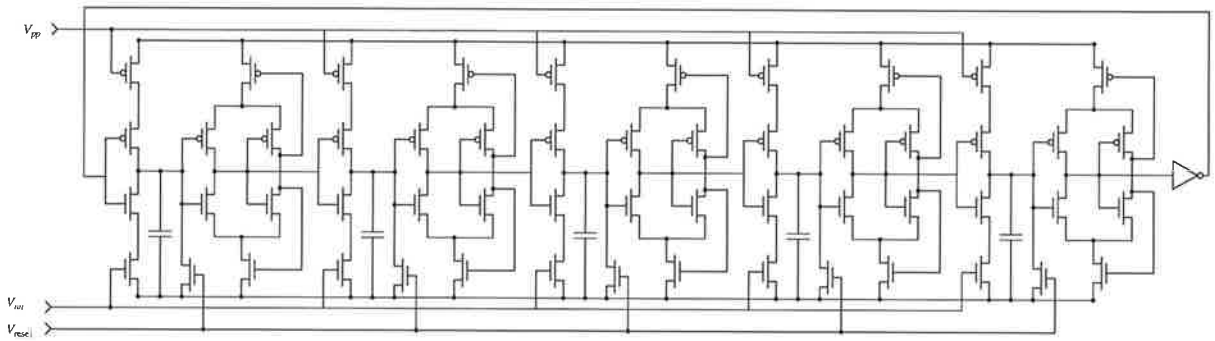

Figure D.7. The circuit connectivity diagram of an EMSO that uses 5 integrators. This circuits illustrates the connectivity of a 5 stage EMSO. In this circuit a reset is need to initials the oscillator internal nodes. This is achieved using terminal V_{reset}.

key element to low power oscillators is the use of a low power Schmitt trigger circuit. The presented analysis and experimental work show that the use of the low power Schmitt trigger circuit dramatically reduced the overall power consumption of the oscillator, as the maximum switching current of the Schmitt trigger circuit is less than 1 μA at 5 Volt supply.

In this chapter, a new methodology to the design of a new variant of the integrator oscillator by using a number of integrators was discussed. The methodology is based on extending the integration voltage to be from rail-to-rail instead of restricting it to the hysteresis width of the Schmitt trigger circuit. Based on the presented analysis, it was found that the optimum number of the integrators is two. The advantage of using such methodology in the design of integrator oscillator is the reduction of the needed capacitor area to achieve the same oscillation frequency in the traditional integrator oscillator. By using the low power Schmitt trigger circuit in the design of the new variant of the integrator oscillator, the oscillator has very low power characteristics that are most favoured in portable applications. In addition to the output waveform of the oscillator, the truncated triangular waveforms at some of the oscillator internal nodes can be of interest in some applications

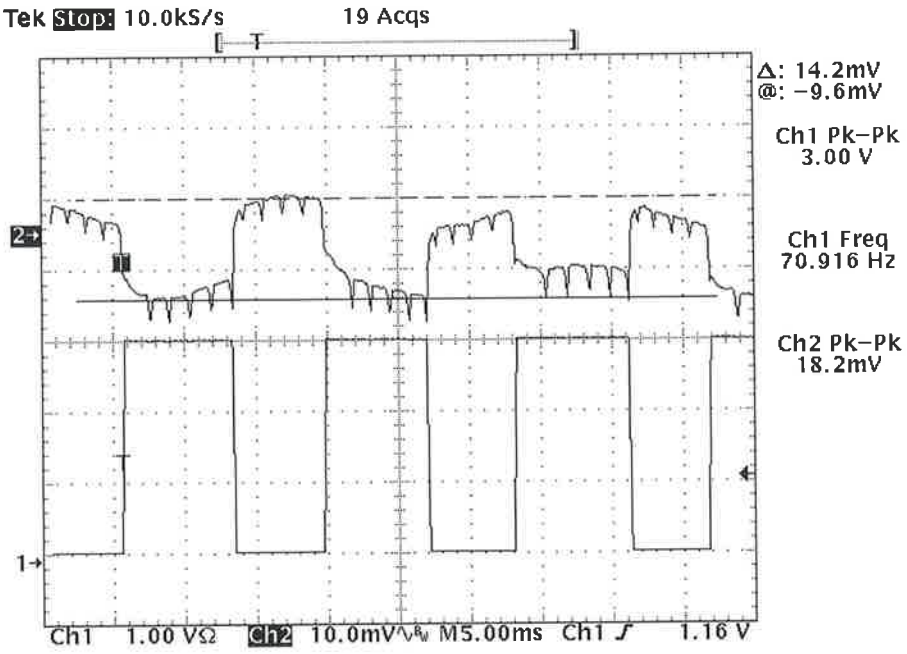

Figure D.8. The measured oscillation frequency of the EMSO which uses five integrators at 3 Volt supply voltage. The upper panel shows the voltage drop across a 10 kΩ resistor connected between the voltage source terminal and the global chip supply voltage. The lower wavefrom shows the output voltage of the oscillator (Screen dump from the Textronix TDS 544A Oscilloscope).

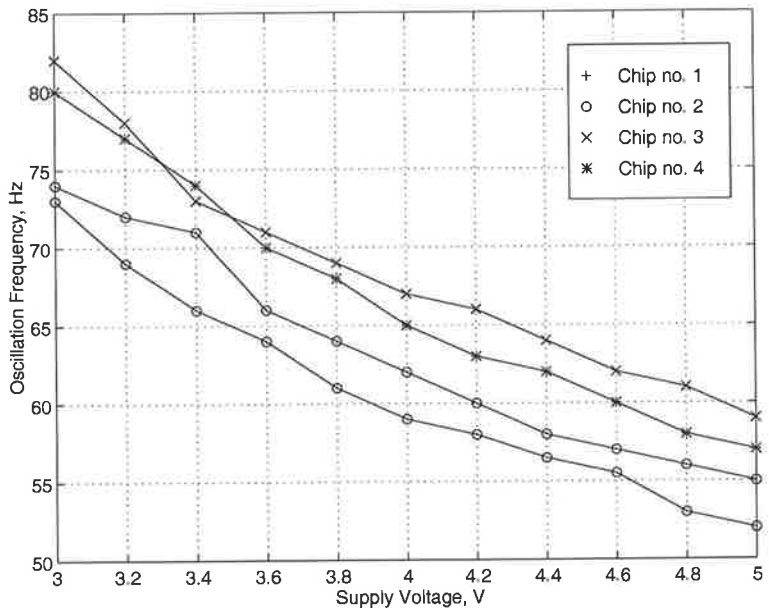

Figure D.9. The measured oscillation frequency of the EMSO as function of the supply voltage. These measurements show negative dependence of the oscillation frequency of the EMSO as function of the supply voltage as predicted by Equation D.6.

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Appendix E

Detailed Derivation of Equation 3.3

This appendix provides a detailed analysis of the digitally trimmed differential amplifier that uses the weighted-voltage technique shown in Figure E.1.

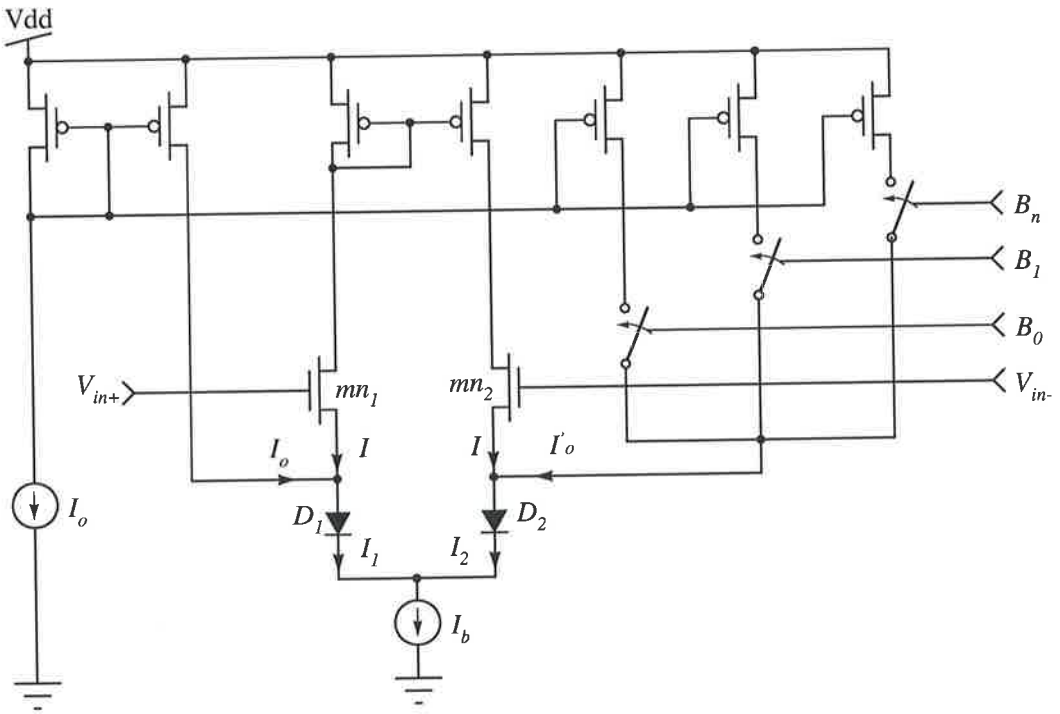

Figure E.1. Digitally trimmed differential amplifier analysis. This amplifier uses the weighted-voltage technique with diodes introduced at the source of the ideally symmetrical transistors mn_1 and mn_2.

The currents through diodes D_1 and D_2 can be written as

$$I_1 = I_o + I \qquad \text{and} \qquad I_2 = I_o^{'} + I.$$

Using the above equation, I_1 and I_2 can be rewritten in terms of the amplifier bias current, I_b, as

$$I_1 = \frac{I_o + I_b - I_o^{'}}{2} \qquad \text{and} \qquad I_2 = \frac{I_o^{'} + I_b - I_o}{2}.$$

The voltage drop across diodes D_1 and D_2 in terms of I_1 and I_2 can be written as

$$V_{D_1} = \eta U_t \ln\left(\frac{I_o + I_b - I_o^{'}}{2I_s}\right) \qquad \text{and} \qquad V_{D_2} = \eta U_t \ln\left(\frac{I_o^{'} + I_b - I_o}{2I_s}\right),$$

where I_s is the reverse saturation current of the pn diode, U_t is the thermal voltage, η is the emission factor. The voltage difference ΔV between the anodes of diodes D_1 and D_2 can be written as

$$\Delta V = V_{D_1} - V_{D_2} = \eta U_t \ln\left(\frac{I_b + I_o - I_o^{'}}{I_b + I_o^{'} - I_o}\right). \tag{E.1}$$

The current $I_o^{'}$ can be written in terms of the switched currents and I_o as:

$$I_o^{'} = \sum_{i=0}^{N} \frac{B_i I_o}{2^i}.$$

Substituting the above definition of $I_o^{'}$ in Equation E.1 yields:

$$\Delta V = \eta U_t \ln\left(\frac{\frac{I_b}{I_o} + (1 - \sum_{i=0}^{N} \frac{W_i}{2^i})}{\frac{I_b}{I_o} - (1 - \sum_{i=0}^{N} \frac{W_i}{2^i})}\right).$$

Appendix F

Measurement Data of the Trimmer Arms

The following tables represent the raw data obtained from measuring the digitally trimmed arms for the offset voltage cancellation technique shown in Figure 3.12. These data are used in the generation of Figures 3.17 and 3.18.

Table F.1. Measurement results of the fabricated trimmer arms shown in Figure 3.12. These measurements were conducted at 3 Volt supply.

State	$S_4 \cdots S_0$	chip 4		chip 3		chip 2		chip 1	
		V_l	V_r	V_l	V_r	V_l	V_r	V_l	V_r
1	0 0 0 0 0	0.8848	3.0000	0.8786	3.0000	0.8878	3.0000	0.8986	3.0000
2	0 0 0 0 1	0.8848	1.0142	0.8786	1.0148	0.8878	1.0112	0.8986	1.0420
3	0 0 0 1 0	0.8848	0.9712	0.8786	0.9679	0.8878	0.9833	0.8986	0.9934
4	0 0 0 1 1	0.8848	0.9573	0.8786	0.9546	0.8878	0.9643	0.8986	0.9795
5	0 0 1 0 0	0.8848	0.9348	0.8786	0.9330	0.8878	0.9518	0.8986	0.9536
6	0 0 1 0 1	0.8848	0.9289	0.8786	0.9273	0.8878	0.9422	0.8986	0.9482
7	0 0 1 1 0	0.8848	0.9210	0.8786	0.9184	0.8878	0.9363	0.8986	0.9398
8	0 0 1 1 1	0.8848	0.9169	0.8786	0.9144	0.8878	0.9298	0.8986	0.9361
9	0 1 0 0 0	0.8848	0.9046	0.8786	0.9054	0.8878	0.9161	0.8986	0.9223
10	0 1 0 0 1	0.8848	0.9020	0.8786	0.9026	0.8878	0.9121	0.8986	0.9200
11	0 1 0 1 0	0.8848	0.8978	0.8786	0.8977	0.8878	0.9094	0.8986	0.9159
12	0 1 0 1 1	0.8848	0.8957	0.8786	0.8955	0.8878	0.9061	0.8986	0.9139
13	0 1 1 0 0	0.8848	0.8899	0.8786	0.8896	0.8878	0.9031	0.8986	0.9075
14	0 1 1 0 1	0.8848	0.8882	0.8786	0.8879	0.8878	0.9002	0.8986	0.9059
15	0 1 1 1 0	0.8848	0.8853	0.8786	0.8845	0.8878	0.8983	0.8986	0.9030
16	0 1 1 1 1	0.8848	0.8838	0.8786	0.8830	0.8878	0.8959	0.8986	0.9017
17	1 0 0 0 0	0.8848	0.8758	0.8786	0.8780	0.8878	0.8907	0.8986	0.8968
18	1 0 0 0 1	0.8848	0.8747	0.8786	0.8767	0.8878	0.8887	0.8986	0.8957
19	1 0 0 1 0	0.8848	0.8726	0.8786	0.8741	0.8878	0.8873	0.8986	0.8937
20	1 0 0 1 1	0.8848	0.8716	0.8786	0.8730	0.8878	0.8854	0.8986	0.8927
21	1 0 1 0 0	0.8848	0.8684	0.8786	0.8696	0.8878	0.8836	0.8986	0.8888
22	1 0 1 0 1	0.8848	0.8675	0.8786	0.8686	0.8878	0.8819	0.8986	0.8880
23	1 0 1 1 0	0.8848	0.8658	0.8786	0.8666	0.8878	0.8808	0.8986	0.8862
24	1 0 1 1 1	0.8848	0.8650	0.8786	0.8657	0.8878	0.8793	0.8986	0.8854
25	1 1 0 0 0	0.8848	0.8612	0.8786	0.8628	0.8878	0.8750	0.8986	0.8810
26	1 1 0 0 1	0.8848	0.8605	0.8786	0.8620	0.8878	0.8737	0.8986	0.8803
27	1 1 0 1 0	0.8848	0.8591	0.8786	0.8602	0.8878	0.8728	0.8986	0.8789
28	1 1 0 1 1	0.8848	0.8585	0.8786	0.8596	0.8878	0.8716	0.8986	0.8783
29	1 1 1 0 0	0.8848	0.8562	0.8786	0.8570	0.8878	0.8703	0.8986	0.8756
30	1 1 1 0 1	0.8848	0.8556	0.8786	0.8564	0.8878	0.8692	0.8986	0.8750
31	1 1 1 1 0	0.8848	0.8543	0.8786	0.8549	0.8878	0.8683	0.8986	0.8738
32	1 1 1 1 1	0.8848	0.8538	0.8786	0.8543	0.8878	0.8673	0.8986	0.8732

Table F.2. Measurement results of the fabricated trimmer arms shown in Figure 3.12. These measurements were conducted at 5 Volt supply.

State	$S_4 \cdots S_0$	chip 4		chip 3		chip 2		chip 1	
		V_l	V_r	V_l	V_r	V_l	V_r	V_l	V_r
1	0 0 0 0 0	0.8903	5	0.884	5	0.8939	5	0.9002	5
2	0 0 0 0 1	0.8903	1.0198	0.884	1.0216	0.8939	1.0187	0.9002	1.0431
3	0 0 0 1 0	0.8903	0.976	0.884	0.9739	0.8939	0.99	0.9002	0.9946
4	0 0 0 1 1	0.8903	0.9622	0.884	0.9678	0.8939	0.9712	0.9002	0.9811
5	0 0 1 0 0	0.8903	0.9393	0.884	0.9389	0.8939	0.9584	0.9002	0.955
6	0 0 1 0 1	0.8903	0.9335	0.884	0.9333	0.8939	0.949	0.9002	0.9499
7	0 0 1 1 0	0.8903	0.9255	0.884	0.9244	0.8939	0.943	0.9002	0.9415
8	0 0 1 1 1	0.8903	0.9216	0.884	0.9207	0.8939	0.9366	0.9002	0.938
9	0 1 0 0 0	0.8903	0.909	0.884	0.9112	0.8939	0.9226	0.9002	0.9239
10	0 1 0 0 1	0.8903	0.9065	0.884	0.9085	0.8939	0.9188	0.9002	0.9218
11	0 1 0 1 0	0.8903	0.9023	0.884	0.9037	0.8939	0.9161	0.9002	0.9177
12	0 1 0 1 1	0.8903	0.9003	0.884	0.9016	0.8939	0.9129	0.9002	0.9159
13	0 1 1 0 0	0.8903	0.8944	0.884	0.8956	0.8939	0.9097	0.9002	0.9093
14	0 1 1 0 1	0.8903	0.8929	0.884	0.894	0.8939	0.907	0.9002	0.9079
15	0 1 1 1 0	0.8903	0.89	0.884	0.8906	0.8939	0.9051	0.9002	0.905
16	0 1 1 1 1	0.8903	0.8887	0.884	0.8893	0.8939	0.9028	0.9002	0.9039
17	1 0 0 0 0	0.8903	0.8802	0.884	0.8839	0.8939	0.8973	0.9002	0.8986
18	1 0 0 0 1	0.8903	0.8793	0.884	0.8828	0.8939	0.8954	0.9002	0.8977
19	1 0 0 1 0	0.8903	0.8772	0.884	0.8802	0.8939	0.894	0.9002	0.8956
20	1 0 0 1 1	0.8903	0.8764	0.884	0.8792	0.8939	0.8924	0.9002	0.8946
21	1 0 1 0 0	0.8903	0.873	0.884	0.8757	0.8939	0.8889	0.9002	0.8907
22	1 0 1 0 1	0.8903	0.8723	0.884	0.8749	0.8939	0.8877	0.9002	0.8899
23	1 0 1 1 0	0.8903	0.8706	0.884	0.8728	0.8939	0.8863	0.9002	0.8882
24	1 0 1 1 1	0.8903	0.87	0.884	0.8721	0.8939	0.8864	0.9002	0.8875
25	1 1 0 0 0	0.8903	0.8661	0.884	0.8689	0.8939	0.8818	0.9002	0.8829
26	1 1 0 0 1	0.8903	0.8655	0.884	0.8683	0.8939	0.8807	0.9002	0.8825
27	1 1 0 1 0	0.8903	0.8641	0.884	0.8666	0.8939	0.8798	0.9002	0.881
28	1 1 0 1 1	0.8903	0.8635	0.884	0.866	0.8939	0.8787	0.9002	0.8805
29	1 1 1 0 0	0.8903	0.8612	0.884	0.8634	0.8939	0.8773	0.9002	0.8776
30	1 1 1 0 1	0.8903	0.8607	0.884	0.8629	0.8939	0.8763	0.9002	0.8772
31	1 1 1 1 0	0.8903	0.8596	0.884	0.8614	0.8939	0.8754	0.9002	0.8759
32	1 1 1 1 1	0.8903	0.8592	0.884	0.861	0.8939	0.8746	0.9002	0.8756

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