Design Techniques for Low Power Mixed Analog-Digital Circuits with Application to Smart Wireless Systems

by

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Abstract

This dissertation presents and discusses new design techniques for mixed analog-digital circuits with emphases on low power and small area for standard low-cost CMOS VLSI technology. The application domain of the devised techniques is radio frequency identification (RFID) systems, however the presented techniques are applicable to wide range of mixed mode analog-digital applications. Hence the techniques herein apply to a range of smart wireless or mobile systems. The integration of both analog and digital circuits on a single substrate has many benefits such as reducing the system power, increasing the system reliability, reducing the system size and providing high inter-system communications speed – hence, a cost effective system implementation with increased performance. On the other hand, some difficulties arise from the fact that standard low-cost CMOS technologies are *tuned* toward maximising digital circuit performance and increasing transistor density per unit area. Usually these technologies have a wide spread in transistor parameters that require new design techniques that provide circuit characteristics based on relative transistor parameters rather than on the absolute value of these parameters.

This research has identified new design techniques for mostly analog and some digital circuits for implementation in standard CMOS technologies with design parameters dependent on the relative values of process parameters, resulting in technology independent circuit design techniques. The techniques presented and discussed in this dissertation are (*i*) applied to the design of low-voltage and low-power controlled gain amplifiers, (*ii*) digital trimming techniques for operational amplifiers, (*iii*) low-power and low-voltage Schmitt trigger circuits, (*iv*) very low frequency to medium frequency low power oscillators, (*v*) low power Gray code counters, (*vi*) analog circuits utilising the neuron MOS transistor, (*vii*) high value floating resistors, and (*viii*) low power application specific integrated circuits (ASICs) that are particularly needed in radio frequency identification systems. The new techniques are analysed, simulated and verified experimentally via five chips fabricated through the MOSIS service.