Modeling, Control and Stability Analysis of VSC-HVDC Links Embedded in a Weak Multi-Machine AC System

by

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Dedicated to my family, my husband, Xike, and my beloved Yaoyi for their constant support and unconditional love.

I love you all dearly.
Abstract

The primary aim of this thesis is to investigate the small-signal dynamic performance of high voltage direct current (HVDC) transmission links based on voltage source converter (VSC) technology operating in parallel with the existing longitudinal Australian power system. This thesis presents the principle design methodology to achieve robust controllers for VSCs including inner current controller, outer power and voltage controllers as well as the supplementary damping controllers for enhancing the small-disturbance rotor-angle stability of a weak multi-machine power system with embedded VSC-HVDC links.

Three types of linear current controller schemes (proportional-integral, proportional-resonant and Dead-Beat schemes) are investigated and discussed in detail to identify the most suitable control method. Due to its wider bandwidth and superior performance under unbalanced operating conditions, the Dead Beat current controller is set as the inner current controller that has not been analysed in detail in the literature.

A new methodology for the selection and optimization of the parameters of the proportional-integral compensators in the various control loops of a VSC-HVDC transmission system using a decoupled control strategy is also proposed in this thesis. It was found that the new methodology is effective in a relatively strong system. However, since the method did not take various operating conditions and system disturbances into account, it will not be effective in a relatively weak system. The analysis shows that the
design of robust outer loop controllers is challenging due to the limited bandwidth of the
inner current controller in a weak AC system. Therefore, the second primary objective of
the project was to develop a simple fixed parameter controller, which can perform well
over a wide range of operating points within the active/reactive power (PQ) capability
chart of the VSCs. To achieve this second objective, various grid conditions including
various Short Circuit Ratios (SCRs), different X/R ratios and PQ capabilities of the VSC
system were studied.

To support the primary objectives, a detailed higher order small-signal model of the
DB controlled VSC is developed and systematically verified. As an original contribution,
the study developed a new methodology to linearize the modulator/demodulator blocks
which are used to develop the small signal models for several key components such as the
sampling block, the delay block and the DB inner current controller.

The initial values of the PI/PID compensator parameters are obtained by applying the
classical frequency response design methods to a set of detailed linear models of the open
loop transfer functions of the VSC-HVDC control system. It was concluded that an
iterative process may be required after examining the co-operation performance of these
controllers designed.

In the final chapter of this thesis, the small-signal rotor-angle stability of a model of
the Australian power system with embedded VSC based HVDC links was examined. For
the analytical purposes of this thesis a simplified model of the Australian power system is
used to connect the high capacity, but as yet undeveloped, geothermal resource in the
region of Innamincka in northern South Australia via a 1,100 km HVDC link to Armidale
in northern New South Wales. It is observed that the introduction of the new source of
geothermal power generation has an adverse impact on the damping performance of the
system. Therefore, two forms of stabilization are examined: (i) generator power system
stabilisers (PSS) fitted to the synchronous machines which are used to convert geothermal
energy to electrical power; and (ii) power oscillation damping controllers (PODs) fitted to
the VSC-HVDC link. In the case of the PODs two types of stabilizing input signals are
considered: (i) local signals such as power flow in adjacent AC lines and (ii) wide-area
signals such as bus voltage angles at key nodes in the various regions of the system. It was
concluded that the small-signal rotor-angle stability of the interconnected AC/DC system
has been greatly enhanced by employing the designed damping controllers.
Statement of Originality

This work contains no material which has been accepted for the award of any other degree or diploma in any university or other tertiary institution and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text.

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____________________________  ______________________________
Signed                                                                          Date

08/12/13
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# Table of Contents

Abstract......................................................................................................................................................... i
Statement of Originality................................................................................................................................. iii
Acknowledgements........................................................................................................................................ iv
Table of Contents........................................................................................................................................... v
List of Figures................................................................................................................................................ viii
List of Tables .................................................................................................................................................. x
List of Publications ......................................................................................................................................... xv
Symbols ......................................................................................................................................................... xix
Acronyms......................................................................................................................................................... xx

Chapter 1: Introduction ................................................................................................................................. 1
  1.1 Background ....................................................................................................................................... 1
  1.2 VSC-HVDC System ......................................................................................................................... 2
    1.2.1 VSC Topology ......................................................................................................................... 2
    1.2.2 Operation Principle of VSC ................................................................................................. 3
    1.2.3 Characteristics and Applications of VSC-HVDC ............................................................. 4
  1.3 Literature Review ............................................................................................................................. 6
    1.3.1 Control Strategies of VSC-HVDC ........................................................................................ 6
    1.3.2 Small Signal Modeling .......................................................................................................... 11
    1.3.3 Grid Interconnection ............................................................................................................ 13
  1.4 Thesis Overview ............................................................................................................................. 15
    1.4.1 Research Gap ...................................................................................................................... 15
### TABLE OF CONTENTS

1.4.2 Thesis Outline ................................................................................................................................. 16

Chapter 2: VSC-HVDC Control Structures ............................................................................................... 18

2.1 Introduction ........................................................................................................................................ 18

2.2 Background Study for System Modeling ......................................................................................... 20

2.2.1 Frame Transformation .................................................................................................................. 20

2.2.2 Transient Mathematical System Model .......................................................................................... 22

2.3 Description of Controllers and Determination of Controller Parameters ....................................... 24

2.3.1 Proportional Integral Control ........................................................................................................ 24

2.3.2 Proportional Resonant Control ....................................................................................................... 39

2.3.3 Dead Beat Control .......................................................................................................................... 42

2.4 Conclusion .......................................................................................................................................... 56

Chapter 3: Analytical Modeling of DB Controlled VSC ........................................................................... 58

3.1 Diagram of DB model ......................................................................................................................... 59

3.2 Characterizing the Components of VSC Small Signal Model ......................................................... 60

3.2.1 Phase Locked Loop ...................................................................................................................... 61

3.2.2 Frame Transformation .................................................................................................................... 72

3.2.3 Grid Voltage Signal Filter ............................................................................................................. 76

3.2.4 Reference Current Phase Compensation and Voltage Prediction Block .................................... 77

3.2.5 Discrete DB Current Feedback Control Block and Current Input Generation .......................... 78

3.2.6 Characterizing ZOH Block, Sampling Block and Inner Current Control .................................... 79

3.2.7 Reference Voltage Generation of the Converter ........................................................................... 102

3.2.8 Voltage Source Converter ............................................................................................................ 103

3.2.9 Grid Model ...................................................................................................................................... 107

3.3 Comparison of the Small Signal Linear Model and PSCAD Simulation ......................................... 109

3.4 Extension of the DB Controlled VSC Together with DC Link ....................................................... 112

3.4.1 Model of DC Link .......................................................................................................................... 112

3.4.2 Interconnection of Subsystems ..................................................................................................... 115

3.4.3 Model of the DB Controlled VSC Including a DC Link ............................................................... 117

3.5 Conclusion .......................................................................................................................................... 118

Chapter 4: Controller Design for VSC-HVDC Connected to a Weak AC Grid ....................................... 120

4.1 Introduction .......................................................................................................................................... 120

4.2 Issues for VSC-HVDC Embedded in a Weak AC Grid .................................................................. 121

4.2.1 Circuit Analysis ............................................................................................................................... 122

4.2.2 System Stability Analysis based on A Simplified Model .............................................................. 123
## TABLE OF CONTENTS

4.3 Controller Design Methodology................................................................. 124
  4.3.1 Scenarios Considered in Controllers Design.............................. 125
  4.3.2 Calculation of the Steady State Operating Points .................. 127
  4.3.3 Controller Design for Rectifier .................................................. 129
  4.3.4 Controller Design for Inverter................................................... 148
  4.3.5 Cross-Coupling Effects Examination........................................... 154

4.4 Discussions and Conclusions ............................................................. 163

Chapter 5: Stability of VSC-HVDC Links Embedded with the Weak Australian Grid ............. 165

  5.1 Introduction.......................................................................................... 165
  5.2 Preparation Tasks for Interconnection ............................................. 167
    5.2.1 Admittance Matrix Representation of the Integrated Grid and Filter .... 168
    5.2.2 Scaling the Existing System...................................................... 173
    5.2.3 DC Link Parameter Sensitivity ................................................. 178
  5.3 Integrating with the Simplified Australian Grid .................................. 179
    5.3.1 Accuracy Evaluation of Designing VSC Controllers Based on Simplified Grid Admittance Model.................................................. 180
    5.3.2 Stability Analysis ........................................................................ 186
    5.3.3 Damping Controllers Design...................................................... 194
  5.4 Conclusion and Discussion ................................................................. 210

Chapter 6: Conclusion .................................................................................... 212

  6.1 Summary .............................................................................................. 212
  6.2 Original Contributions and associated Key Results ............................ 214
    6.2.1 Original Contributions .................................................................. 214
    6.2.2 Associated Key Results of the Thesis ......................................... 214
  6.3 Suggestions for Further Research ........................................................... 217

Appendix A: VSC-HVDC System Parameters ................................................. 219

Appendix B: Method (II) for Elimination of Modulator/De-modulator System .......... 221

Appendix C: Method (I) for Elimination of Modulator/Demodulator System .......... 225

Appendix D: Lead-Lag Block........................................................................ 231

Appendix E: Regional Boundaries for the National Electricity Market & Committed Developments................................................................. 233

Appendix F: Performance Evaluation of all the Power and Voltage Controllers with a New set of DC Link Parameters.................................................. 235

Appendix G: VSC-HVDC System (II) Parameters ........................................... 243

Reference .................................................................................................... 245
List of Figures

Figure 1-1 A typical VSC topology connected to the AC grid (a) simplified diagram, (b) the details of the circuit including three phase two-level VSC using IGBTs.........................3

Figure 2-1 Current control classifications .................................................................19

Figure 2-2 Representation of rotating vector in converter including stationary αβ reference frame and abc natural reference frame. .........................................................21

Figure 2-3 Representation of rotating vector in dq reference frame and αβ reference frame ..............................................................................................................................................22

Figure 2-4 Single line diagram representation of VSC-HVDC......................................22

Figure 2-5 (a) The diagram of the inner and outer controllers; (b) Inner current control loop. ............................................................................................................................................25

Figure 2-6 Flow chart of the process for determining the PI compensator parameters for VSC-HVDC control system ........................................................................................................27

Figure 2-7 Detailed inner current control loop in pu system...........................................28

Figure 2-8 Block diagram of DC voltage control scheme in pu system.........................29

Figure 2-9 (a) Block diagram of active power control scheme in pu system; (b) block diagram of reactive power control scheme in pu system.........................................................30

Figure 2-10 VSC-HVDC system diagram........................................................................32
LIST OF FIGURES

Figure 2-11 Open-loop Bode plots of the current controller transfer function (i) without PI control (blue solid line); (ii) with PI compensation using initial parameters (green dashed line). ........................................................................................................................................33

Figure 2-12 Step responses of current controller transfer function (i) without PI control (blue solid line); (ii) with PI compensation using initial parameters (green dashed line) ........................................................................................................................................34

Figure 2-13 Open-loop Bode plots of the outer DC controller transfer-function (i) without PI compensation (solid blue line); and (ii) with PI compensation using the initial parameters (dashed green line). ........................................................................................................................................35

Figure 2-14 Step responses of the outer DC controller transfer-function (i) without PI compensation (solid blue line) and (ii) with PI compensation using the initial parameters (dashed green line). ........................................................................................................................................35

Figure 2-15 Open-loop Bode plots of the outer active/reactive power controller transfer-function (i) without PI compensation (blue solid line) and (ii) with PI compensation using the initial parameters (dashed green line) ........................................................................................................................................36

Figure 2-16 Responses of VSC-HVDC following a reversal of the power order for (i) the initial set of PI compensator parameters (red line); (ii) the parameters obtained with the optimization function (2-34) (blue line) and (iii) the parameters obtained with the refined optimization function (2-35) (cyan line). The reference values of the variables are shown in green line........................................................................................................................................37

Figure 2-17 Structure of the paralleled harmonic compensators ..................................................40
Figure 2-18 Diagram of αβ reference frame mathematical model of VSC system ....41
Figure 2-19 The simplified model of PR current controlled VSC system in αβ reference frame ........................................................................................................................................41

Figure 2-20 The categories of DB current controllers .................................................................42
Figure 2-21 Digital DB current controlled VSC system .............................................................43
Figure 2-22 The closed-loop DB current Control ........................................................................44

Figure 2-23 Pole-zero map of the one sample delay system: red cross: one sample delay DB without considering the computation delay time; blue cross: represents one sample delay DB considering the computation delay time; green cross: represents reducing the proportional gain;........................................................................................................................................45

Figure 2-24 One sample delay DB control with Smith Predictor .................................46

ix
Figure 2-25 Internal model control design for DB implementation block ............47
Figure 2-26 The block diagram of solving feedback transfer function DB current control ..............................................................................................................48
Figure 2-27 The structure of the solving feedback transfer function DB current controller ........................................................................................................48
Figure 2-28 Frequency response and step response of various DB current controllers ........................................................................................................49
Figure 2-29 PSCAD step response simulation results of the DB current controller ..54
Figure 3-1 Small signal model of VSC with the discrete DB current controller.....60
Figure 3-2 Structure of phase locked loop ..........................................................62
Figure 3-3 Non-linear model for PLL .................................................................65
Figure 3-4 Block diagram of PLL linearized model .............................................66
Figure 3-5 Frequency response of PLL in the case study ....................................68
Figure 3-6 Linearized model verification, 1% step change in phase .............. 68
Figure 3-7 50% step (180°) change in phase ....................................................69
Figure 3-8 1% step change in frequency ............................................................70
Figure 3-9 PLL responses to 90% magnitude step change of input voltage ..........70
Figure 3-10 PLL output phase angle in comparison with input phase angle when being subject to a sudden 90% magnitude step change of input voltage ............70
Figure 3-11 PLL output frequency in comparison with input frequency when being subject to a sudden 90% magnitude step change of input voltage ..................71
Figure 3-12 PLL output phase angle when being subject to an A-phase to ground fault ..............................................................................................................71
Figure 3-13 PLL output frequency when being subject to an A-phase to ground fault ..............................................................................................................72
Figure 3-14 Relationship between converter reference frame and grid RI reference frame ..........................................................................................................73
Figure 3-15 Controlled voltage source representation with an inductance ........74
Figure 3-16 Test results for grid RI reference frame transformation ..................74
Figure 3-17 The test circuit for small signal mathematical equation ................75
Figure 3-18 Small signal test results for the grid frame transformation .......... 75
Figure 3-19 Current compensation block verification .......................................77
Figure 3-20 Frequency responses of pure one sample delay...........................................80
Figure 3-21 Step responses of pure one sample delay ..................................................81
Figure 3-22 Demonstration of ZOH function .................................................................82
Figure 3-23 A typical sampled data system structure ....................................................83
Figure 3-24 Composition of a rectangular impulse .........................................................83
Figure 3-25 Frequency responses of ZOH block and its approximation .........................84
Figure 3-26 Step responses of ZOH block and its approximation ....................................85
Figure 3-27 Verification of responses to the sinusoid input for ZOH by Matlab ..........86
Figure 3-28 Responses to the sinusoid input for ZOH by PSCAD ..............................86
Figure 3-29 Comparison of the simulation results ..........................................................87
Figure 3-30 Frequency response of inner current controller and its approximations 88
Figure 3-31 Step response of inner DB current controller and its approximation ....89
Figure 3-32 Implementation of the inner DB current controller scheme in continuous

domain and in the z domain .........................................................................................90

Figure 3-33: Comparison of the responses of (i) the discrete DB current controller
and (ii) its first order Padé Approximation to a sinusoidal input signal. .......................91
Figure 3-34 The abc natural reference frame DB current control block ......................91
Figure 3-35 The simplified abc natural reference frame DB current control block ...92
Figure 3-36 The simplified αβ reference frame DB current control block ...............92
Figure 3-37 Simplified dq reference frame DB current control block including the
time-varying terms (modulator/de-modulator) .........................................................92
Figure 3-38 Modulator/de-modulator system ...............................................................93
Figure 3-39 Transfer function representation of the modulator/de-modulator system
transform from αβ reference frame to dq reference frame ........................................96

Figure 3-40 Small signal model for DB current controller in equivalent dq reference
frame ..............................................................................................................................98

Figure 3-41 Compare \( \frac{Y_d}{Y_q} \) outputs from (i) the modulator/de-modulator system; (ii)
the small-signal equivalent transfer function and iii) the small-signal equivalent state space.
(a) \( U_{dSTEP} = 0, U_{qSTEP} = -0.02 \) and (b) \( U_{dSTEP} = -0.02, U_{qSTEP} = 0 \); .........................99

Figure 3-42 Difference between \( \frac{Y_d}{Y_q} \) outputs from (i) the modulator/de-modulator
system versus the small-signal equivalent transfer function; (ii) the modulator/de-
modulator system versus the small-signal equivalent state space. (a) \( U_{d\text{STEP}} = 0, U_{q\text{STEP}} = -0.02 \) and (b) \( U_{d\text{STEP}} = -0.02, U_{q\text{STEP}} = 0 \);

Figure 3-43 Compare \( Y_d/Y_q \) outputs from the (i) modulator/de-modulator system; (ii) the small-signal equivalent transfer function and iii) the small-signal equivalent state space .................................................................99

Figure 3-44 Test circuit for the detailed VSC model ........................................102
Figure 3-45 The equivalent circuit diagram of grid .......................................107
Figure 3-46 Small signal model of the grid..................................................108
Figure 3-47 (a) Grid side current and (b) filter bus voltage responses of i) large signal model ii) small signal model following a input voltage step change order on \( \Delta V_{c_q} = -0.56\text{kV} \) .................................................................109

Figure 3-48 Comparison of the converter output current \( \Delta I_{ed}^C, \Delta I_{eq}^C \) using the (i) large signal model simulating with VSC simplified as a controlled voltage source; (ii) the small-signal model for AC system with different SCRs .................................................................111

Figure 3-49 Comparison of the converter output currents \( \Delta I_{ed}^C, \Delta I_{eq}^C \) from the (i) large signal model using the detailed VSC model, and (ii) the small-signal model for the weak AC system ........................................................................................................112

Figure 3-50 The model DC transmission link ..............................................113
Figure 3-51 Test circuit for DC link test .......................................................114
Figure 3-52 The converter currents behind the DC capacitor from both of the rectifier side and inverter side (circle: Large signal model; rectangular: Small signal model) ......114
Figure 3-53 Demonstration of sub-modular interconnection .......................115
Figure 3-54 The base model for the converter side controller .......................117
Figure 3-55 Comparison of the converter output currents \( \Delta I_{ed}^C, \Delta I_{eq}^C \) using the (i) large-signal model simulated in the detailed VSC model including the DC link, and (ii) the small-signal model for a weak AC system together with the DC link .........................118

Figure 4-1 Single phase equivalent circuit ................................................122
Figure 4-2 Simplified DB current controlled VSC .......................................123
Figure 4-3 Zeros/poles in z-domain for (a) weak system (b) strong system of a DB current controlled VSC system ........................................................................................................124
Figure 4-4 (a) Bode plots and (b) step responses of a DB current controlled VSC system ..................................................................................................................................................124

Figure 4-5 Flow chart of the controller design methodology .............................................125

Figure 4-6 PQ capability chart (a) demonstration chart; (b) defined operating points .................................................................................................................................................................................................126

Figure 4-7 Single-line diagram of AC side converter including a high-pass filter ..129

Figure 4-8 Influence of the DC link model: (a) pole-zero map of I_q(s)/I_qref(s); (b) Bode plots of I_q(s)/I_qref(s) ...............................................................................................................................................................................................129

Figure 4-9 Basic structure for outer power controller design ........................................130

Figure 4-10 (a) In the DB current controlled VSC with P=P_{max} (a) eigenvalue maps with SCR reduced from 7.5 to 0.5 at a step of -1 (i.e. A to G); (b) Bode plots of the TF (blue: SCR=7.5, red: SCR=4.5, cyan: SCR=2). ........................................................................................................................133

Figure 4-11 The time-domain simulation results: PSCAD SCR=7.5 (solid cyan line); Matlab SCR=7.5 (dash-dot blue line); PSCAD SCR=2 (solid black line); Matlab SCR=2(dash-dot red line). ................................................................................................................134

Figure 4-12 Four main low frequency modes for A: rectifier mode with a 90° angle; B: rectifier mode with a 75° angle; C: rectifier mode with a 60° angle; a: inverter mode under 90° angle; b: inverter mode under 75° angle; c: inverter mode under 60° angle; ....135

Figure 4-13 The Bode plots of the DB current controlled VSC. blue: rectifier mode under 90° angle; cyan: Rectifier mode under 75° angle; red: rectifier mode under 60° angle; magenta: inverter mode under 90° angle; black: inverter mode under 75° angle; green: inverter mode under 60° angle; .................................................................................................................135

Figure 4-14 Step responses of DB current controlled VSC for the rectifier (left) and the inverter (right). rectifier mode at angle 90° (blue); rectifier mode at angle 75° (cyan); rectifier mode at angle 60° (red); inverter mode at angle 90° (magenta); inverter mode at angle 75° (black); inverter mode at angle 60° (green); .........................................................................................................................136

Figure 4-15 For DB controlled VSC with SCR=2 (a) the eigenvalue map with P equals to be 1pu (A), 0.5pu (B) and 0pu (C); (b) Bode plots of the TF with different loading conditions. blue: P=1pu, cyan: P=0.5pu, red: P=0pu). ..........................................................................................................................137

Figure 4-16 (a) The eigen-value map and (b) Bode plot of the transfer function for the DB current controlled VSC at SCR=2 and different power factors (Q=Q_{max}, Q=0 and
Q=Q_{min}) under full load condition. (dark blue: lagging power factor, light blue: unity power factor, red: leading power factor). ................................................................. 138

Figure 4-17 The analysis of the transfer functions using Bode plots and at 36 operating conditions in total (a) SCR=2 at 90° (b) SCR=2 at 75°; (c) SCR=7.5 at 90°; (d) SCR=7.5 at 75°; ................................................................. 139

Figure 4-18 Right half-plane zeros for the transfer function of the open loop power controller .............................................................................................................. 141

Figure 4-19 Bode plots of the selected cases for the power controller design ........142

Figure 4-20 The Bode plots with (a) low-pass filter; (b) DB current controlled VSC with a low-pass filter; (c) designed PI compensator; (d) open loop transfer function of P(s)/P_{ref}(s) ........................................................................................................ 143

Figure 4-21 Step responses of P(s)/P_{ref}(s) ................................................................................................. 143

Figure 4-22 Control block for the power controller .......................................................... 144

Figure 4-23 A typical MIMO system, in which the hidden feedback loop is shown in red lines .......................................................................................................................... 144

Figure 4-24 Bode plots of selected cases in the AC voltage controller design ......146

Figure 4-25 The Bode plots of (a) U(f)/I_{dref} (s) of DB current controlled VSC with a low-pass filter; (c) the designed PI compensator and (d) open loop transfer function of U(f)/U_{ref}(s) at the rectifier side ......................................................................................................................... 147

Figure 4-26 Step responses of U(f)/U_{ref}(s) ................................................................................................. 148

Figure 4-27 Control block for AC voltage controller .............................................................................. 148

Figure 4-28 The frequency responses of (a) U_{dc}(s)/I_{qref}_inv(s); (b) U_{dc}(s)/I_{dref}(s); (c) U_{f,inv}(s)/I_{q,ref}_inv(s) and (d) U_{f,inv}(s)/I_{d,ref}_inv(s) being subject to the operating point variation of the rectifier side converter (36 scenarios), but with a constant operating point at the inverter side converter that is P_{max}Q_{0}, SCR=2 and with angle equals to 90°. ............ 149

Figure 4-29 (a) The Bode plots of the selected cases of the DC voltage controller design U_{dc}(s)/I_{qref}_inv(s); (b) designed PID compensator (K_{p,dc}+K_{i,dc}/s+K_{d,dc}·s/(1+T_{Udc}·s)=-0.024-0.088/s+0.0009·s/(1+0.06·s)); (c) frequency responses of open loop transfer functions of U_{dc}(s)/U_{dc,ref} (s) and (d) step responses of the closed-loop U_{dc}(s)/U_{dc,ref}(s). ................................................................................................................................. 151

Figure 4-30 The control block diagram of the DC voltage controller ...................... 151
Figure 4-31 (a) Bode plots of selected cases for inverter end AC voltage controller design $U_{f_{inv}}(s)/I_{dref_{inv}}(s)$; (b) designed filter+PI compensator; (c) frequency responses of open loop transfer functions of $U_{f_{inv}}(s)/U_{f_{inv ref}}(s)$; (d) step responses of closed-loop $U_{f_{inv}}(s)/U_{f_{inv ref}}(s)$.

Figure 4-32 1% step of AC voltage reference at the rectifier end; (a) responses of power at the rectifier end; (b) responses of the filter bus voltage $U_{f_{rec}}$ at the rectifier end; (c) responses of DC voltage $U_{dc_{inv}}$ at the inverter end; (d) responses of the filter bus voltage $U_{f_{inv}}$ at the inverter end.

Figure 4-33 1% step of power reference at the rectifier end; (a) responses of the power at the rectifier end; (b) responses of the filter bus voltage $U_{f_{rec}}$ at the rectifier end; (c) responses of the DC voltage $U_{dc_{inv}}$ at the inverter end; (d) responses of the filter bus voltage $U_{f_{inv}}$ at the inverter end.

Figure 4-34 1% Step of the AC voltage reference at the inverter end; (a) response of the power at the rectifier end; (b) response of filter bus voltage $U_{f_{rec}}$ at the rectifier end; (c) response of the DC voltage $U_{dc_{inv}}$ at the inverter end and (d) response of the filter bus voltage $U_{f_{inv}}$ at the inverter end.

Figure 4-35 1% step of the DC reference voltage at the rectifier side; (a) the responses of power at the rectifier; (b) the responses of the filter bus voltage $U_{f_{rec}}$ at the rectifier; (c) the responses of the DC voltage $U_{dc_{inv}}$ at the inverter end; (d) the responses of the filter bus voltage $U_{f_{inv}}$ at the inverter end.

Figure 4-36 The step responses of $U_{finv_{ref}}$ (a) and $U_{dcinv_{ref}}$ (b) and their induced performances in their cross-coupling loops as the system working at an operating point $P_{max}Q_{max}$, SCR=2 with $\phi=90^\circ$. red: Matlab 1%; cyan: PSCAD 1%; black: PSCAD 2%/2; magenta: PSCAD 4%/4; green: PSCAD 8%/8.

Figure 4-37 The step responses of $U_{dcinv_{ref}}$ (a) and $U_{finv_{ref}}$ (b) and their induced performances in their cross-coupling loops as the system working at an operating point $P_{0}Q_{min}$, SCR=7.5 with $\phi=75^\circ$. red: Matlab 1%; cyan: PSCAD 1%; black: PSCAD 2%/2; magenta: PSCAD 4%/4; green: PSCAD 8%/8.

Figure 5-1 The diagram of the extended Simplified South-East Australian power grid with VSC-HVDC links.

Figure 5-2 Grid model as an admittance.
Figure 5-3 1% DC voltage step responses of the dynamic and grid admittance models (a) for rectifier side; (b) for inverter side. .................................................................170
Figure 5-4 The grid and filter model as an admittance.................................171
Figure 5-5 1% DC voltage step response comparison of the admittance representation of grid model only, and the grid and filter models adopting admittance representation: (a) the rectifier side; (b) the inverter side. .................................................................172
Figure 5-6 System parameter scaling scheme ............................................173
Figure 5-7 Scaling of inner current controllers ............................................174
Figure 5-8 Scaling of PI controller with additional filter ..............................176
Figure 5-9 Scaling of the PID controller ......................................................176
Figure 5-10 Flow chart of the verification methodology of modeling ...............177
Figure 5-11 Eigenvalue map of the original and scaled systems .....................178
Figure 5-12 The comparison of the system eigenvalues between the new updated DC link system and the original system .................................................................179
Figure 5-13 The frequency responses for the rectifier side (a) and for inverter side (b) for the higher order grid impedance models (I to V). .........................................................181
Figure 5-14 The open loop frequency responses, $P_{\text{rec}}/P_{\text{ref}}$ ......................182
Figure 5-15 The step responses test of the power reference at the rectifier side.....183
Figure 5-16 The open loop frequency responses, $U_{f,\text{ref}_{\text{rec}}}/U_{f,\text{rec}}$ ...............183
Figure 5-17 The step response test of the AC voltage reference at the rectifier side .................................................................................................................................184
Figure 5-18 The open loop frequency responses, $U_{\text{dc,ref}_{\text{rec}}}/U_{\text{dc,rec}}$ .........184
Figure 5-19 The step response test of the DC voltage reference at the inverter side .................................................................185
Figure 5-20 The open loop frequency responses, $U_{f,\text{ref}_{\text{inv}}}/U_{f,\text{inv}}$ ...................185
Figure 5-21 The step response of the AC voltage reference at the inverter side.....186
Figure 5-22 Eigenvalue map of the interconnected system............................187
Figure 5-23 Right eigenvector prototype of mode I40 ....................................188
Figure 5-24 Participation factor for mode I40 ..............................................189
Figure 5-25 Right eigenvector prototype of mode I35 ....................................190
Figure 5-26 Participation factor for mode I35 ..............................................190
Figure 5-27 Right eigenvector prototype of mode I25 ....................................191
Figure 5-28 Participation factor for mode I25..................................................... 192
Figure 5-29 Right eigenvector prototype of mode I15............................... 193
Figure 5-30 Participation factor for mode I15............................................. 193
Figure 5-31 Eigenvalue evolution for the PSS damping gain on each generator is increased from zero (no PSS in service) to 30 pu on machine base (750MVA) in 5 pu steps. .................................................................................................................. 194
Figure 5-32 Bode plot for DAMP(s) with \( D_{\text{PSS}} = 20 \text{pu} \) on \( M_{\text{base}} \) 750 MVA, \( T_w = 3 \text{s} \) and \( T_p = 0.05 \text{s} \) .................................................................................................................. 196
Figure 5-33 PVR characteristic and curve fitting for Innamincka generator #1 ....... 197
Figure 5-34 The comparison of the rotor modes of the system with the equivalent damping torque (blue star) and the system fitted with PSS (red dot) under the high loading condition and light loading condition. The damping gain in Innamincka generators are increased from zero (no PSS in service) to 30 pu in 5 pu steps........................................... 198
Figure 5-35 Comparison on the power output of generator #1 from Innamincka under the condition with and without PSS in service by applying a small disturbance 0.01pu on the reference voltage of Innamincka generator #1 ................................................................. 198
Figure 5-36 (a) Damping torque coefficients introduced by the PSS in the Innamincka generator #1 (red curve) compared with the specified damping torque coefficient (blue curve) (b) induced synchronizing torque (De equals to be 20 pu on \( M_{\text{base}} \)) .......................................................................................................................... 199
Figure 5-37 The schematic diagram of the VSC-HVDC damping system .......... 200
Figure 5-38 Frequency response of lead compensator \( Q(s) \) for the local POD ...... 203
Figure 5-39 The eigenvalue map of system fitted with POD, where the letters represent the gains of the POD and KSS is increased from \( 3.642 \times 10^{-3} \) to \( 7.03642 \times 10^{-2} \) with a step size of 0.01. .................................................................................................................. 204
Figure 5-40 The eigenvalue map of system fitted with POD and PSS. Here the letters are the gains of the POD and KSS is increased from \( 3.642 \times 10^{-3} \) to \( 7.03642 \times 10^{-2} \) with a step size of 0.01.................................................................................................................. 205
Figure 5-41 Power output of Innamincka generator #1 following a 0.01 pu step change on the voltage reference of Innamincka generators ........................................ 205
Figure 5-42 The performance evaluation of the VSC controllers with the supplementary controllers in service following a step change of 0.01 pu on power reference of the rectifier side converter. .................................................................206

Figure 5-43 Frequency response of lead compensator Q(s) of the WAPOD ........207

Figure 5-44 The eigenvalue map of system fitted with WAPOD under high loading condition, where the letters represent the gains of the WAPOD, as KSS is increased from 3.642x10^-4 to 0.12 with a step size of 0.02. .................................................................207

Figure 5-45 The eigenvalue map of system fitted with WAPOD under light loading condition, where the letters represent the gains of the WAPOD, while KSS is increased from 3.642x10^-4 to 0.12 with a step size of 0.02.................................................................208

Figure 5-46 Eigenvalue analysis of WAPOD with PSS under high loading condition, where KSS is increased from 3.642x10^-4 to 0.12 with a step size of 0.02.........................209

Figure 5-47 Power outputs of Innamincka generator #1 following a step change of 0.01 pu on voltage reference of Innamincka generators. ........................................209

Figure 5-48 The performance evaluation of the VSC controllers with PSS and WAPOD in service following a step change of 0.01 pu on power reference of the rectifier side converter. .................................................................210
List of Tables

Table 1-1 Categories of SCR.................................................................8
Table 2-1 PI parameters comparison.......................................................38
Table 2-2 Open loop transfer function of DB current controllers...............49
Table 2-3 Sensitivity to plant parameters................................................50
Table 2-4 Simulation parameter ................................................................51
Table 2-5 Summary of specific data obtained from Figure 2-29 .................54
Table 2-6 Mean derivation of simulation results........................................56
Table 3-1 PLL parameters.........................................................................67
Table 3-2 Characteristics of the linearized model......................................69
Table 3-3 Characteristics of the step response corresponding to the pure one sample delay...............................................................................81
Table 3-4 Characteristics of the step response corresponding to ZOH.........85
Table 3-5 Summary of transfer functions for DB current controller, sampling block and delay block ..................................................................................97
Table 3-6 Equivalent dq reference frame transfer function for the lead-lag block ....98
Table 3-7 State space equations for DB controller in equivalent dq reference frame .................................................................................................................100
Table 3-8 Simulation results for VSC model verification............................107
Table 3-9 Summary of the large signal model of the AC grid in abc reference frame and small signal model in dq reference frame .................................................................108
Table 3-10 Large and small signal for DC link ........................................................................113
Table 3-11 Parameters for the DC link test ........................................................................114
Table 4-1 Equivalent Thevenin impedance of the AC grid ...................................................127
Table 4-2 Basic power flow equation .......................................................................................127
Table 4-3 Equations for the power flow study .........................................................................128
Table 4-4 Modes of the inner current controller (SCR=2) ......................................................131
Table 4-5 Participation factors of dominant state variables for selected modes of the inner DB current controller .........................................................................................132
Table 5-1 The units derivation for the PID coefficients ..........................................................177
Table 5-2 Inter-area modes of the integrating system ...............................................................186
Table 5-3 Approximate improvements on system damping: comparison of the results obtained from adding with equivalent damping torque (Figure 5-31) and the analysis for participation factor ........................................................................................................194
Table 5-4 Residue analysis of the system ..............................................................................202
List of Publications

Published


Papers in Preparation


[3] W. Liying, David J. Vowles and N. Ertugrul, "Robust controllers design for DB controlled VSC linked to a weak AC system"

[4] W. Liying, David J. Vowles and N. Ertugrul, "Damping controller design of DB controlled VSC operating in parallel with a Weak Multi-machine AC Power System"
Symbols

\[ A \] system matrix
\[ f \] filter-bus values of the VSC
\[ P \] active power
\[ ac \] alternating current quantity
\[ N \] base value
\[ C \] capacitance
\[ c \] converter terminal values of the VSC
\[ I \] current
\[ d \] d component in the dq frame
\[ D_e \] damping torque
\[ K_d \] derivative gain
\[ dc \] direct current quantity
\[ D \] feedthrough matrix
\[ i \] imaginary component in the grid RI frame
\[ L \] inductance
\[ B \] input matrix
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_i$</td>
<td>integral gain</td>
</tr>
<tr>
<td>$s$</td>
<td>Laplace factor</td>
</tr>
<tr>
<td>$\max$</td>
<td>maximum value</td>
</tr>
<tr>
<td>$\min$</td>
<td>minimum value</td>
</tr>
<tr>
<td>$o$</td>
<td>operating point value</td>
</tr>
<tr>
<td>$C$</td>
<td>output matrix</td>
</tr>
<tr>
<td>$\text{peak}$</td>
<td>peak value</td>
</tr>
<tr>
<td>$\theta$</td>
<td>phase angle</td>
</tr>
<tr>
<td>$\text{abc}$</td>
<td>phase quantities</td>
</tr>
<tr>
<td>$\text{PLL}$</td>
<td>PLL quantity</td>
</tr>
<tr>
<td>$K_p$</td>
<td>proportional gain</td>
</tr>
<tr>
<td>$q$</td>
<td>q component in the dq frame</td>
</tr>
<tr>
<td>$\text{C}$</td>
<td>quantity in converter dq frame</td>
</tr>
<tr>
<td>$\text{G}$</td>
<td>quantity in grid RI frame</td>
</tr>
<tr>
<td>$Q$</td>
<td>reactive power</td>
</tr>
<tr>
<td>$r$</td>
<td>real component in the grid RI frame</td>
</tr>
<tr>
<td>$\text{ref}$</td>
<td>reference value</td>
</tr>
<tr>
<td>$T_s$</td>
<td>sampling time constant</td>
</tr>
<tr>
<td>$s$</td>
<td>source values of the interconnected grid</td>
</tr>
<tr>
<td>$p$</td>
<td>values of controlled plant</td>
</tr>
<tr>
<td>$\text{db}$</td>
<td>values of DB current controller</td>
</tr>
<tr>
<td>$K_v$</td>
<td>gain of the voltage controlled oscillator</td>
</tr>
<tr>
<td>$U$</td>
<td>voltage</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>$\alpha$ component in the $\alpha\beta$ frame</td>
</tr>
<tr>
<td>$\beta$</td>
<td>$\beta$ component in the $\alpha\beta$ frame</td>
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### Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
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<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>AVM</td>
<td>Average Value Modeling</td>
</tr>
<tr>
<td>AVR</td>
<td>Automatic Voltage Regulator</td>
</tr>
<tr>
<td>DB</td>
<td>Dead Beat</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DG</td>
<td>Distributed Generation</td>
</tr>
<tr>
<td>EMT</td>
<td>Electro-Magnetic Transient</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response</td>
</tr>
<tr>
<td>GM</td>
<td>Gain Margin</td>
</tr>
<tr>
<td>GPS</td>
<td>Global Positioning System</td>
</tr>
<tr>
<td>GTOs</td>
<td>Gate Turn-off Devices</td>
</tr>
<tr>
<td>H∞</td>
<td>H Infinity</td>
</tr>
<tr>
<td>HSV</td>
<td>Hankel Singular Value</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistors</td>
</tr>
<tr>
<td>Im</td>
<td>Imaginary</td>
</tr>
<tr>
<td>IMC</td>
<td>Internal Model Control</td>
</tr>
<tr>
<td>ITAE</td>
<td>Integral of the Time Absolute-Error Products</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchhoff's Current Law</td>
</tr>
<tr>
<td>KVL</td>
<td>Kirchhoff's Voltage Law</td>
</tr>
<tr>
<td>LCC</td>
<td>Line-Commutated Control</td>
</tr>
<tr>
<td>LL</td>
<td>Lead-Lag</td>
</tr>
<tr>
<td>LMI</td>
<td>Linear Matrix Inequality</td>
</tr>
<tr>
<td>LTI</td>
<td>Linear Time Invariant</td>
</tr>
<tr>
<td>Max</td>
<td>Maximum</td>
</tr>
<tr>
<td>MIMO</td>
<td>Multi-Input Multi-Output</td>
</tr>
<tr>
<td>Min</td>
<td>Minimum</td>
</tr>
<tr>
<td>MTDC</td>
<td>Multi-Terminal Direct Current</td>
</tr>
<tr>
<td>PCC</td>
<td>Point of Common Coupling</td>
</tr>
<tr>
<td>PM</td>
<td>Phase Margin</td>
</tr>
<tr>
<td>PI</td>
<td>Proportional-Integral</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Lock Loop</td>
</tr>
<tr>
<td>POD</td>
<td>Power Oscillation Damping</td>
</tr>
<tr>
<td>PQ</td>
<td>Active-/Reactive- Power</td>
</tr>
<tr>
<td>PR</td>
<td>Proportional-Resonant</td>
</tr>
<tr>
<td>PSS</td>
<td>Power System Stabilizer</td>
</tr>
<tr>
<td>pu</td>
<td>Per Unit</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>Re</td>
<td>Real</td>
</tr>
<tr>
<td>RHP</td>
<td>Right Half Plane</td>
</tr>
<tr>
<td>SCR</td>
<td>Short Circuit Ratio</td>
</tr>
<tr>
<td>SISO</td>
<td>Single-In Single-Out</td>
</tr>
<tr>
<td>SVCs</td>
<td>Static Var Compensators</td>
</tr>
<tr>
<td>TF</td>
<td>Transfer Function</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>VSC-HVDC</td>
<td>Voltage Source Converter- High Voltage Direct Current</td>
</tr>
<tr>
<td>WAPOD</td>
<td>Wide Area Power Oscillation Damping</td>
</tr>
<tr>
<td>ZOH</td>
<td>Zero Order Holding</td>
</tr>
</tbody>
</table>
Chapter 1: Introduction

1.1 Background

As is known, the limited availability and environmental concern of fossil fuels, as well as the continuous growing demand of electricity, have caused renewable energy to become commercially attractive. However, the integration of large scale renewable energy sources into the power grid changes the characteristics of the supply in terms of the composition of energy generation, the transmission network, the technology and the economics of the electricity industry. This will be very different from the current situation in which fossil-fuel generation occupies the dominant position [1].

To allow the large scale integration of renewable energy sources into the grid, VSC-HVDC is a commonly developed power electronic converter. This converter topology is particularly suitable for long distance power transmission, such as in offshore wind farms. Since VSCs do not require commutating voltage from the connected AC grid, they are also highly effective in supplying power to isolated and remote loads and convenient when interconnecting distributed sources.
The existing transmission networks and power stations will not be able to meet the growing challenges of renewable energy transmission. The increasing penetration of power electronic converters into existing power systems have also caused several power system stability issues [2, 3]. The modern VSC-HVDC technology can help to solve the adverse impact on system stability and power quality issues. Furthermore, it can also significantly increase the transmission capacity and can provide flexible control of power flow. Therefore, it is envisaged that there is a strong need to investigate the design, operation and control of VSC-HVDC transmission links. This includes the link’s integration into the existing power network which may be notably weak as in the Australian case which is investigated in this thesis.

1.2 VSC-HVDC System

1.2.1 VSC Topology

A typical VSC converter station consists of a voltage source converter, a reactor, a transformer, a filter and a DC capacitor as shown in Figure 1-1a.

The detailed VSC circuit diagram is also given in Figure 1-1b which includes a conventional three phase six-switch converter. A number of series switching devices such as insulated gate bipolar transistors (IGBTs) or gate turn off devices (GTOs) can be used to increase the voltage blocking capability of the converter and hence increase the voltage rating of the HVDC transmission system. Note that the anti-parallel diodes are required in the converter to allow possible voltage reversals caused by changing external circuit conditions, thus facilitating four-quadrant operation of the converter. Note also that such voltage source converter can be treated as a voltage source from the AC side. The VSC controls the angle and voltage difference across the reactor and possibly transformer so as to regulate the AC power and reactive power delivered by the converter. The reactor also filters the AC harmonics. Reactive power compensation devices are not required as the converter can control the reactive power generation. Note that only a small AC filter will be required to eliminate higher order harmonics. The VSC acts as a constant current source on the DC side. The DC bus capacitor is required to store energy to facilitate the control of power flow and to reduce the DC-link harmonics.
1.2.2 Operation Principle of VSC

The operational principle of VSC can be explained using the following well-known power equations.

\[
P = \frac{U_s U_c \sin \delta}{X_L}
\]

\[
Q = \frac{U_s (U_s - U_c \cos \delta)}{X_L}
\]  (1-1)

Figure 1-1 A typical VSC topology connected to the AC grid (a) simplified diagram, (b) the details of the circuit including three phase two-level VSC using IGBTs.
Chapter 1: Introduction

Where $U_c$ is the fundamental frequency positive-phase sequence component of the converter output voltage magnitude; $U_s$ is the fundamental frequency positive-phase sequence component of the AC source voltage magnitude (see Figure 1-1a); $\delta$ is the phase angle difference between the converter and source voltage phasors ($\delta=\theta_s-\theta_c$) and $X_L$ is the inductance between the source and converter.

It can be easily seen from the above equations that the real power is primarily a function of $\delta$, whereas the reactive power is mainly determined by the difference ($U_s-U_c$) since $\cos\delta$ approaches 1. This indicates that the reactive power flows from the voltage with higher amplitude to the voltage with lower amplitude. This allows us to independently control the magnitude and the direction of real and reactive power synchronously by an appropriate control of the amplitude and the phase angle of the converter voltage. Normally, the pulse width modulation (PWM) control scheme is employed to realize the control requirement. However, due to the switched characteristics of $\hat{u}_c$, the modulation index $M$ of PWM (where $M=2U_{c\text{peak}}/U_{dc}$) should also be considered to determine its amplitude [2]. Here, the phase angle $\delta$ is determined by the reference modulation voltage. Therefore, the desired $\delta$ and $U_c$ can be obtained by appropriately adjusting the PWM outputs, which consequently regulate P and Q. This allows us to operate the VSC in four quadrants.

1.2.3 Characteristics and Applications of VSC-HVDC

The VSC-HVDC transmission technology provides an effective alternative to conventional power transmission and distribution. The unique features of this technology can be listed as below [4-9]:

1) Active and reactive power exchange can be controlled flexibly and independently.

2) The power quality and power system stability can be improved by means of fast continuously acting power oscillation damper; and/or power transfer controller.

3) This technology can supply AC systems with low short circuit capacity or even passive networks with no local power generation.

4) It can be used for the black start-up of a power grid.

5) There is no communication required between multiple converters, which can also be used to form a multi-terminal DC system (MTDC).

6) It has a fast recovery of its control capabilities after a grid fault.
7) It can reduce harmonics due to the adoption of higher switching frequencies, although this has an adverse effect of creating losses.

8) There is no need to reverse the DC voltage polarity when reversing the power direction.

9) Possible to develop small converters to reduce the space requirement.

10) It requires only compact filters.

The VSC-HVDC technology can also be applied in a wide range of applications due to the above mentioned characteristics [4, 5, 10-13]. For example, it can

- connect distributed small-scale power plants, small-medium sized hydropower plants, wind farms, tidal power stations, solar power stations and so on;
- operate asynchronously between AC systems with the same or different nominal frequencies.
- increase power capacity of urban centres.
- supply power to remote areas or even passive networks;
- be integrated in a multi-terminal system;
- improve the power quality of a distribution network;
- ensure the security and efficiency of power transmission;
- be applied to a deregulated power system.

The VSC-HVDC projects around the world are summarized in [8] and [14]. Among these the Hellsjön-Sweden prototype project 3MW, ±10kV was the first VSC-HVDC transmission project, which was commissioned in 1997. The world’s first HVDC project employing VSCs in a modular multilevel converter (MMC) topology was the Trans Bay Cable Project (TBC) of USA. It has a transmission capacity 400MW and ±200kV of DC voltage rating which was the highest rating for this type of technology until 2010 [15]. After that, the Caprivi link interconnector was commissioned in Oct 2010. This was the first ABB’s HVDC-Light transmission system (350kV, 300MW) to employ overhead line which is 950km long. The latest milestone is the Skagerrak 4 link from Denmark to Norway, for which the voltage rating is 500kV, the highest to date [16]. Note that it will be used as a reference for determining the DC voltage rating in this project.
1.3 Literature Review

1.3.1 Control Strategies of VSC-HVDC

The performance of a VSC-HVDC system depends on its control system and the system parameters. Therefore, it is very important to investigate the VSC-HVDC control system. In the following paragraphs the history on the development of VSC control strategy and a literature survey on controllers design for VSC operating under both strong and weak AC system conditions are reviewed and summarized.

1.3.1.1 History on Development of Control Strategy

The PWM control strategy in VSC-HVDC system accommodating IGBTs was initially proposed in the early 1990s’ [17-20]. However, in these studies only the phase shift angle $\delta$ between output fundamental frequency positive-phase sequence voltage and AC bus voltage was set as a control parameter, ignoring the amplitude of fundamental frequency positive-phase sequence voltage. Therefore, independent control of active and reactive power was not realized at that time. In these early schemes separate facilities were required to control reactive power. Therefore these early studies did not fully demonstrate the technological superiority of the VSC-HVDC technology. Later, in the mid to late 1990s’ a simpler and straight-forward control strategy based on the power control concept mentioned in section 1.2.2 is developed [21-23]. These control schemes were characterized by relatively low bandwidth and consequently these schemes are unable to damp various resonances that exist in the AC systems. Furthermore, these schemes did not have effective capabilities of limiting over current. Consequently, this control strategy is undesirable.

Vector current control is now widely employed worldwide. It has the characteristics that inherent converter current protection, fast dynamic responses and decoupled active power and reactive power control. Conventionally, it is realized through a hierarchical control structure including outer-loop controllers and inner current loop controllers (as shown in Figure 1-1b), within which a dq decoupling technique is applied [24].

Note that, the outer-loop controllers produce reference values for the faster acting inner-loop current-controllers, and typically, the sending-end converter controls the real power and the receiving-end converter regulates the DC voltage. However, it is sometimes the case that one end is designated for power flow control and the other end for DC voltage
control irrespective of the direction of power flow. The reactive power at either end of the link is controlled separately by the respective converters. The control of reactive power is used to control reactive power directly or indirectly as a means of controlling the power-factor or AC voltage at a designated bus. Due to the simplicity and robustness, double closed-loop vector oriented PI controllers have been utilized in compensating the system to achieve the desired performance. The inner-loop controllers employ feed-forward decoupled control to make the active- and reactive-current track the reference values produced by the outer-loop controllers [25].

1.3.1.2 Controller Design for VSC Operating Under Strong AC System Condition

The selection of the parameters of the PI compensators of the various VSC control systems is a key issue to ensure an adequate dynamic performance (including a fast response, and a sufficient stability margin for the VSC-HVDC transmission system). Note that the dynamic performance criteria typically results in conflicting requirements when tuning the PI controller parameters. Consequently, a compromise between the speed of response and stability for small disturbances is needed. Further compromises may also be needed to achieve adequate performance in response to large disturbances. The need to coordinate the tuning of several PI compensators is particularly challenging. Typically, the PI controller parameters of the various compensators are obtained by trial-and-error which relies heavily on the experiences and skills of the design engineers.

Very few publications were identified that quantify the selection and optimization of PI parameters associated with VSC control systems. The approach adopted in [26] applies a trial and error method with the objective of ensuring the transient stability of the system without using any theoretical evaluation criteria. In [27] frequency response analysis is used to obtain an envelope of PI compensator parameter values which satisfy specified stability criteria. Then an objective function is evaluated for each set of PI parameters in the above envelope using a detailed electro-magnetic transients (EMT) model. The set of PI parameters which minimizes the objective function is selected. The approach proposed in [27] was found to be promising but requires a significant amount of computation time because there is no mathematically derived procedure for selecting the next set of PI parameters on the basis of accumulated experience gained from the previous trials [28]. In addition, it does not provide any insight on how to adjust several PI parameters simultaneously. Although the papers in [29] and [30] apply optimization techniques based
on the Simplex Algorithm to different VSC-HVDC control systems, the selection of the initial set of parameters for input to the optimization algorithm is ad-hoc. In addition, the method tends to find a local optimum rather than the global optimum set of PI compensator parameters. References [31] and [32] propose approaches for determining the PI compensator parameters, but these methods do not include the simultaneous adjustment of several PI parameters. Therefore, it is desirable to develop a new methodology to determine these parameters.

1.3.1.3 Controller Design for VSC Operating Under Weak AC System Condition

It is noted that there are only a few research papers that consider the impacts of VSC-HVDC transmission systems connected to a weak grid. It is identified that the outer power loop, the inner current loop, the synchronization method and the input-output impedance can be studied in such grids that accommodate the VSC-HVDC system. The strength of the AC system to which the link is connected is determined by the short circuit ratio (SCR). The SCR is a ratio of the AC-system short-circuit capacity divided by the rated power of the HVDC link. The AC system strength is classified in [33] and given below in Table 1-1.

<table>
<thead>
<tr>
<th>Categories of SCR</th>
<th>SCR Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strong system</td>
<td>SCR≥3</td>
</tr>
<tr>
<td>Weak System</td>
<td>3 &gt; SCR ≥2</td>
</tr>
<tr>
<td>Very weak system</td>
<td>SCR&lt;2</td>
</tr>
</tbody>
</table>

A. Outer Loop Control

Controller design for VSC-HVDC converters connected to a strong AC system condition is simple and accurate enough to be designed based on a simplified model without considering the dynamics of the PLL and bus filter as in refs [31, 32, 34]. However, a robust controller design which is suitable for a wide range of equivalent grid impedances is challenging due to the resonances in both the low (1.5-15 rad/s) to high frequency range. In order to suppress the higher order harmonics caused by the converter switching, a third order LCL filter is conventionally adopted. In this approach, a higher order model is required to adequately represent the grid behaviour. This complicates the dynamics of VSC-HVDC control system particularly when a wide range of grid impedance
is considered. In a weak system, the voltage is sensitive to converter current, whereas the sensitivity can be ignored when the grid is strong. Moreover, the dynamics of the PLL and the bus filter also become significant in the dynamic performance of the system.

The literature survey has also considered how to improve the design and performance characteristics of the various outer loop controllers. It was reported in [35] that the flexible AC voltage control can be realized through optimum power and reactive power management to offer additional voltage support to reduce the impact of fast varying filter bus voltage. A non-linear eight state model of the VSC was developed in [36] by taking into account the dynamics of the PLL and the bus filter to accommodate the connection to weak AC grids. Based on this multi-input multi-output (MIMO) model, a robust H infinity (H∞) controller over a range of operating points is designed by employing linear matrix inequality (LMI) techniques [36, 37]. Two genetic algorithms based on direct search methods are also applied in [38] to optimize this type of controller.

**B. Inner Loop Control**

A challenging feature for the design of controllers associated with distributed generation (DG) systems is high grid impedance and resistance. Hence, the advanced techniques developed in the DG research area provide useful insights to controller design for VSC-HVDC system [39-42]. As discussed below it was suggested in previous studies that the instability problems associated with the connection of VSC-HVDC systems to weak AC grids can be divided into two categories: i) high frequency instability which can be yielded due to grid-converter resonance (e.g. LCL filter resonance) and interaction between the inner current control and the active damping controller [41, 43]; ii) low frequency instability which is highly influenced by the inner current control loop.

**a) High Frequency Instability**

Mitigation of the high frequency instability can be achieved by a number of alternative active damping control schemes which include: i) the utilization of poorly damped complex poles [43-45], ii) split capacitor [46, 47], iii) full state feedback control [48] and iv) virtual resistance [39-41, 49]. With the employment of active damping control, the open loop gain and bandwidth of the inner current controller are consequently increased and current harmonic distortion is reduced. As a result, the increased bandwidth facilitates the design and tuning of the outer-loop controller parameters.
b) Low Frequency Instability

In the following paragraphs the relative effectiveness of the PI, PR and DB inner-current controllers on mitigating the low frequency instability are summarized.

The conventionally adopted PI inner loop control is ineffective in weak AC application irrespective of the reference frame used. This is largely due to the weakness in the low bandwidth of the PI control and the disability to suppress the grid induced distortion and imbalance [50].

The PR controller developed in [50], which is tuned for the selective harmonics elimination, can relieve the above mentioned problem to some extent. However, this controller is very sensitive to variation in harmonic frequencies since it is tuned for pre-set harmonic frequencies. In addition, the high sensitivity to the grid impedance contributes to another drawback. This is due to the bandwidth of the current controller tends to be lower than the resonant frequencies with the increase of the grid impedance [43]. Consequently, the PR controller becomes failure.

Thanks to the high bandwidth of the DB controller, it does not only minimize the cross-coupling effects among the controller loops, but also maximizes the disturbance rejection ability against the grid distortion and the parametric uncertainties. Several DB control algorithms are reported in [51-53]. Therefore, it is necessary to review the various DB algorithms and explore their relative advantages and disadvantages. The current control schemes are also evaluated and verified in [54] and [55], which concluded that the DB control scheme is the best tailored current control scheme for a grid with large impedance. A more advanced and robust DB control is developed in the DG field which is designed based on a higher order augmented plant model by taking into account the filter and the active damping resistance during the control process [40]. However, in this thesis the former conventional DB control scheme is adopted, while the latter scheme is left for subsequent investigation.

C. Synchronization Method

The conventional d-q-z type PLL [52, 56, 57] for extracting the phase angle of the grid voltages is employed in this thesis. However, there are also alternative approaches in the literature as discussed below. A small number of investigations on the synchronization methods as virtual flux estimation and power synchronization control are identified.
The virtual flux estimation method investigated in [58-60] is a synchronization method based on “virtual flux” concept. It is found in [59] that this scheme can be used to improve the operation of VSC in weak grids with high impedance seen from the converter. The mechanism adopted here is to synchronize to a voltage at a relatively stable point, consequently achieve a more robust control system. However, normally, the closer to the converter terminal in terms of choosing a synchronization point, the more accurate of the control system performance can be achieved. Hence, a compromise needs to be made to achieve a satisfactory performance. Nevertheless, a contrary viewpoint is presented in [61] that virtual flux estimation is robust for distributed grid but cannot outperform conventional PLL.

The power synchronization might be viewed as a combination of power-angle control and vector current control as reported in [62, 63]. Reference to the power synchronization control, two types of complex outer controllers are developed in [64] which are based on H∞ and IMC control theories respectively. It was concluded that both of these two controllers perform similarly.

D. Input/output Impedance

To investigate the overall stability of the interconnected VSC-HVDC link and power system, a new method based on the converter output impedance together with grid input impedance is developed in [65]. The primary criteria used here is to evaluate whether the ratio between the grid impedance and the converter output impedance satisfies the Nyquist stability criterion, which is also discussed in [66, 67]. It was concluded that the admittance shaping technique provides an effective method in optimizing the control, the bus filter and on the design of the controllers.

1.3.2 Small Signal Modeling

As indicated in [68], there is a need to develop a detailed linear time-invariant (i.e. small-signal) model of VSC-HVDC links. Such modelling is needed to understand how the sub-components impact on the dynamic performance of both the VSCs and the wider interconnected power system to which the link is connected. Detailed modelling of the links is particularly required when the converters are connected to weak parts of the grid. Clearly, the pre-requisite for such a small-signal model is a detailed three-phase non-linear model including comprehensive representation of the switching controls. Linearization of
such a non-linear model facilitates the application of well-established linear systems analysis and controller design methods. The applications include such as the design of the VSC controls to power systems incorporating VSC-HVDC links and other technologies based on VSCs. These techniques include but are not limited to eigen-analysis, frequency response analysis, residue analysis, classical controller design methods as well as modern controller design methods. It is well known that the conventional eigen-analysis provides a powerful tool for the system stability study only if the analytical model is sufficiently accurate to represent the target plant.

The small signal modeling of a conventional line-commutated converter HVDC (LCC-HVDC) is reported in [56, 69, 70]. A relatively early investigation of the small signal model of VSC is also given in [71]. Due to the development of the off-shore wind industry specifically in Europe, the multilevel VSC technology with cascaded bridge is considered a common solution by main system manufactures. Due to this impetus, a good number of studies on small signal modeling are given in [72-76]. However, the latter models have inner current controllers that are based on the PI control scheme rather than the DB controllers that are employed in this thesis. In reference [77], two types of inner current controllers: i) predictive controller and ii) fast PID control scheme are investigated. It can be noted here that the predictive controller mentioned in ref [77], is in fact similar to the conventional PI control with additional current feed-forward technique.

As an alternative to dq-frame controllers in the grid connected converters, PR control is also widely used owing its superiority to the PI controller under unbalanced condition. However, due to the presence of the time-varying components, the small signal model of PR controlled VSC is very challenging. Using the method proposed in [78], a small signal model of the PR controlled VSC is developed in [79, 80], which also studied the dynamics of a DC voltage control loop. All these works facilitate the ongoing research studies with regards to the area of PR controlled VSCs.

As stated earlier, the DB control scheme is the best tailored inner current scheme for a weak AC grid connected VSC. However, no studies were reported previously on the small signal model of such controller, which will also be investigated in this thesis.
1.3.3 Grid Interconnection

Modern large interconnected power systems are characterized by the requirement to transmit large amounts of power over long distances, large-scale of integration of renewable energy, and deregulation of power system operations. These and other factors are significant driving forces behind the development of power systems with a hybrid AC/DC structure. The hybrid AC/DC grid is not only capable of enhancing the system stability through relieving the congestion and transmission bottlenecks, it also acts as a firewall against cascade disturbances, further preventing blackouts [4, 81]. However, the integration of VSC-HVDC links may deteriorate the damping of the inter area modes [82, 83]. In addition, the sub synchronous resonance is also a common problem since the first adverse interaction between the turbine-generator torsional modes of the vibration and a conventional HVDC transmission system was observed in Square Butte Electric Coop Project in North Dakota [84] dating back to 1977. The solutions for enhancing the damping of electromechanical modes of oscillation in a system can be divided into two categories: i) PSSs fitted to synchronous generators [85]; ii) Power Oscillation Dampers (PODs) fitted to flexible alternating current transmission systems (FACTs) [3, 86-89], HVDC links [4, 82, 83, 90-94]; and potentially asynchronous generators such as wind turbines [95]. Note that since the VSC-HVDC is the primary research topic in this thesis, the majority of the review has been performed about the HVDC damping controller.

It was reported in [83] that the VSC-HVDC link has four controllable quantities, within which the inter-area modes are able to be decoupled by two ΔPs and the local modes within the area where the converter located can be simultaneously damped by each ΔV (or ΔQ). However, it is investigated in [90] that active power control is more effective in damping electromechanical modes of oscillation than reactive power control. Therefore, in this thesis active power and the DC voltage are considered as the most suitable inputs to PODs fitted to VSC-HVDC links.

Depending on whether the input signal to the POD is local or remote it is classified as either: i) a local POD or ii) a wide area power oscillation damper (WAPOD). Due to the limitations in signal communication, the local POD is adopted initially. However, with the developments in Global Position System (GPS) and satellite communication technologies, the WAPOD is may now be technically feasible. It is conceivable that the combination of these two types of PODs will become increasingly important as power systems evolve.
CHAPTER 1: INTRODUCTION

The effectiveness of the POD design depends on a number of factors including the location of controlled plant (relates to controllability); the modal content of the selected stabilizing signal (relates to observability); and the measurement accuracy of the selected signal. In [96], to damp out the inter-area mode in the Hydro-Quebec network, two different approaches on feedback signal selection were investigated. They were i) the geometric approach (also known as controllability/observability index) and ii) the residue approach. It was concluded that the geometric approach is more reliable and useful in this application, rather than the residues approach which is widely used. Moreover, it was also concluded that the global signal input is more effective than the local signal. However, it should be noted that, this is not always true. Differences in performance between local POD and WAPOD vary depending on several factors including: i) the actual tuning of those PODs, ii) the availability of measurements with good ‘modal content’, iii) the power system configuration and disturbances, iv) the location of VSC and v) the specific operating point [89].

Later, in addition to the aforementioned controllability/observability and residue methods, the Hankel singular value (HSV) approach is added to complete the comparison in [97]. It was concluded that based on a small two-area system, the residue and Hankel singular value methods perform in a similar way. However, in a medium scale system, the system damping performance was better when signal selection was based on the HSV method. There are also a number of studies on investigations of the design approaches of PSS and POD, which are documented in [98-103].

Recently, several investigations on enhancing system stability through POD are published based on the Hydro-Québec network [96], the Nordic power system [89], the reduced Great Britain model [104], the China Southern Power Grid (CSG) [105], and the New England test system integrated with the New York power system [94]. In fact, Australia also has an important track record in utilizing PODs for damping inter-area modes of oscillation. References [98] and [100] formed the basis of PODs fitted to SVCs in Brisbane that were required to stabilize the interconnection between NSW and Queensland [106]. Furthermore, improved damping controls fitted to the SVCs in the Brisbane area were investigated in [107] in the mid to late 2000’s. The new controls were based on local bus frequency measurements.
In Australia, significant amount of geothermal energy is available in the area of Cooper Basin near South Australia and Queensland. It can be foreseen that the energy production will be economically harvested by the geothermal resources in the future, although this has not yet been established, only a number of pilot projects are being undertaken to establish the technical and economic feasibility. However, such resources are located far away from the major cities and loads. Therefore, this thesis considers as a case study the possible future development of parallel VSC-HVDC and AC links to transmit power generated from large geothermal sources in the far north east of South Australia to northern New South Wales and the mid north of South Australia. Although there are some pilot studies on utilizing these geo-thermal energy [108, 109], the study undertaken in this thesis are different, which is characterized by a more suitable power transmission option and employing a detailed DB controlled VSC model. Furthermore, the focus of the case study is the design of the VSC-HVDC link controllers and the damping performance of the system, including the design of damping controllers.

1.4 Thesis Overview

1.4.1 Research Gap

Based on the literature review conducted above, several significant limitations are identified which form the basis of the main original research topics in this thesis.

- A simple and effective methodology for the controller design and optimization of VSC-HVDC systems connected to weak grids is not available.
- A comparison of various types of DB current controllers for the VSCs in terms of principle, parameter sensitivity as well as robustness against large disturbances has not been studied previously.
- Stability studies involving the DB controlled VSC-HVDC links are only based on time-domain analysis in the previous studies. The small signal analysis, which is essential to characterize the system characteristics, of such discrete power system has not yet been reported due to the difficulty that the time varying nature prevents the direct application of small signal studies.
• Controller design in a weak multi-machine AC system integrated with VSC-HVDC links by taking into account the robustness of the controllers for a wide range of operating conditions and system disturbances has not been studied in the literature.

• The possible interactions between VSC-HVDC links and the extended weak Australian grid have not been reported.

• Finally, the compensation methodologies (PSS, POD and WAPOD) for a secure operation of VSC-HVDC links embedded in an extended weak Australian grid also require further investigation.

This thesis aims to address the above research gaps.

1.4.2 Thesis Outline

The thesis is divided into six main chapters which have the following contents.

Chapter 2: Investigates three types of linear inner-current loop controllers in terms of principle and controller design. A new methodology for determining controller parameters based on simplified linear models of VSC-HVDC links and simultaneously optimizing several control loops are presented.

Chapter 3: VSC control systems typically involve transformations between fundamental frequency positive-phase sequence signals in a stationary reference frame (either the abc or αβ reference frame) and the corresponding DC signals in the synchronous dq reference frame. A feature of the proposed transformation method in this chapter is that it facilitates the development of an equivalent linear time-invariant representation of controllers that in practice are time-varying. In addition, a small signal model for the discrete DB controlled VSC is also developed and verified systematically against the detailed PSCAD model from which it is derived.

Chapter 4: The methodology for the robust outer loop controller design of a VSC-HVDC transmission system is developed which considers the operating range of the converters and the grid characteristics as represented by the SCR and X/R ratio.

Chapter 5: An in-depth investigation of the small signal stability of a simplified model of the Australian power system incorporating a VSCHVDC link is undertaken. The case study also includes supplementary damping controllers design to achieve adequate system damping performance.
Chapter 6: The chapter summarizes the conclusions drawn in each chapter and also reiterates the original contributions.
Chapter 2: VSC-HVDC Control Structures

This chapter aims to evaluate various inner current controllers widely employed by the VSC-HVDC systems. The primary focus is mainly set on three linear control structures, i.e. i) the conventional decoupled PI-controller in the synchronously rotating reference frame, ii) Proportional Resonant (PR) controller and iii) discrete Dead Beat (DB) controller in the natural stationary reference frame. The controller design methodologies are also investigated in this chapter.

2.1 Introduction

In a typical VSC-HVDC system, the hierarchical control structure is conventionally adopted including system control, converter control and firing control from top to the bottom, as shown in Figure 1-1b. Here, only two levels of the converter control that the outer power-, voltage- control and the inner current control are discussed. The main function of the outer loop controller is to control voltage or power of the three-phase converter. Yet, the inner current control is mainly responsible for current control according to current references that are generated by the outer loop controllers. For example, to
realize sinusoidal current wave tracking with a unity power factor by using inner current control. Since the inner current loop control is much faster than the outer loop control, hence, the inner current control loop plays a significant role in improving the overall performance of the control system.

Usually the adopted outer loop control contains a) constant DC voltage control; b) constant real power control; c) constant reactive power control; d) constant frequency control and e) constant AC voltage control. Generally speaking, a, b and d are a group of incompatible control objects, which means a VSC station can only work in either of the three control modes. In order to maintain the real power balance and DC voltage stability, there must be one VSC station adopts constant DC voltage control, and others can work in b or d mode. For the same reason, the c and e are also two incompatible control modes. Note that one VSC station can only realize one control mode.

Converter control is the core strategy of the VSC-HVDC system, and it is therefore being set as the research emphasis of this chapter.

In accordance with the linearity properties, the control method can be classified into two categories: i) linear control scheme and ii) non-linear control scheme [61]. The linear controllers can also be classified as the conventional decoupled PI-controller in the synchronously rotating reference frame, the PR controller in the stationary reference frame, and the predictive controller involving feed-forward and DB control scheme, as shown in Figure 2-1. All these linear controllers are the focus of this chapter and will be explained further in the following section.

![Figure 2-1 Current control classifications](image)
2.2 Background Study for System Modeling

Frame transformation plays a significant role in developing the control algorithm. Therefore, the frame transformation criteria will be explained first.

2.2.1 Frame Transformation

2.2.1.1 Clark Transformation

Let us assume that a symmetrical sinusoidal three phase voltage \( u_{abc} \) with a constant angular frequency \( \omega_0 \) is under investigation. Hence, the voltage equations can be given by equation (2-1), where \( u_p \) and \( \theta_{PLL} \) denote the peak value and initial phase angle of the rotating vector \( \hat{U} \) respectively.

\[
\begin{align*}
  u_a(t) &= u_p \sin[\omega_0(t)t + \theta_{PLL}(t)] \\
  u_b(t) &= u_p \sin[\omega_0(t)t + \theta_{PLL}(t) - \frac{2}{3}\pi] \\
  u_c(t) &= u_p \sin[\omega_0(t)t + \theta_{PLL}(t) + \frac{2}{3}\pi]
\end{align*}
\] (2-1)

The adopted Clark Transformation matrix for transformation from the converter stationary abc natural reference frame to \( \alpha\beta \) reference frame is given in equation (2-2), and the time domain expression of the resultant \( \alpha\beta \) components is given in equation (2-3) [85].

\[
\begin{bmatrix}
  u_a \\
  u_{\beta} \\
  u_{0}
\end{bmatrix} = \frac{2}{3} \begin{bmatrix}
  1 & -\frac{1}{2} & -\frac{1}{2} \\
  -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\
  -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2}
\end{bmatrix} \begin{bmatrix}
  u_a \\
  u_b \\
  u_c
\end{bmatrix} \quad (2-2)
\]

\[
\begin{bmatrix}
  u_a \\
  u_{\beta}
\end{bmatrix} = u_p \begin{bmatrix}
  \sin[\omega_0(t)t + \theta_{PLL}(t)] \\
  -\cos[\omega_0(t)t + \theta_{PLL}(t)]
\end{bmatrix} \quad (2-3)
\]

Therefore, the positive sequence voltage for the balanced three phase supply voltage can be represented using the stationary \( \alpha\beta \) reference frame and abc natural reference frame as given in equation (2-4) and shown in Figure 2-2 [110], where the scaling of the factor K
can be equal to 2/3 to ensure power invariance, alternatively it can also be chosen to $\sqrt{2/3}$ to ensure the voltage invariance [111].

$$\hat{U} = u_a(t) + j u_\beta(t) = K \cdot (u_a(t) + u_b(t) \cdot e^{j\frac{2\pi}{3}} + u_c(t) \cdot e^{j\frac{4\pi}{3}})$$ \hspace{1cm} (2-4)

The inverse voltage transformation equations are also given below in equation (2-5),

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & \frac{1}{2} \\ -\frac{1}{2} & \sqrt{3} & \frac{1}{2} \\ -\frac{1}{2} & -\sqrt{3} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} u_a' \\ u_\beta' \\ u_0' \end{bmatrix}$$ \hspace{1cm} (2-5)

![Figure 2-2 Representation of rotating vector in converter including stationary $\alpha\beta$ reference frame and abc natural reference frame.](image)

**2.2.1.2 Transformation from Stationary $\alpha\beta$ Reference Frame to Rotating dq Reference Frame**

Reference to the relative motion theory, it can be noted that the dq reference frame rotates at the same frequency $\omega_0$ with the rotating vector $\hat{U}$. Therefore observing from vector $\hat{U}$ it will appear stationary, and will contain a set of DC terms which will facilitate the controller design and modeling of VSC system. As shown in Figure 2-3, the q-axis is chosen aligning with the opposite direction of the rotating vector, and d-axis is orthogonal to the q-axis, lagging it by 90°. This transformation can be given in a vector form as in equation (2-6), and in matrix form as in equation (2-7). Equation (2-8) and equation (2-9) provide the reverse transformation from dq reference frame to $\alpha\beta$ reference frame written in a vector form and matrix form respectively.
\[ u_{dq}(t) = u_{\alpha\beta}(t)e^{-j(\omega_0(t)t + \theta_{PLL}(t))} \] (2-6)

\[
\begin{bmatrix}
  d \\
  q 
\end{bmatrix} =
\begin{bmatrix}
  \cos(\omega_0(t)t + \theta_{PLL}(t)) & \sin(\omega_0(t)t + \theta_{PLL}(t)) \\
  -\sin(\omega_0(t)t + \theta_{PLL}(t)) & \cos(\omega_0(t)t + \theta_{PLL}(t))
\end{bmatrix}
\begin{bmatrix}
  \alpha \\
  \beta 
\end{bmatrix} \] (2-7)

\[ u_{\alpha\beta}(t) = u_{dq}(t)e^{j(\omega_0(t)t + \theta_{PLL}(t))} \] (2-8)

\[
\begin{bmatrix}
  \alpha \\
  \beta 
\end{bmatrix} =
\begin{bmatrix}
  \cos(\omega_0(t)t + \theta_{PLL}(t)) & -\sin(\omega_0(t)t + \theta_{PLL}(t)) \\
  \sin(\omega_0(t)t + \theta_{PLL}(t)) & \cos(\omega_0(t)t + \theta_{PLL}(t))
\end{bmatrix}
\begin{bmatrix}
  d \\
  q 
\end{bmatrix} \] (2-9)

**2.2.2 Transient Mathematical System Model**

From the perspective of controller design, it is important to understand the plant to be controlled. The single line diagram of VSC-HVDC is given below in Figure 2-4, where R and L represent the internal resistance and summation of the inductance of VSC transformer and converter reactor respectively.

Assuming that the system is operating under a balanced condition, considering only the fundamental frequency positive-phase sequence components of \( u_{abc} \) and \( i_{abc} \) (i.e. point B in Figure 2-4), the fundamental frequency positive-phase sequence components of the
three-phase AC voltage at the VSC terminals (i.e. point A in Figure 2-4) $u_{c,abc}$ are able to be given by equation (2-10) [112-114].

$$
\begin{align*}
U_{sa} - U_{ca} &= L \frac{di_{sa}}{dt} + R_i s_a \\
U_{sb} - U_{cb} &= L \frac{di_{sb}}{dt} + R_i s_b \\
U_{sc} - U_{cc} &= L \frac{di_{sc}}{dt} + R_i s_c
\end{align*}
$$

(2-10)

Due to the DC link capacitor C, the converter DC voltage ($U_{dc}$) and currents ($i_{dc}$ and $i_L$) are related, which can be given by equation (2-11),

$$
C \frac{dU_{dc}}{dt} = i_{dc} - i_L
$$

(2-11)

If we apply Clark Transformation (2-5), the equation (2-10) can be transformed to $\alpha\beta$ reference frame as in equation (2-12),

$$
\begin{align*}
U_{s\alpha} - U_{c\alpha} &= L \frac{di_{s\alpha}}{dt} + R_i s_{\alpha} \\
U_{s\beta} - U_{c\beta} &= L \frac{di_{s\beta}}{dt} + R_i s_{\beta}
\end{align*}
$$

(2-12)

Since the fact that the relationship between $\alpha\beta$ and $dq$ reference frames is determined by equation (2-8). Then, the voltage and current equations in $\alpha\beta$ reference frame becomes,

$$
\begin{align*}
U_{s\alpha\beta} &= U_{s\alpha\beta} e^{j\omega t} \\
U_{c\alpha\beta} &= U_{c\alpha\beta} e^{j\omega t} \\
i_{s\alpha\beta} &= i_{s\alpha\beta} e^{j\omega t}
\end{align*}
$$

(2-13)

Substituting equation (2-13) into equation (2-12) yields to the following set of equations,

$$
\begin{align*}
U_{s\alpha\beta} e^{j\omega t} - U_{c\alpha\beta} e^{j\omega t} &= L \frac{d(i_{s\alpha\beta} e^{j\omega t})}{dt} + R_i s_{\alpha\beta} e^{j\omega t} \\
U_{s\beta\beta} e^{j\omega t} - U_{c\beta\beta} e^{j\omega t} &= e^{j\omega t} L \frac{d(i_{s\beta\beta} e^{j\omega t})}{dt} + L_i s_{\beta\beta} e^{j\omega t} + R_i s_{\beta\beta} e^{j\omega t} \\
U_{s\alpha\beta} e^{j\omega t} - U_{c\alpha\beta} e^{j\omega t} &= e^{j\omega t} L \frac{d(i_{s\alpha\beta} e^{j\omega t})}{dt} + j\omega L i_{s\alpha\beta} e^{j\omega t} + R_i s_{\alpha\beta} e^{j\omega t}
\end{align*}
$$

(2-14)

If we extend these equations to the matrix form and apply the Laplace Transformation, then VSC system’s mathematical model can be given in the $dq$ reference frame by equation (2-15).

$$
\begin{bmatrix}
    u_{sd} \\
    u_{sq}
\end{bmatrix} =
\begin{bmatrix}
sL + R & -\omega L \\
\omega L & sL + R\end{bmatrix} \begin{bmatrix}
i_{sd} \\
i_{sq}
\end{bmatrix} +
\begin{bmatrix}
    u_{cd} \\
    u_{cq}
\end{bmatrix}
$$

(2-15)
2.3 Description of Controllers and Determination of Controller Parameters

Three main linear inner current controllers are discussed in this sub-section. First, the mechanisms are introduced and explained in detail. Then, a methodology concerning the selection of controller parameters is proposed for each type of current controllers, and the simulation models established on a PSCAD/EMTDC platform are also employed for verification purpose.

2.3.1 Proportional Integral Control

In steady state, the dq components of the variables are typically transformed by using abc-dq (i.e. Park’s) transformation modulation, which synchronously rotate with the voltage vector, but behave as DC quantities as given earlier. A PI control is normally associated with the control structure (see Figure 2-5b), since it has the capability to reduce the steady-state error.

The reason to present a more detailed explanation of PI control here is to provide a better understanding on the algorithm and its operation principle.

Note that equation (2-15) can be rearranged for the currents as given below,

\[
\begin{align*}
  s_i_{sd} &= \frac{-R}{L} i_{sd} + \omega i_{sq} + \frac{1}{L} (u_{sd} - u_{cd}) \\
  s_i_{sq} &= \frac{R}{L} i_{sq} - \omega i_{sd} + \frac{1}{L} (u_{sq} - u_{cq})
\end{align*}
\] (2-16)

Let us assume that the VSC output voltage is determined by the following feed-forward decoupled PI controller [113],

\[
\begin{align*}
  u_{cd} &= (K_{ip} + \frac{K_d}{s}) (i^*_{sd} - i_{sd}) + \omega L i_{sq} + u_{sd} \\
  u_{cq} &= (K_{ip} + \frac{K_d}{s}) (i^*_{sq} - i_{sq}) - \omega L i_{sd} + u_{sq}
\end{align*}
\] (2-17)

where \( K_{ip} \) and \( K_{il} \) are proportional and integral gains, \( i^*_{sd} \) and \( i^*_{sq} \) are the current references of the d,q axes respectively, and \( i_{sd} \) and \( i_{sq} \) are the measured converter output currents in terms of the d-, q- axis respectively.

Substituting equation (2-17) into equation (2-16),
2.3. DESCRIPTION OF CONTROLLERS AND DETERMINATION OF CONTROLLER PARAMETERS

\[
\begin{bmatrix}
    s i_{sd} \\
    s i_{sq}
\end{bmatrix} = \begin{bmatrix}
    -\frac{R - (K_p + \frac{K_d}{s})}{L} & 0 \\
    0 & -\frac{R - (K_p + \frac{K_d}{s})}{L}
\end{bmatrix} \begin{bmatrix}
    i_{sd} \\
    i_{sq}
\end{bmatrix} - \frac{1}{L} \left( K_p + \frac{K_d}{s} \right) \begin{bmatrix}
    i_{sd}' \\
    i_{sq}'
\end{bmatrix}
\] (2-18)

From the above equation, it can be easily seen that, d- and q- axis current \( i_d \) and \( i_q \) are successfully decoupled. Hence, the control strategy structure using the above discussions can be illustrated as in Figure 2-5b.

Figure 2-5 (a) The diagram of the inner and outer controllers; (b) Inner current control loop.
Figure 2-5a shows a three-phase, two-level VSC adopting a voltage oriented vector control structure implemented in the synchronously rotating dq-reference frame, where the three-phase AC voltage at the network node of the VSC and the three-phase current flowing from the network into the VSC are denoted by $u_{s_{abc}}$ and $i_{s_{abc}}$ respectively, C is the capacitance of the DC filter, and the entire control system including the outer power and voltage loop, the inner current control loop together with phase locked loop (PLL) control are also given. The error of $P_{\text{ref}}$ and $P$ is the input to the sending end controller, while the error of $U_{\text{dc}_{\text{ref}}}$ and $U_{\text{dc}}$ is the input to the receiving end controller. Note that, only the positive sequence current is the control target considered. The reference value of the converter terminal voltage $u_{c_{abc}_{\text{ref}}}$ is generated from the control system then fed into the VSC-HVDC system through the firing control that ‘PWM control’. Lastly, it should be noted that the reference phase angle of control system is extracted from the filter bus voltage by the PLL control.

2.3.1.1 Controller Design and Optimization for PI Controlled VSC-HVDC System

As is well known, the performance of a system highly depends on the performance of its controllers, which was emphasised here about the importance of controller design. This section proposes an approach to the selection and optimization of the parameters of the PI compensators in the various control loops of a VSC-HVDC transmission system using a decoupled control scheme.

In this study, an optimization algorithm based on the simplex method is adopted. The main objective of this method is to simultaneously minimize the weighted sum of the ‘integral of the time absolute-error products’ (ITAE) of the active power, the reactive-power, the DC voltage and the inner current controllers of the respective VSCs. The initial values of the PI compensator parameters for input to the optimization algorithm are obtained by the application of classical frequency response design methods to simplified linear models of the open-loop transfer functions (TFs) of VSC-HVDC control system. The optimization process is applied to a detailed electromagnetic transient (EMT) model of the VSC-HVDC system to which a large disturbance is applied.

The effectiveness of the optimized PI compensator parameter settings are assessed in terms of rise-time, overshoot, and settling times for a range of disturbances applied to the detailed EMT model. On the basis of these assessments, modifications to the weightings of
2.3. Description of Controllers and Determination of Controller Parameters

the error signals are found to be necessary to obtain good performance according to the specific control design requirements.

Figure 2-6 shows the flow chart of the process for determining the PI compensator parameters for VSC-HVDC control system.

Figure 2-6 Flow chart of the process for determining the PI compensator parameters for VSC-HVDC control system

In the below paragraphs the design parameters of the controllers are explained systematically.

A. Transfer Function of Control Loops

a) Inner Current Control loop

The inner current loop control shown in Figure 2-7 is composed of 4 parts: i) PI compensator \( H_{c1}(s)=(K_{p1}+K_{i1}/s) \); ii) equivalent simplified filter model \( G_1(s)=1/(R(\text{pu})+s\cdot X_L(\text{pu})/\omega) \); iii) converter circuit \( G_2(s) = K_{PWM}/ (1+1/2\cdot T_s\cdot s) \) and iv) measurement circuit \( G_3(s)=1/(1+T_s\cdot s) \). Hence, the compensated open loop transfer function of the inner current control loop can then be written as
where the plant transfer function \( G_{pl}(s) \) is

\[
G_{pl}(s) = G_1(s) \cdot G_2(s) \cdot G_3(s) = \frac{K_{PWM}}{1 + \frac{1}{2} T_s \cdot s} \cdot \frac{1}{1 + T_i \cdot s} \cdot \frac{1}{R(pu) + s \frac{X_L(pu)}{\omega}}
\]  

Here, \( T_s \) is the sampling interval of the inner current control loop, \( K_{PWM} \) is the equivalent gain of the PWM, which is normally defined by \( K_{PWM} = 2 \cdot \frac{u_{ac}}{U_{dc}} \), where \( u_{ac} \) is the peak value of the terminal line-to-ground voltage of the converter.

\[
F_i(s) = H_{i1}(s) \cdot G_{pi}(s)
\]

\[
F_2(s) = H_{i2}(s) \cdot G_{p2}(s)
\]

\[
F_3(s) = H_{i3}(s) \cdot G_{p3}(s)
\]

**Figure 2-7** Detailed inner current control loop in pu system

**b) Outer DC Voltage Control Loop**

The outer DC voltage control loop shown in Figure 2-8 is composed of 5 parts: (i) PI compensator \( H_{c3}(s)=(K_{p3}+K_{i3} / s) \); (ii) equivalent inner current control loop \( G_4(s)=1/(1+T_{eq} \cdot s) \), where \( T_{eq} \) is the equivalent time constant of first order approximation of current control loop [31, 32]; (iii) line circuit \( G_5(s)=1/(s \cdot C_{pu}) \); (iv) current transmission relationship according to power balance between AC side and DC side \( G_6(s)=\frac{3u_{sqpu}}{2U_{dcpu}} \) and (v) measurement circuit \( G_7(s)=1/(1+T_i \cdot s) \) [115]. The compensated open loop transfer function of the outer DC voltage control loop can then be written as,

\[
F_2(s) = H_{i2}(s) \cdot G_{p2}(s)
\]

where the plant transfer function \( G_{p2}(s) \) is
2.3. DESCRIPTION OF CONTROLLERS AND DETERMINATION OF CONTROLLER PARAMETERS

\[ G_{p2}(s) = G_4(s) \cdot G_5(s) \cdot G_6(s) \cdot G_7(s) = \frac{1}{T_{eq} \cdot s + 1} \cdot \frac{u_{sq,pu}}{U_{dc,pu}} \cdot \frac{1}{s \cdot C_{pu}} \cdot \frac{1}{T_s \cdot s + 1} \]  \hspace{1cm} (2-22)

\[ P_s = 3/2 \cdot (u_{sq} \cdot i_{sq} + u_{sd} \cdot i_{sd}) \]
\[ Q_s = 3/2 \cdot (u_{sq} \cdot i_{sd} - u_{sd} \cdot i_{sq}) \]  \hspace{1cm} (2-23)

According to Figure 2-3, the q-axis is aligned with the opposite direction of U_s phasor. Therefore, u_{sd} equals to be 0. The power equation can be simplified as,
\[ P_s = 3/2 \cdot u_{sq} \cdot i_{sq} \]
\[ Q_s = 3/2 \cdot u_{sq} \cdot i_{sd} \]  \hspace{1cm} (2-24)

The above equation shows that the active power and reactive power can be controlled independently by controlling the q axis current i_{sq} and the d axis current i_{sd}.

The outer- active and reactive power control loops are shown in Figure 2-9. For initial design purposes the network voltage can be assumed to be fixed with a value of one per-unit, i.e. u_{sq}=1.0.

The outer- active/reactive power control loops is composed of 4 parts: i) PI compensator \((H_{c3}(s)=(K_{p3}+K_{i3}/s))\); (ii) equivalent inner current control loop \((G_q(s)=1/(1+T_{eq} \cdot s))\); (iii) power balance transmission relationship \((G_9(s)=3/2u_{sq}(pu))\) and (iv) measurement circuit \((G_{i0}(s)=1/(1+T_c \cdot s))\). The compensated open loop transfer function of the outer active/reactive power control loop is shown in equation (2-25),
\[ F_3(s) = H_{c3}(s) \cdot G_{p3}(s) \]  \hspace{1cm} (2-25)
Figure 2-9 (a) Block diagram of active power control scheme in pu system; (b) block diagram of reactive power control scheme in pu system.

where the plant transfer function $G_{p3}(s)$ is

$$G_{p3}(s) = G_i(s) \cdot G_q(s) \cdot G_{t0}(s) = \frac{1}{T_{eq} \cdot s + 1} \cdot \frac{3}{2} u_{sq}(pu) \cdot \frac{1}{T_s \cdot s + 1} \quad (2-26)$$

Simplifying equation (2-26) by eliminating third order term, equation (2-27) is obtained

$$F_i(s) = (K_p + K_i l s) \cdot \frac{1}{4T_s s + 1} \cdot \frac{3}{2} u_{sq}(pu) \quad (2-27)$$

**B. Initial Estimates of PI Compensator Parameters**

The initial values of the PI compensator parameters are selected based on the application of frequency response design methods to simplified linearized models of the various control loops. The PI compensator parameters are chosen such that the gain margin (GM) and phase margin (PM) of the compensated open-loop system are respectively within the ranges of $GM \geq 6$dB and $40 \leq PM \leq 60$ deg. The following design criteria are applied to the closed-loop step responses:
2.3. Description of Controllers and Determination of Controller Parameters

- the rise time must be less than 30 ms for underdamped system or less than 70 ms for a damped system;
- the overshoot must be no more than 30% [27].

C. Optimization Consideration and Simplex Algorithm

Due to the adoption of hierarchical control strategy, the VSC at each end of the link has four double closed-loop PI controllers which must be integrated. Therefore the coordination of the controller parameters is a challenging problem for the designer. In total, 12 parameters must be determined (note that since the respective d- and q-axis inner-loop current controllers are identical the number of controller parameters is reduced from 16 to 12). Note also that the selection of an appropriate objective function for the optimization procedure is also critical.

The Simplex Algorithm is considered as comparably faster optimization technique in terms of reaching the optimal solution compared with other optimization techniques [29, 30, 116]. The algorithm is a geometric object formed by N+1 vertices in the N-dimensional space (number of parameters) and suitable for cases where the number of variables ranges from 2 to 20, which makes it the most suitable optimization method here. It successively compares the values of the objective function at the N+1 vertices of a simplex and discards the worst one then another new value of vertex is selected to be calculated in the same procedure until the optimum point is reached.

D. System Objective Functions

The ITAE index is a simplified form of the integral time absolute error and is one of the error-integral indices used to evaluate the dynamic response of a control system [27, 28, 117]. The ITAE index $J_{\text{ITAE}}$ is given by,

$$J_{\text{ITAE}} = \int_0^T t |e| dt$$  \hspace{1cm} (2-28)

Where $t$ is the time since the disturbance is applied, $|e|$ is the absolute value of the control system error and $T$ is a finite time chosen so that the integral approaches to a steady-state value and is usually chosen as the settling time $T_s$.

For a VSC-HVDC transmission system which includes multiple control loops, the objective is to minimize the weighted sum of ITAE indices $O_f(X)$ associated with each of the control systems [28].
\[ O_f(X) = \sum_i m_i f_i(X) \]  
(2-29)  
\[ f_i(X) = \sum_j \omega_j \int |e_j(t)| dt \]  
(2-30)

where \( f_i \) is the performance index for evaluating controller operation performance; \( m_i \) is the weighting factor applied to the \( i^{th} \) objective function (\( i \) is the number of controllers); \( e_j(t) \) is the error between the real value of the \( j^{th} \) controlled variable and its reference value; and \( \omega_j \) is the weighting factor applied to the ITAE of the \( j^{th} \) controlled variable. The vector \( X=(X_1 X_2 \ldots X_n) \) in the equations is the set of control system parameters, i.e. the parameters of the PI compensators.

2.3.1.2 Computer Simulation of the PI controlled VSC-HVDC system

The approach has been tested on a detailed EMT model of a VSC-HVDC system using the control strategy described in 2.3.1.1. The system block diagram is given in Figure 2-10. The model data is given in the Appendix A. The process of initializing the parameter values of all the PI compensators is listed below.

---

A. Initial Setting of PI Parameters by Classical Frequency Response Methods

a) Inner Current Control Loop

By substituting the system parameters that are given in Appendix A into equation (2-19), equation (2-31) is obtained.
2.3. **Description of Controllers and Determination of Controller Parameters**

\[
F_i(s) = \left( K_{p1} + K_{i1} / s \right) \cdot \frac{0.78509}{1+3.7 \times 10^{-4} s} \cdot \frac{1}{1+7.4 \times 10^{-4} s} \cdot \frac{1}{9.5493 \times 10^{-4} s + 0.0015} \\
= \frac{0.78509K_{p1}}{2.615 \times 10^{-3} s^2 + 1.06 \times 10^{-6} s^3 + 0.0009566 s^2 + 0.0015 s}\
\]

(2-31)

The frequency response of the plant transfer function \( G_{p1}(s) \) in equation (2-20) is calculated and displayed in Bode plot as shown in Figure 2-11 (solid blue line). According to the requirements listed in section 2.3.1.1 B, it can be seen that the phase margin of 39.4 deg is smaller than the minimum requirement of 40 deg. For the uncompensated system the gain margin is 11.4dB, the overshoot of the step response is 30%, and the settling time is 0.01s, all of which are acceptable (see solid blue line in Figure 2-12). PI compensation is applied \( (K_{p1}=0.62, K_{i1}=53) \) to reduce the gain cross-over frequency thereby increasing the phase margin to 50.4 deg and the gain margin to 17.1dB (dashed green line in Figure 2-11). The overshoot of 23.6% (dashed green line in Figure 2-12) is lower than the original 30%. Although the settling time has been increased to 0.025s, it is still acceptable.

![Figure 2-11 Open-loop Bode plots of the current controller transfer function (i) without PI control (blue solid line); (ii) with PI compensation using initial parameters (green dashed line).](image-url)

33
PI compensation is applied ($K_{p1}=0.62$, $K_{i1}=53$) to reduce the gain cross-over frequency thereby increasing the phase margin to 50.4 deg and the gain margin to 17.1dB (dashed green line in Figure 2-11). The overshoot of 23.6% (dashed green line in Figure 2-12) is lower than the original 30%. Although the settling time has been increased to 0.025s, it is still acceptable.

**b) Outer Constant DC Voltage Control**

Substituting numerical values of the system parameters in equation (2-22) yields the following compensated open-loop transfer-function for the DC voltage controller,

$$F_2(s) = \frac{K_{p3} + K_{p3} \cdot s}{3.33592 \times 10^{-3} s^3 + 0.1127 s^2}$$

(2-32)

The frequency response of the plant transfer function $G_{p2}(s)$ in equation (2-22) is calculated and displayed in Bode plot as shown by the solid blue line in Figure 2-13. The phase margin of 88.5 deg is significantly higher than the specified maximum of 60 deg, and the settling time of 0.432 (solid blue line in Figure 2-14) is considered excessive. The bandwidth of the controller is increased with the PI compensation ($K_p=20$, $K_i=1000$). The compensated open-loop transfer-function (dashed green line in Figure 2-13) has a phase margin of 47.1 deg, decreased settling time 0.046s (dashed green line in Figure 2-14). The overshoot of 30.2% (dashed green line in Figure 2-14) is relatively high, but it will be revised in the next optimization procedure.
2.3. Description of Controllers and Determination of Controller Parameters

![Figure 2-13](image1.png)

Figure 2-13 Open-loop Bode plots of the outer DC controller transfer-function (i) without PI compensation (solid blue line); and (ii) with PI compensation using the initial parameters (dashed green line).

![Figure 2-14](image2.png)

Figure 2-14 Step responses of the outer DC controller transfer-function (i) without PI compensation (solid blue line) and (ii) with PI compensation using the initial parameters (dashed green line).

c) Outer Active/Reactive Power Control

Similarly, inserting the numerical values into equation (2-25), the following compensated open-loop transfer-function of the active/reactive power controller is obtained.

\[ F_i(s) = -\frac{3}{2} \cdot \frac{K_{ps} + K_{ps} \cdot s}{29.6 \times 10^{-4} \cdot s^3 + s^2} \]  

(2-33)
The frequency responses of the active/reactive power controller without PI compensator are shown in Figure 2-15 (solid blue line). The phase margin is 89.7 deg. The PI compensator ($K_p = 3.65$, $K_i = 20.0$) is used to increase the gain cross-over frequency, thereby increasing the speed of response. The phase margin is reduced to 50.6 deg (dashed green line in Figure 2-15), which is still acceptable.

**B. Simplex Algorithm for Multi-objective Optimization of VSC-HVDC System**

The objective function of multi-objective optimization for VSC-HVDC system is expressed as in equation (2-34) which is obtained from equation (2-30)

$$O_j (X) = \int_0^T t |e_{Q, rec}| dt + \int_0^T t |e_{P, rec}| dt + \int_0^T t |e_{Q, inv}| dt + \int_0^T t |e_{dc, inv}| dt$$

$$+ \int_0^T t |e_{L, inner, rec}| dt + \int_0^T t |e_{L, inner, inv}| dt + \int_0^T t |e_{L, outer, inv}| dt + \int_0^T t |e_{L, outer, inv}| dt$$

(2-34)

Where $e_j(t)$ is the difference between the $j^{th}$ controlled variable and its reference value. The value of $\omega_j$ is set to unity indicating that all of the controlled variables have the same importance.

The vector $X = (K_{p1} K_{i1} K_{p2} K_{i2} K_{p3} K_{i3} K_{p4} K_{i4} K_{p5} K_{i5} K_{p6} K_{i6})$ represents the variables.
As it is well known, the control system is required to operate satisfactorily when being subject to both large and small disturbances. For the purpose of parameter optimization the disturbance is the reversal of the power-order from +1 pu to -1 pu at time $t = 2s$. The value of the optimization function is computed and is then passed to the Simplex Optimization Algorithm which computes an update set of the PI compensator parameters, $X$. The final dynamic response of the system with the optimized set of PI compensator parameters obtained with the objective function equation (2-34) is given in Figure 2-16. Table 2-1 shows the initial and optimized values of the control parameters and the resultant values of the objective function.

Figure 2-16 Responses of VSC-HVDC modelled in PSACD following a reversal of the power order for (i) the initial set of PI compensator parameters (red line); (ii) the parameters obtained with the optimization function (2-34) (blue line) and (iii) the parameters obtained with the refined optimization function (2-35) (cyan line). The reference values of the variables are shown in green line.

As it can be seen in Figure 2-16a, the optimization does greatly improve the tracking capability of power order, where the settling time is reduced from 500ms to 40ms. It can be reported that the value of the objective function is also reduced from 3.41 to 3.29 within duration of 3s. Moreover, the resulting transient performance including the relatively long
settling times and the relatively high overshoot of the other reactive power controllers and DC voltage controller are considered unsatisfactory (see Figure 2-16c). Therefore the definition of the objective function is refined according to the controller design requirement as illustrated in Figure 2-16. As an example, an increased weighting of 4 is applied to the DC voltage controller and the active power controller which results in the following objective function as equation (2-35).

\[
O_f(X) = \int_0^T e_{q_{rec}} \, dt + 4 \cdot \int_0^T e_{p_{rec}} \, dt + \int_0^T e_{q_{inv}} \, dt + 4 \cdot \int_0^T e_{u_{dc-inv}} \, dt
\]

\[
+ \int_0^T e_{u_{inner-rec}} \, dt + \int_0^T e_{u_{inner-inv}} \, dt + \int_0^T e_{u_{inv-inv}} \, dt + \int_0^T e_{u_{inv-inv}} \, dt
\]

(2-35)

It can be seen from Figure 2-16 that the performance of the active and reactive power controllers at the sending end are barely altered as a result of the refined optimization function. However, the dynamic performance of the DC voltage controller and the receiving end reactive power controller are improved significantly with refined objective function. The values of the new objective function have been reduced from 4.51 to 4.4729 within duration of 4s after optimization. To conclude, the dynamic behaviour of the VSC-HVDC system is improved with the refined set of PI parameters.
C. Summary of Proposed Controller Design Methodology

A methodology for the design of the control system of a VSC-HVDC transmission system is developed in this section. An initial set of PI compensator parameters is determined according to the frequency response analysis of the open loop transfer functions of simplified linear models of the VSC-HVDC control system. This initial set of controller parameters is then optimized by the application of the Simplex Algorithm. The objective is to simultaneously minimize the weighted sum of the “integral of the time absolute-error products” (ITAE) of the power, reactive-power, DC voltage and current controllers of the respective VSCs. The methodology has been demonstrated by simulation studies based on a detailed EMT model of a VSC-HVDC system. It is found that the objective function for the optimization function must be carefully chosen to obtain adequate performance.

It should be clarified that, in the proposed new design methodology, neither the design of starting point for the simplex algorithm by using classical control technique nor the simplex algorithm for optimizing the control parameters is new, but the combination of these approaches has not been recorded in the literatures, which can be treated as new. In addition, it also worth noting that this controller design methodology is only applicable for relatively strong system, in other words, the system which is not operating point dependent. For a weak AC system, the controller design method should take into account the dynamics of the filter and PLL which play a significant role in the system stability. This will be further discussed in Chapter 4 later.

2.3.2 Proportional Resonant Control

2.3.2.1 Principle

The PR control is developed based on the use of generalized integrator. Paper [118] has mapped out how to derive PR controller through the synchronous frame PI control. In addition, paper [79] provided a simpler method to obtain the relationship between the PR control and the PI control based on a block diagram approach [78]. Furthermore, paper [119] extends the previous work while developing a stationary frame controller PRX2 that is an exact equivalence to the decoupled d-q frame PI controllers by adding another two cross-coupling branches X-control and X-feedback. A set of stationary frame controllers have been obtained based on this PRX2 controller by eliminating one of the cross-coupling
CHAPTER 2: VSC-HVDC CONTROL STRUCTURES

branches or all of them (which is the exact PR controller). Results showed that it is this elimination that caused the increase of the frequency sensitiveness. This study offers a systematic method to understand this type of control in detail, and explains the discrepancies from the frequency analysis and experimental verification point of views.

A more complicated small signal model of PR controlled VSC was first proposed in paper [79] and thesis [80], which provides researchers a valuable tool to understand how such controller can affect the stability of an entire system.

One of the most preferable characteristics of PR controllers is it is easy to compensate on the low-order harmonics. This is done simply by positioning the generalized integrators that tuned to resonate at the harmonic frequencies to be compensated, in parallel with the main controller without affecting the dynamics of the entire closed-loop system as shown in Figure 2-17 [54, 120].

The typical transfer function of PR controller is given by,

\[ G_{PR}(s) = K_p + K_i \frac{s}{s^2 + \omega_0^2} \]  \hspace{1cm} (2-36)

The harmonic compensator transfer function of PR controller is defined as,

\[ G_{HC}(s) = \sum_{h=3,5,7} K_{ih} \frac{s}{s^2 + (h\omega_0)^2} \]  \hspace{1cm} (2-37)

This is because the PR controller works at a very narrow band around the resonant frequency \( \omega_0 \). However the bandwidth of these compensators has to be smaller, lower enough than the bandwidth of the system to prevent triggering the system low frequency
instability [121]. Moreover, an extremely high gain (near the resonant frequency) can be achieved offering a fast dynamic response. Therefore, it can realize the zero steady state tracking error for sinusoidal signals [119, 122]. This control scheme offers a better capability when regulating the negative-sequence control target since it has symmetrical characteristics in the frequency response plot. In other words, it is superior to PI controller under unbalanced situation [119]. However, the biggest drawback of this control structure is its high sensitiveness to frequency fluctuation. In addition to this, it is hard to insert the harmonic compensators into the system when the interconnected system becomes weak, which is characterized by a relatively narrow bandwidth. In this case, modified active damping controller together with PR controller is required as investigated in paper [43].

2.3.2.2 Controller Design

Applying Laplace Transformation to the \( \alpha \beta \) reference frame mathematical model of VSC system equation (2-12), equation (2-38) can be obtained, which is also illustrated in Figure 2-18.

\[
(R+sL) \cdot i_{\alpha\beta} = u_{\alpha\beta} - u_{\text{caf}} \tag{2-38}
\]

![Figure 2-18 Diagram of \( \alpha \beta \) reference frame mathematical model of VSC system](image)

Figure 2-18 Diagram of \( \alpha \beta \) reference frame mathematical model of VSC system

Figure 2-19 shows the diagram of the simplified \( \alpha \beta \) reference frame model of PR current controlled VSC system, where \( \omega_0 \) represents the resonance frequency of the controller, \( K_{p1} \) is the proportional gain and \( K_{i1} \) is the integrator of the PR controller respectively.

![Figure 2-19 The simplified model of PR current controlled VSC system in \( \alpha \beta \) reference frame](image)
Then the closed-loop transfer function of the system yields to equation (2-39),

\[
G_p(s) = \frac{I_{sofi}}{I_{sofi-ref}} = \frac{K_{p1}(s^2 + \alpha_0^2) + sK_{i1}}{(R + sL)(s^2 + \alpha_0^2) + K_{p1}(s^2 + \alpha_0^2) + sK_{i1}}
\]  

The proportional gain of the controller $K_{p1}$ can be tuned by root locus theory provided that the integrator gain $K_{i1}$ is set to be zero first. Then the integrator of the controller $K_{i1}$ can be obtained by frequency response analysis of the open loop transfer function. As suggested in [123], the controller parameters for PR scheme should be kept the same as the parameters of PI controllers.

### 2.3.3 Dead Beat Control

The working principle of DB control is to increase the step-response speed of a system by manipulating the input signal into two parts. In such control scheme, a proportionally larger step signal (positive) drives the system response fast to reach the original constant value, which is followed by a delayed smaller step signal (negative) to cancel the remainder transient response of the former step [52]. Since the DB control itself is allowed to reach its reference value at the end of next switching period, consequently one sample time delay is introduced in this method of control. In addition, DB control can be divided into two parts depending on whether or not the computational delay time being taken into consideration as demonstrated in Figure 2-20. This sub-section of the study also investigates the operation and control algorithm design of DB controllers, and presents the results about the system stability and the sensitivity analyses of plant parameter variations for the four types of DB current controllers.

![Figure 2-20 The categories of DB current controllers](image)
2.3.3.1 Model of the System

The principal block diagram of the digital DB current controlled VSC system is given in the Figure 2-21, which includes three main blocks: the phase locked loop, the feed-forward loop and the DB current control loop. In the figure, the fundamental frequency positive-phase sequence components of three-phase AC voltage at the network node of the VSC and the three-phase current flowing from the network into the VSC are denoted by $U_{\text{abc}}$ and $I_{\text{abc}}$ respectively. $R_{\text{ac}}$ and $L_{\text{ac}}$ in the figure are the resistance and inductance of the Thevenin equivalent circuit of the AC system. In addition, $R_{\text{v}}$ and $L_{\text{v}}$ represent the resistance and inductance of converter; and $C$ is the capacitance of the DC filter. The modulation input voltage signal $U_{\text{v,abc}_\text{ref}}$ of the SPWM (a block for generating pulse signal) is composed of two parts: the output of voltage prediction block $U_{\text{v,abc}_2}$ and the output of the DB current control block $U_{\text{v,abc}_1}$.

![Digital DB current controlled VSC system](image)

The measured PCC voltage $U_{\text{f,abc}}$ in Figure 2-21 needs to be filtered out and then be added with a $3T_s/2$ time delay before sending to the modulation signal. This is due to the fact that a time delay of $T_s/2$ is introduced by the zero order holding (ZOH) block and also the sampling block contributes an additional time delay $T_s$, where $T_s$ is the sampling
interval [53, 54, 124]. The DB current control block in Figure 2-21 generates a pre-calculated additional voltage that is equal and opposite to the voltage reduction caused by the $R_v$ and $L_v$. This allows the current in the inductance is not affected by the PCC filter bus voltage. The PLL is used for synchronizing the PCC voltage. A dq to abc reference frame transformation block is also needed in the control system. The phase forward loop block in the control system is employed for time delay compensation.

### 2.3.3.2 DB Current Control with One Sample Time Delay

The closed-loop DB current control block without considering the computation time delay is illustrated in Figure 2-22. The internal model control for design of DB control can be expressed by using the following set of equations [51],

\[
G_{DB}(z) = \frac{G^{-1}(z)}{z-1} = \left(\frac{z^{-1}}{T_s}\right) (L_v + R_v) / (z-1)
\] (2-40)

\[
\Rightarrow \frac{u_{va_{-1}}((k+1)T_s)}{\Delta I(kT_s)} = \left(\frac{L_v}{T_s} + (R_v - \frac{L_v}{T_s})z^{-1}\right) / (1 - z^{-1})
\] (2-41)

\[
u_{va}((k+1)T_s) = \frac{L_v}{T_s} \Delta I(kT_s) + (R_v - \frac{L_v}{T_s})\Delta I((k-1)T_s)
+ u_{va_{-1}}(kT_s) + u_{fa}((k+1)T_s)
\] (2-42)

where $G_{DB}(z)$ is the transfer function of the current control, $u_{va_{-1}}$ is the first part of VSC input voltage generated by DB current controller, and $kT_s$ represents the $k^{th}$ time interval, $u_{va}$ is the total input voltage for VSC, $u_{fa}((k+1)T_s)$ is the predicted filter bus voltage at $(k+1)T_s$ time interval, and $\Delta I$ represents the current change order. Hence the control algorithm can be implemented by using equation (2-42).

\[
\begin{array}{c}
\text{I}_{a_{\text{ref}}} \\
\rightarrow \\
\Delta I \\
\leftarrow \\
\text{I}_a \\
\end{array}
\]

Figure 2-22 The closed-loop DB current Control

The closed-loop transfer-function of the one sample time delay DB current control with the presence of the one sample computation time delay can be given by,
\[ G_{DB_{cl}}(z) = \frac{z^{-1}/(z-1)}{1+z^{-1}/(z-1)} = \frac{z^{-1}}{z-1+z^{-1}} = \frac{1}{z^2 - z + 1} \] (2-43)

Therefore, one sample delay DB current control does work at the stability margin with two poles which are \( z_{1,2} = 1/2 \pm \sqrt{3}j \) (in the presence of one sampling period computational delay).

A. Reducing the Proportional Gain Method

This method used in papers [54, 124] does move the poles inside the unit circle, but at the cost of changing the closed-loop gain, which increases the phase difference between the reference and output current. For example, by changing the proportional gain part \( L_v/T_s \) of the controller to \( L_v/(2T_s) \) and \( R_v \) to \( R_v/2 \), the system characteristic equation becomes \( z^2 - z + 1/2 = 0 \). This results in two new poles as \( z_{1,2} = 1/2 (1 \pm j) \), which are inside the unity circle making the system stable as illustrated in Figure 2-23,

![Figure 2-23 Pole-zero map of the one sample delay system: red cross: one sample delay DB without considering the computation delay time; blue cross: represents one sample delay DB considering the computation delay time; green cross: represents reducing the proportional gain;](image-url)
B. Smith Predictor Method

The one sample delay DB current controller with Smith Predictor by considering the computation delay has the same performance with the two-sample delays DB current controller [51], which can be verified by using the derivation process given below.

The principle of Smith Predictor is that the output of the delayed DB plant model should ideally be cancelled through the feedback while the non-delayed process remains unchanged [125].

\[
G_{sp}(z) = \frac{G_{DB}(z)}{1 + G_{DB}G(z)(1 - z^{-1})} = \frac{G_{DB}(z)}{1 + z^{-1}}
\]

\[
= \frac{G^{-1}(z)}{(z-1)(1 + z^{-1})}
\]

2.3.3.3 DB Current Control with Two Sample Time Delays

In the following paragraphs, the control algorithms of two sample delays DB current control schemes based on internal model control (IMC) and solving feedback TF approaches are analysed below.
A. IMC Design for DB Current Controller

The ‘delayed’ plant model \( G(z) = z^{-1}G(z) \) is a second order system [51] and therefore the controller should be designed according to the following equation,

\[
G_{DB2}(s) = \frac{\alpha^2}{s^2 + 2s\alpha}G^{-1}(s)
\]

(2-45)

where, \( \alpha \) represents the bandwidth of the low pass filter adopted for damping purpose.

After discretizing the equation (2-45), the following controller is obtained,

\[
G_{DB2}(z) = \frac{\alpha^2}{((z-1)/T_s)^2 + 2\alpha(z-1)/T_s}G^{-1}(z) \bigg|_{z=\frac{1}{T_s}}
\]

(2-46)

Expanding and rearranging equation (2-46), we can obtain,

\[
u_{u,x-1}((k+1)T_s) = \frac{L}{T_s} \Delta I((k+1)T_s) + (R_v - \frac{L}{T_s})\Delta I(kT_s) + u_{u,x-1}((k-1)T_s)
\]

(2-47)

The developed control algorithm is very similar to the one used in [54], which clearly demonstrate the derivation of the control algorithm from a different point of view (IMC).

The algorithm can be implemented in PSCAD according to Figure 2-25.

![Internal model control design for DB implementation block](image)

Figure 2-25 Internal model control design for DB implementation block

B. Solving Feedback Transfer Function of DB Current Controller

The algorithm is obtained by solving the feedback transfer function of the closed-loop DB current controlled VSC model, also named as AC current tracking control, has been studied in [52] firstly and then successfully applied in [53, 126]. The control block diagram of solving feedback transfer function method in z domain is given below in Figure 2-26.
Figure 2-26 The block diagram of solving feedback transfer function DB current control

In the above figure, the block $G_{db}(z)$ and the feedback loop transfer function $G_F(z)$ are given by,

$$G_{db}(z) = \frac{N_1}{1 + N_2 z^{-1}} \quad (2-48)$$

$$G_F(z) = N_2^2 \quad (2-49)$$

where, $N_1 = -R_i / (1 - N_2)$, $N_2 = e^{-(R_i/I_s)T_i}$

The control algorithm can be implemented in PSCAD using the following equation (2-50) and is also illustrated in Figure 2-27.

$$N_1 \Delta I(kT_i) - N_2 u_{va-1}(kT_i) = u_{va-1}((k+1)T_i) \quad (2-50)$$

Figure 2-27 The structure of the solving feedback transfer function DB current controller

2.3.3.4 System Stability Analysis

The system stability analysis is done through frequency response analysis of the open loop transfer function of the simplified model of each controller. Table 2-2 shows the open loop transfer function of each DB current controller, and Figure 2-28 is given to summarize the frequency and step response of various DB controllers.
2.3. DESCRIPTION OF CONTROLLERS AND DETERMINATION OF CONTROLLER PARAMETERS

Table 2-2 Open loop transfer function of DB current controllers

<table>
<thead>
<tr>
<th>Types of DB controller</th>
<th>Open loop transfer function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reducing the proportional gain method</td>
<td>$z^2/(2\cdot(1 - z^{-1}))$</td>
</tr>
<tr>
<td>Smith predictor and IMC based two sample delays DB</td>
<td>$z^2/(1 - z^{-1}) \cdot (1 + z^{-1})$</td>
</tr>
<tr>
<td>Solving feedback transfer function based two sample delays DB</td>
<td>$z^2 \cdot e^{-2RvTs/Lv}/(1 - z^{-1} e^{-2RvTs/Lv})$</td>
</tr>
</tbody>
</table>

Figure 2-28 Frequency response and step response of various DB current controllers
As they are shown and observed in Figure 2-28 that the Smith Predictor method, the IMC method and the solving feedback TF method have nearly the same bandwidth, the same cut-off frequency and the same settling time. The performance of the reducing gain method is observed slightly poor specifically with a relatively narrower bandwidth, higher overshoot and longer settling time. Note that, the results in Figure 2-28 are obtained based on the simplified linear models under the assumption that the voltage applied across the AC side L/R circuit is unlimited. It is done for analytical purpose only, and which is not the authentic case in practice.

2.3.3.5 Sensitivity to Plant Parameters

The expressions of the sensitivity to plant parameters for each of the four controllers are shown in Table 2-3 which are derived according to the sensitivity formula defined as the percentage change in overall transfer function divided by percentage change in the plant transfer function [12], The sensitivity formula is depicted by,

\[ S(s) = \frac{\Delta G(s)}{\Delta G_p(s)} = \frac{\partial G(s)}{\partial G_p(s)} \cdot \frac{G_p(\sigma)}{G_p(s)} \]

\[ = \frac{\partial (G_{db}(s) \cdot G_p(s))}{\partial G_p(s)} \cdot \frac{G_p(s)}{G_p(s)} \]

\[ = G_{db}(s) / (1 + G_p(s)G_{db}(s) \cdot G_p(s))^2 \]

\[ \Rightarrow S(s) = \frac{1}{1 + G_p(s)G_{db}(s) \cdot G_p(s)} \]  

(2-51) 

(2-52)

Table 2-3 Sensitivity to plant parameters

<table>
<thead>
<tr>
<th>Controller</th>
<th>Sensitivity Expressions</th>
<th>Sensitivity Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reduce Gain</td>
<td>( \frac{1 - z^{-1}}{2 - 2z^{-1} - z^{-2}} )</td>
<td>0.2239</td>
</tr>
<tr>
<td>Smith Predictor &amp; IMC</td>
<td>( 1 - z^{-2} )</td>
<td>0.6173</td>
</tr>
<tr>
<td>Solving Feedback</td>
<td>( 1 - e^{-2\alpha_T}z^{-2} )</td>
<td>0.6152</td>
</tr>
</tbody>
</table>
It has been observed through the simulation studies that the sensitivity of one sample delay DB with reducing gain has the lowest sensitivity to plant parameters with respect to the operational frequency of 50Hz. The remaining other three two sample delays DB controllers demonstrate similar higher sensitivity values reference to the plant parameters.

2.3.3.6 Computer Simulation of DB Current Controller

The simulation model has been developed by using the equivalent circuit model shown in Figure 2-21 and the block diagrams given in Figure 2-25 and Figure 2-27, and the complete system was implemented in PSCAD. In addition, in order to improve the dynamic performance of the controller, a disturbance observer [127] is introduced in each control structure. The simulated circuit parameters are given in the Table 2-4.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>The rated power</td>
<td>75 MW</td>
</tr>
<tr>
<td>AC bus voltage</td>
<td>62.5kV</td>
</tr>
<tr>
<td>Inductance, L_v</td>
<td>0.15 pu</td>
</tr>
<tr>
<td>Resistance, R_v</td>
<td>0.0015 pu</td>
</tr>
<tr>
<td>Sampling time period, T_s</td>
<td>0.001s</td>
</tr>
</tbody>
</table>

A. Step Response Simulation of the DB Current Controllers

It is expected from a control system to operate satisfactorily when it is subject to both large and small disturbances. For the purpose of evaluating the performance of the transient operation, the simulation studies are carried out by varying the level of the active current reference from -1 pu to -2 pu and followed by an increase from -2 pu to -1.8 pu.
CHAPTER 2: VSC-HVDC CONTROL STRUCTURES

a) Reduce gain results

b) Smith Predictor results
2.3. Description of Controllers and Determination of Controller Parameters

c) Internal model control results

- Grid current
- Error (pu)

Graphs showing the response of different current references and error over time.
CHAPTER 2: VSC-HVDC CONTROL STRUCTURES

Figure 2-29 PSCAD step response simulation results of the DB current controller

It can be observed from Figure 2-29a that the reducing gain method has a frequently altered current as seen from dq synchronous reference frame plots due to the existence of phase difference caused by reducing the gain. The settling time of this controller is fast, but its overshoot in reactive current is also the highest among these four controllers, which is not desirable. The Smith Predictor method has approximately the same performance with IMC based DB when being subject to the step response tests. However, the overshoot in reactive current is observed slightly higher than IMC based DB controller. Compared with the IMC based method, the solving feedback TF method has a much shorter settling time, but with a slightly higher reactive current overshoot. The summary of the characteristics of the simulation results are given in Table 2-5.

Table 2-5 Summary of specific data obtained from Figure 2-29

<table>
<thead>
<tr>
<th>Controller Type</th>
<th>Step Test Type</th>
<th>Settling Time (ms)</th>
<th>Overshoot (%)</th>
<th>Overshoot Reactive Current (%)</th>
<th>Largest Error (pu)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reduce Gain</td>
<td>Large Step</td>
<td>14.9</td>
<td>16</td>
<td>84.6</td>
<td>0.479</td>
</tr>
<tr>
<td></td>
<td>Small Step</td>
<td>8</td>
<td>2.5</td>
<td>2</td>
<td>0.2</td>
</tr>
<tr>
<td>Smith Predictor</td>
<td>Large Step</td>
<td>26</td>
<td>25</td>
<td>48.8</td>
<td>0.349</td>
</tr>
<tr>
<td></td>
<td>Small Step</td>
<td>20</td>
<td>1</td>
<td>5.46</td>
<td>0.110</td>
</tr>
<tr>
<td>IMC Designed</td>
<td>Large Step</td>
<td>25</td>
<td>17.2</td>
<td>34</td>
<td>0.358</td>
</tr>
<tr>
<td></td>
<td>Small Step</td>
<td>21</td>
<td>4.9</td>
<td>5</td>
<td>0.067</td>
</tr>
<tr>
<td>Solving Feedback</td>
<td>Large Step</td>
<td>14.5</td>
<td>20</td>
<td>44.78</td>
<td>0.3348</td>
</tr>
<tr>
<td></td>
<td>Small Step</td>
<td>14.9</td>
<td>16</td>
<td>84.6</td>
<td>0.479</td>
</tr>
</tbody>
</table>
The simulation results presented here simply aim to verify the accuracy of the analysis given. The observed discrepancies are highly induced by the model linearization. It can be concluded that the entire performance of a controller is a trade-off between the response speed and reactive current overshoot. Furthermore, the solving feedback transfer function method proves to be superior to the other methods specifically during the large step response with a fast settling time and reasonable reactive current overshoot.

B. DB Current Control System Performance Simulations under Plant Parameter Variations

In this part of the simulation study, only the IMC based method and solving feedback transfer function method have been considered, since the one sample delay with Smith Predictor is approximately equal to the IMC based two sample delays DB current control. Therefore, the reducing gain method can be analysed as one sample delay DB with controller designed by halving the original plant parameters.

In order to examine the effect of parameter variation in each controller, the mean deviation examination method [52] is used in this study. The different mean deviation values equation (2-53) are used by varying the plant parameter value for three different I_d and I_q specifications, where I_d and I_q represent for the current reference in the dq reference frame.

\[
\text{Mean Deviation} = \frac{\sqrt{(I_d - I_{d0})^2 + (I_q - I_{q0})^2}}{\sqrt{I_{d0}^2 + I_{q0}^2}}
\] (2-53)

where, I_{d0} and I_{q0} represent the resulted current under original plant parameter.

The simulation results shown in the Table 2-6 demonstrate that the resistance has little effect on the sensitivity, which is mainly determined by the inductance. The sensitivity of solving the feedback transfer function method is somewhat lower than the IMC based DB controller in this particular case, and it is the same with the analysis given in section 2.3.3.4. However, the simulation result is significantly smaller than the results given in section 2.3.3.4, which is likely due to the inaccuracy introduced during simplification. The simulation results show that the output of control system have an approximate 3% variation when with the 10% change in an inductance value.
Table 2-6 Mean derivation of simulation results

<table>
<thead>
<tr>
<th></th>
<th>IMC(%)</th>
<th>SF(%)</th>
<th>IMC(%)</th>
<th>SF(%)</th>
<th>IMC(%)</th>
<th>SF(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(I_q)</td>
<td>(I_d)</td>
<td>(I_q)</td>
<td>(I_d)</td>
<td>(I_q)</td>
<td>(I_d)</td>
</tr>
<tr>
<td>Original Plant</td>
<td>-1</td>
<td>0</td>
<td>0</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
</tr>
<tr>
<td>(R' = 0.9R; L' = 1.0 L)</td>
<td>0.8382</td>
<td>0.2557</td>
<td>0.5</td>
<td>0.203</td>
<td>0.354</td>
<td>0.358</td>
</tr>
<tr>
<td>(R' = 1.1R; L' = 1.0 L)</td>
<td>0.559</td>
<td>0.487</td>
<td>0.65</td>
<td>0.254</td>
<td>0</td>
<td>0.703</td>
</tr>
<tr>
<td>(R' = 1.0R; L' = 0.9 L)</td>
<td>2.761</td>
<td>2.716</td>
<td>2.75</td>
<td>3.198</td>
<td>3.147</td>
<td>2.974</td>
</tr>
<tr>
<td>(R' = 1.0R; L' = 1.1 L)</td>
<td>3.25</td>
<td>2.795</td>
<td>4</td>
<td>3.238</td>
<td>3.758</td>
<td>3.522</td>
</tr>
<tr>
<td>(R' = 0.9R; L' = 0.9 L)</td>
<td>3.509</td>
<td>3.27</td>
<td>2.761</td>
<td>3.198</td>
<td>3.041</td>
<td>2.974</td>
</tr>
<tr>
<td>(R' = 1.1R; L' = 1.1 L)</td>
<td>3.25</td>
<td>2.795</td>
<td>3.5</td>
<td>3.238</td>
<td>3.487</td>
<td>3.48</td>
</tr>
</tbody>
</table>

2.4 Conclusion

This chapter has investigated several linear inner current controllers from operational principles introduction and their controller design methodologies. Firstly, the operation principle of the PI control is introduced and discussed. Furthermore, a methodology for the design and optimization of the various loops of controllers of the PI controlled VSC-HVDC transmission system is developed. This is adequately effective for a relatively strong system. However, for the weak AC system application, the inaccurate feed-forward compensation caused by low-order harmonics distortion in the case of PI control structures stands for the major disadvantage [61, 120]. In addition, the cross-coupling terms also add to these shortcomings further. The theory and the simple control design method for the PR control strategy are also introduced in this chapter. It was reported that this method has a serious frequency sensitiveness problem, which makes it hard to implement when interconnected with a weak AC grid characterized by large grid impedance.

As suggested in [54], the DB controller is the best-tailored scheme in a weak AC application in terms of robustness against parameter variation and system disturbances. Therefore, this chapter also studied four different types of DB controllers by including one sample delay with the i) reducing gain and ii) Smith Predictor, two sample delays based on iii) IMC control design and iv) solving feedback transfer function. It was also found that
the two sample delays DB current controller based on IMC derived and introduced in this chapter demonstrates similar performance as the one employed by A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg in [54].

The analysis of the results showed similar step responses for both of two sample delays DB current controllers. However, simulation results indicated that solving feedback transfer function method proves to be superior to the other methods specifically during the large step response with a fast settling time and with an acceptable reactive current overshoot. In addition, it was observed that simulation results of the same method presents smaller variations under parameter sensitivity tests compared with the IMC based DB current controller. Therefore, the solving feedback TF based DB control method is chosen as the definite inner current control scheme which is utilized in the remaining chapters of this thesis.
Chapter 3: Analytical Modeling of DB Controlled VSC

In the previous chapter, the digital DB current control which is implemented in abc natural reference frame was introduced and evaluated. This control method has two major benefits: i) fast response to set point change and ii) limiting the current magnitudes during ac faults, which offers better sinusoidal signals tracking capability compared with the conventional PI control and PR control. Until now, however, no small signal model for this type of DB controlled VSC has been reported in the literature. A major difficulty withholds the establishment of the small signal model for such DB controlled VSC is because it contains non-linear time invariant (non-LTI) and time varying components. Hence, conventional linear control design theory cannot be applied to it directly. Moreover, it is a digital controller, which makes it more complicated to develop the small signal model.

Therefore, to understand and implement this control scheme, it is necessary to develop a LTI model (small signal model) for the DB controlled VSC. In this chapter, Padé Approximation is used first to transform the model from discrete domain to continuous domain. Then, a methodology for model transforming from the αβ reference frame to dq
synchronous reference frame was proposed as an extension to the Charles Sao’s and Peter W Lehn’s works in [78-80].

This newly proposed reference frame transformation approach, which facilitates the understanding the DB controlled VSC, is one of the original contributions of this thesis. The study aims at developing a detailed higher order small signal model for the discrete DB current controlled VSC, which can facilitate further linear controller design, system parameterizations when implementing such type of VSC based applications, and establishing the foundation for the system small-signal stability analysis that Modal analysis (e.g. Eigen values, mode shapes, participation factor, etc.).

3.1 Diagram of DB model

The system structure of the proposed benchmark small signal model is given by Figure 3-1. Firstly, the input current references $\Delta I_{cd,\text{ref}}^C$ and $\Delta I_{cq,\text{ref}}^C$ for the inner current controller are pre-set based on the specified active power $Q$ and reactive power $P$, where $I_c$ stands for converter output current, the superscript $C$ represents the converter frame, the subscript $dq$ implies the variable is in the $dq$ synchronous reference frame, the subscript $RI$ denotes ‘Real-Imaginary’, and the subscript ref indicates it is a reference value. Note that the similar format is used in the rest of the thesis. Then the input current references are compensated with a two sample period ahead values, followed by a sampling block to obtain the discrete form of the input current references $\Delta I_{cd,\text{ref}}^C(k)'$ and $\Delta I_{cq,\text{ref}}^C(k)'$. In the meantime, the measured converter output currents pass through a ZOH block and feedback gain $G_f(s)$, which arrive at $\Delta I_{cd,d}^C(k)'$ and $\Delta I_{cq,q}^C(k)'$ respectively.

Based on the reference values and measured values of the input currents, the current errors $\Delta I_{cd,e}^C(k)$ and $\Delta I_{cq,e}^C(k)$ as inputs to the discrete DB controller are generated. Using these current errors, the voltage drop across the controlled plant can be predicted by the DB control algorithm, including $\Delta V_{cd,\text{ref}1}^C(k)$ and $\Delta V_{cq,\text{ref}1}^C(k)$. Moreover, the filter bus voltage should also be accessed and compensated by a 1.5 sample period ahead values. Then the second part of the converter input voltage references $\Delta V_{cd,\text{ref}2}^C(k)$ and $\Delta V_{cq,\text{ref}2}^C(k)$ are obtained. Finally, the converter input references $\Delta V_{cd,\text{ref}}^C(k)'$, $\Delta V_{cq,\text{ref}}^C(k)'$ can be generated by computing the summation of $\Delta V_{cd,\text{ref}1}^C(k)$, $\Delta V_{cd,\text{ref}2}^C(k)$ and $\Delta V_{cq,\text{ref}1}^C(k)$, $\Delta V_{cq,\text{ref}2}^C(k)$ respectively.
Figure 3-1 Small signal model of VSC with the discrete DB current controller

The computation delay needs to be taken into account as well which is approximately one sample period ($\varepsilon^{-1}$). Before conducting the calculation in grid reference frame, the VSC input references ($\Delta V_{cd, \text{ref}}(k)$, $\Delta V_{cq, \text{ref}}(k)$) in the converter reference frame should be transformed into the grid reference frame, ‘dq to RI block’, as shown in Figure 3-1. Similarly, the grid output current and voltage should also be back transformed from the grid frame to the converter frame, ‘RI to dq block’, before conducting the converter frame calculation.

By ignoring the dynamics of the DC voltage, the VSC is supposed to be ideal. This means that the VSC ideally outputs voltage as required. Utilizing this voltage, the converter reactance and the filter bus voltage, the converter output current can be easily obtained.

3.2 Characterizing the Components of VSC Small Signal Model
The procedure on how to develop the small signal model for each individual component needs to be carefully addressed. Therefore, the block diagram and its corresponding non-linear equations are established first, which is followed by a linearization process to obtain the small signal model and the small signal state-space equations. Finally, simulation results based upon tests setting on both of Simulink/Matlab and PSCAD platforms are utilized to assess the accuracy of the linearized models. The following sub-sections of this thesis will provide the details of these studies. It should be clarified that in the remainder of the thesis the large signal model can also be termed as non-linear model which is detailed model transient simulation (PSCAD). Similarly, the small signal model can also be named as linear model which is simplified s-domain simulation (Matlab).

### 3.2.1 Phase Locked Loop

The successful implementation of DB current control for a VSC highly depends on the accuracy of the performance of a PLL which can extract the phase of the filter bus voltage and system operating frequency, specifically in the case of the digital DB controlled VSC integrating with a weak AC grid. A good PLL requires four desirable characteristics: i) fast response speed, ii) no steady state error, iii) broad frequency acquisition range and iv) high noise rejection capability. A fundamental review and assessment of research on the d-q-z type PLL are given in reference [52, 56, 57] and which is currently used worldwide. This section includes discussions concerning the operational principle of such type of PLL, the derivation of a linearized model for the PLL and model verification based on PSCAD simulation. Furthermore, the PLL dynamic performance for several disturbance scenarios will also be examined and discussed.

As shown in Figure 3-2, the three-phase PLL is composed of three parts: i) phase detector; ii) PI filter and iii) voltage controlled oscillator (VCO). In PLL, The phase detector compares the phase difference between the grid phase voltages in the $\alpha\beta$ reference frame ($u_{sa}, u_{sb}$ in per unit) and the outputs of VCO ($u_{va}$ and $u_{vb}$) to calculate the error $\xi_d$. This is then passing through a filter outputs $u_f$ followed by a magnification by a gain $K_v$ and outputs the frequency difference $\Delta \omega$. The output frequency is the summation of the central frequency $\omega_0$ and $\Delta \omega$. The output phase angle $\theta$ is obtained by the integration of frequency $\omega$ [52]. In the meantime, the phase angle $\theta$ is utilized by the two functional
blocks \sin() \text{ and } \cos() \text{ of the VCO block, which are magnified by a gain } K_L, \text{ then output } u_{\alpha}, u_{\beta}. \text{ Finally the close loop PLL is formed.}

Using the arrangement in Figure 3-2, the output of the phase detector } \xi_{sd} \text{ can be easily derived as,

\begin{align*}
\xi_d &= u_{\alpha} \cdot u_{\alpha} + u_{\beta} \cdot u_{\beta} \\
&= u_{sp} \sin(\omega t + \varphi_1) \cdot K_L \cdot \cos \theta - u_{sp} \cos(\omega t + \varphi_1) \cdot K_L \cdot \sin \theta
\end{align*}

(3-1)

Since the PLL is assumed to be locked to its input signal, then the output of PLL } \theta \text{ can be given by,

\begin{align*}
\theta &= \omega t + \varphi_2
\end{align*}

(3-2)

Substituting equation (3-2) into equation (3-1) yields,

\begin{align*}
\xi_d &= u_{sp} \sin(\omega t + \varphi_1) \cdot K_L \cdot \cos(\omega t + \varphi_2) - u_{sp} \cos(\omega t + \varphi_1) \cdot K_L \cdot \sin(\omega t + \varphi_2) \\
&= u_{sp} \cdot K_L \sin[\omega t + (\varphi_1 - \varphi_2)]
\end{align*}

(3-3)

Since, } \omega_c = \omega_1, \text{ the above equation can be expanded as

\begin{align*}
\xi_d &= u_{sp} \cdot K_L \sin[\omega c t + (\varphi_1 - \varphi_2)] \\
&= u_{sp} \cdot K_L (\sin \omega c t \cos(\varphi_1 - \varphi_2) + \cos \omega c t \sin(\varphi_1 - \varphi_2))
\end{align*}

(3-4)

Note that if the } \omega_c \text{ is small enough, then } \sin \omega_c t \approx \omega_c t \text{ and } \cos \omega_c t \approx 1. \text{ However, this is not strictly true since the grid frequency is a time dependent term. Therefore, it is worth noting that under some condition, small variation in grid frequency may results in large phase difference. Hence,
3.2 CHARACTERIZING THE COMPONENTS OF VSC SMALL SIGNAL MODEL

\[ \xi_d = u_{sp} \cdot K_L (\omega_1 t \cos(\varphi_1 - \varphi_2) + \sin(\varphi_1 - \varphi_2)) \]  
(3-5)

Assuming the variations in grid frequency and initial phase angle is small enough, which means \( \omega_1 = \omega_2 \) and \( \varphi_1 = \varphi_2 \).

\[ \xi_d = u_{sp} \cdot K_L \sin(\varphi_1 - \varphi_2) \]
\[ = u_{sp} \cdot K_L (\varphi_1 - \varphi_2) \]  
(3-6)

Therefore, the double frequency components \( 2\omega_1 t \) are fully eliminated by this arrangement. However, under unbalanced conditions, phase can be locked to the positive sequence component of its input signal.

3.2.1.1 Derivation of Linearized Model of PLL

Linearized model of the PLL will be derived in this sub-section considering dynamic of each individual component of PLL independently.

For facilitating the analysis, the nominal system frequency \( \omega_0 \) of the VCO which is assumed to be constant is involved linking the input phase angle \( \theta_1 \) and the output phase \( \theta_2 \). Using Figure 3-2, the input \( \alpha\beta \) reference frame voltages to PLL block can be given by

\[
\begin{bmatrix}
  u_{sa} \\
  u_{sb}
\end{bmatrix} = u_{sp} \begin{bmatrix}
  \sin(\omega_0 t + \theta_1) \\
  -\cos(\omega_0 t + \theta_1)
\end{bmatrix}
\]  
(3-7)

The outputs of VCO in \( \alpha\beta \) reference frame ( \( u_{va} \) and \( u_{vb} \) ), can be obtained by

\[
\begin{bmatrix}
  u_{va} \\
  u_{vb}
\end{bmatrix} = K_L \begin{bmatrix}
  \cos(\omega_0 t + \theta_2) \\
  \sin(\omega_0 t + \theta_2)
\end{bmatrix}
\]  
(3-8)

In which, the phase angle \( \theta_1 \) and \( \theta_2 \) can be given by

\[ \theta_1 = \omega_1 (t) t + \varphi_1(t) - \omega_0 t \]  
(3-9)

\[ \theta_2 = \theta(t) - \omega_0 t \]  
(3-10)

A. Phase Detector

Note that using equation (3-9), one can derive that \( \varphi_1(t) = \theta_1 + \omega_0 t - \omega_1(t) \). If \( \omega_2 = \omega_1 \), using equation (3-2) and (3-10), \( \varphi_2(t) = \theta_2 + \omega_0 t - \omega_1 t \) can be obtained. If \( \varphi_1(t) \) and \( \varphi_2(t) \) are substituted into equation (3-6), the controlled error can be obtained as

\[
\xi_d = u_{sp} \cdot K_L (\omega_1 t \cos(\varphi_1 - \varphi_2)) 
\]
\[
= u_{sp} \cdot K_L \sin(\omega_0 t + \theta_1) - (\omega_0 t + \theta_2 - \omega_1 t)) 
\]
\[
= u_{sp} \cdot K_L (\theta_1 - \theta_2) \]  
(3-11)
CHAPTER 3: ANALYTICAL MODELING OF DB CONTROLLED VSC

Assuming the PLL is initially locked, by definition, the phase error \( (\theta_1 - \theta_2) \) is approximately zero,

\[
\xi_d = u_{sp} \cdot K_i (\theta_1 - \theta_2) \tag{3-12}
\]

Therefore, the linearized model for phase detector becomes

\[
\Delta \xi_d / \Delta (\theta_1 - \theta_2) = u_{sp} \cdot K_i = K_d \tag{3-13}
\]

B. First Order Low Pass PI Filter

Using the first order low pass PI filter definition

\[
\frac{u_f(s)}{\xi_d(s)} = K_{p_{-PLL}} + \frac{K_{i_{-PLL}}}{s} \tag{3-14}
\]

the linearized filter output can be given by

\[
\Delta u_f = (K_{p_{-PLL}} + \frac{K_{i_{-PLL}}}{s}) \Delta \xi_d \tag{3-15}
\]

C. Voltage Controlled Oscillator

The output angle of the VCO can be given by

\[
\theta(t) = \int_{-\infty}^{t} [\omega_0 + \Delta \omega] d\gamma = \omega_f t + \int_{-\infty}^{t} K_{V_{-PLL}} u_f(\gamma) d\gamma \tag{3-16}
\]

\[
\theta_2(t) = \theta(t) - \omega_f t \Rightarrow \theta_2(t) = \int_{-\infty}^{t} K_{V_{-PLL}} u_f(\gamma) d\gamma \tag{3-17}
\]

\[
\frac{\theta_2(s)}{u_f(s)} = \frac{K_{v_{-PLL}}}{s} \tag{3-18}
\]

Hence, the linearized phase angle can be written as

\[
\Delta \theta_2 = \frac{K_{v_{-PLL}}}{s} \Delta u_f \tag{3-19}
\]

D. Formulation of Linearized State-Space Model of PLL under Balanced Condition

Since,

\[
\xi_d = u_{sa} \cos \theta + u_{sb} \sin \theta
\]

\[
= (\frac{2}{3} u_{sa} - \frac{1}{3} u_{sb} - \frac{1}{3} u_{sc}) \cos \theta + (\frac{\sqrt{3}}{3} u_{sb} - \frac{\sqrt{3}}{3} u_{sc}) \sin \theta \tag{3-20}
\]

\[
= \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2}{3} \pi) & \cos(\theta + \frac{2}{3} \pi) \end{bmatrix} \begin{bmatrix} u_{sa} \\ u_{sb} \\ u_{sc} \end{bmatrix}
\]
This means \( \xi_d = u_{sd} \)

Therefore, \( \xi_d = u_{sp} \cdot K_L (\theta_1 - \theta_2) \)  \hspace{1cm} (3-21)

since \( \theta_1^0 = \theta_2^0 \) at nominal operating point A, the linearized error becomes

\[ \Delta \xi_d = \Delta u_{sd} = u_{sp} \cdot K_L (\Delta \theta_1 - \Delta \theta_2) \]  \hspace{1cm} (3-22)

where, the subscript 0 stands for nominal operating point.

Therefore, the PLL model given in Figure 3-2 can be simplified as the model presented in Figure 3-3, which forms the basis for deriving the small signal of PLL.

\[ \frac{d}{dt} \begin{bmatrix} l \\ \theta_2 \end{bmatrix} = \begin{bmatrix} K_{i_PPLL} \\ K_v K_{p_PPLL} \end{bmatrix} u_{sd} + \begin{bmatrix} 0 \\ K_v \end{bmatrix} l + \begin{bmatrix} 0 \\ \omega_0 \end{bmatrix} \]  \hspace{1cm} (3-23)

and,

\[ \omega = \omega_0 + K_v K_{p_PPLL} u_{sd} + K_j l \]  \hspace{1cm} (3-24)

When the above state space equations are linearized, the small signal model for PLL can be obtained as,

\[ \frac{d}{dt} \begin{bmatrix} \Delta l \\ \Delta \theta_2 \end{bmatrix} = \begin{bmatrix} K_{i_PPLL} \\ K_v K_{p_PPLL} \end{bmatrix} \Delta u_{sd} + \begin{bmatrix} 0 \\ K_v \end{bmatrix} \Delta l \]  \hspace{1cm} (3-25)

### 3.2.1.2 Analysis of linearized PLL model

In order to develop a PLL controller, it is necessary to obtain the transfer function of \( \Delta \theta_2(s)/\Delta \theta_1(s) \), where \( \Delta \theta_2(s) \) denotes the output of PLL and \( \Delta \theta_1(s) \) represents the input to the PLL control block. The block diagram of the linearized model of the PLL is illustrated below,
The open and closed loop transfer functions of the model can be given by

\[ \frac{\Delta \theta_2(s)}{\Delta \theta_1(s)}_{\text{open-loop}} = K_d \cdot \left( K_{p_{-PLL}} + \frac{K_{i_{PLL}}}{s} \right) \cdot \frac{K_v}{s} \]  

(3-26)

\[ \frac{\Delta \theta_2(s)}{\Delta \theta_1(s)}_{\text{close-loop}} = \frac{K_d K_v \left( K_{i_{PLL}} + K_{p_{PLL}} s \right)}{s^2 + K_d K_v K_{p_{PLL}} s + K_d K_v K_{i_{PLL}}} \]  

(3-27)

\[ \frac{\Delta \theta_2(s)}{\Delta \theta_1(s)}_{\text{close-loop}} = \frac{2 \xi \omega_n s + \omega_n^2}{s^2 + 2 \xi \omega_n s + \omega_n^2} \]  

(3-28)

\[ \omega_n = \sqrt{K_d K_v K_{i_{PLL}}} \]  

(3-29)

and the lock in range for PLL is [128]

\[ \Delta \omega_n = 2 \xi \omega_n = K_d K_v K_{p_{PLL}} \]  

(3-30)

3.2.1.3 Parameter Design Procedure

The systematic design procedure for PLL is well documented in [52]. Therefore, this sub-section aims to review the PLL controller design process briefly.

A. Determination of \( \omega_n \)

The lock in range is first determined by the application requirement. Using the pre-set damping ratio \( \xi \), the nature frequency \( \omega_n \) can be determined first.

\[ \omega_n = \Delta \omega_n / 2 \xi \]  

(3-30)

B. Determination of VCO Gain \( K_v_{PLL} \)

The gain \( K_v_{PLL} \) can be given by

\[ K_v = S_{\text{Margin}} \left( \omega_{\text{max}} - \omega_{\text{min}} \right) / (u_{f_{\text{max}}} - u_{f_{\text{min}}}) \]  

(3-31)

where, \( S_{\text{Margin}} \) is the stability margin, \( \omega_{\text{max}} \) and \( \omega_{\text{min}} \) are the maximum and minimum frequency that the PLL can lock to. In practice, the VCO control signal is usually limited to a range smaller than the VCO supply voltage, which is mostly +5kV [52]. For example, the
values of $u_{\text{max}}$ and $u_{\text{min}}$, with +5kV supply voltage, can be chosen as 90%·5kV and 10%·5kV respectively.

C. Let $K_d = 1$, then Determine $K_{p,PLL}$ and Finally Determine $K_{i,PLL}$

It should be noted that the lock-in range and speed response to step change of PLL is proportional to the characteristic frequency, but inversely proportional to the capability of harmonics rejection. Decision on the value of $\omega_n$ has to be made by trading off the response speed and noise rejection capability of PLL according to the requirements of applications.

3.2.1.4 Case study

Using the PLL parameters shown in Table 3-1, the transfer function of PLL can be defined as equation (3-32).

$$\frac{\theta(s)}{\theta(s)_{\text{close-loop}}} = \frac{K_d K_v (K_{i,PLL} + K_{p,PLL} s)}{s^2 + K_d K_v K_{p,PLL} s + K_d K_v K_{i,PLL}}$$

$$= \frac{2351.9s + 4.509 \cdot 10^5}{s^2 + 2351.9s + 4.509 \cdot 10^5}$$

Table 3-1 PLL parameters

<table>
<thead>
<tr>
<th>Rated Line voltage (RMS)</th>
<th>$U_{s,\text{line_rated}}$</th>
<th>62.5kV</th>
<th>PI Parameter</th>
<th>$K_{p,PLL}$</th>
<th>0.163</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Voltage Peak value</td>
<td>$U_{s,\text{phase_peak}}$</td>
<td>51.031 kV</td>
<td>PI Parameter</td>
<td>$K_{i,PLL}$</td>
<td>31.25</td>
</tr>
<tr>
<td>VCO Functional Block Gain</td>
<td>$K_L$</td>
<td>1</td>
<td>Nature Frequency</td>
<td>$\omega_n$</td>
<td>213.74\pi</td>
</tr>
<tr>
<td>Equivalent Gain Phase Detector</td>
<td>$K_d$</td>
<td>51.031</td>
<td>Damping Ratio</td>
<td>$\zeta$</td>
<td>1.751</td>
</tr>
<tr>
<td>VCO Gain</td>
<td>$K_V$</td>
<td>90\pi</td>
<td>Lock in Range</td>
<td>$\Delta \omega_L$</td>
<td>748.61\pi</td>
</tr>
</tbody>
</table>

Figure 3-5 shows the frequency response of the PLL, where the gain margin is infinite and the phase margin is 84.5°. This indicates that the designed PLL is stable.
3.2.1.5 Verification by PSCAD simulation

To compare the performances of the linear and non-linear PLL model developed, two step change tests on the phase of the source voltage $U_{sa}$ are employed using PSCAD. These tests are summarized below.

A. 1% (3.6°) Step Change in Phase

This simulation is performed by setting a fixed frequency of 50Hz for the reference voltage and introducing a 1% step in phase on the phase angle which is 3.6°. The output of the PLL is a saw-tooth waveform as shown in Figure 3-9. To isolate the perturbation in the measured phase angle, the angular rotation of the input signal, a constant periodic angle $\omega_0 t$ is subtracted from measured phase angle as shown in Figure 3-6 (solid blue curve). The results of 1% step phase change of PLL in PSCAD shows a good agreement with the linearized model in MATLAB (dotted red curve), which successfully verify the accuracy of the small signal model. The specific characteristic values of the linearized model are summarized in Table 3-2.

Figure 3-5 Frequency response of PLL in the case study

![Figure 3-5 Frequency response of PLL in the case study](image)

Figure 3-6 Linearized model verification, 1% step change in phase
Table 3-2 Characteristics of the linearized model

<table>
<thead>
<tr>
<th>Rise Time</th>
<th>Settling Time:</th>
<th>Settling Min</th>
<th>Settling Max:</th>
<th>Over Shoot</th>
<th>Under Shoot</th>
<th>Peak</th>
<th>Peak Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00094</td>
<td>0.0081</td>
<td>0.9553</td>
<td>1.059</td>
<td>5.925</td>
<td>0</td>
<td>1.059</td>
<td>0.0025</td>
</tr>
</tbody>
</table>

B. 50% (180°) Step Change in Phase

The conditions of the simulation study here are the same as in the previous text except the size of the phase step change, 50%. The results presented in Figure 3-7 shows an obvious difference at the initial step change stage in comparison with Figure 3-6.

![Figure 3-7 50% step (180°) change in phase](image)

The settling time in PSCAD is 9.9ms which is a little bit longer than the Matlab result of 8.1ms. Hence, it can be easily concluded that the linear model is developed based on a small signal and therefore 50% change cannot be considered as a small signal. However, it is important to note that after about 20ms there is an exact match between two simulation studies. This means that the PLL has a good tracking ability even though it experiences a large phase perturbation.

C. 1% Step Change in Frequency

This test is performed by setting a fixed zero initial phase and a constant magnitude for the reference voltage. Then a 1% step change in frequency (0.5Hz) is applied to the 50Hz at t=5s which lasts for 0.02s. As shown in Figure 3-8, the settling time for the 1% step change in frequency is 8ms.
Figure 3-8 1% step change in frequency simulated in PSCAD

**D. 90% step change in Magnitude**

In this test, a constant frequency of 50Hz and a zero initial phase angle and a sudden 90% step change for the magnitude are applied to the input reference voltage at t=5s.

Figure 3-9 PLL responses to 90% magnitude step change of input voltage simulated in PSCAD

Figure 3-10 PLL output phase angle in comparison with input phase angle when being subject to a sudden 90% magnitude step change of input voltage simulated in PSCAD
3.2. Characterizing the Components of VSC Small Signal Model

Figure 3-11 PLL output frequency in comparison with input frequency when being subject to a sudden 90% magnitude step change of input voltage simulated in PSCAD.

The results given in Figure 3-9 to Figure 3-11 show that the sudden magnitude reduction has no effect on the PLL outputs.

E. Single Phase to Ground Fault

In this simulation study, while the initial phase is zero at a constant frequency of 50Hz and at a constant magnitude, a ground fault is created at A-phase at t=1s.

Figure 3-12 shows the phase response of PLL under a phase to ground fault. As is shown in the figure, the result of twice the fundamental frequency, which can be expressed below,

\[ y = -0.00346\cos(200\pi t) \]  

(3-33)

Figure 3-12 PLL output phase angle when being subject to an A-phase to ground fault simulated in PSCAD.

Figure 3-13 shows the frequency response of PLL under the same fault, which can be expressed by,
$y = -50.3475 \cos(200\pi t)$  \hfill (3-34)

Figure 3-13 PLL output frequency when being subject to an A-phase to ground fault simulated in PSCAD

### 3.2.1.6 Summary of PLL

The developed linearized model and non-linear model of PLL both have the fast response and wide frequency range acquisition abilities. In addition, the linear model and non-linear model match each other very well. Its performance for a large reduction in voltage magnitude and for a single phase to ground fault are also examined in this section.

### 3.2.2 Frame Transformation

As shown in section 3.1, the small signal model requires calculations both in the grid frame and converter frame. Therefore, the variables in the model need to be freely transformed between these frames. In this sub-section, the small signal model for the required frame transformation will be developed in terms of the VSC input voltage reference $V_{c,ref}$, the converter output current $I_c$ and the filter bus voltage $U_f$. The equations (3-35) to (3-37) indicate the relationship between the grid RI reference frame and the converter reference frame, as illustrated in Figure 3-1. The figure below is also given to graphically demonstrate this relationship.

\[
V_{eRI,ref}^e(k) = e^{j(\theta_{rel} + \pi/2)} V_{edq,ref}^c(k) \\
I_{cdq}^e = e^{-j(\theta_{rel} + \pi/2)} I_{eRI}^g \\
u_{fdq}^e = e^{-j(\theta_{rel} + \pi/2)} u_{fRI}^g
\]  \hfill (3-35)

\hfill (3-36)

\hfill (3-37)
3.2. CHARACTERIZING THE COMPONENTS OF VSC SMALL SIGNAL MODEL

Figure 3-14 Relationship between converter reference frame and grid RI reference frame

3.2.2.1 Mathematical Equation of VSC Input Voltage Reference

If we expand equation (3-35), equation (3-38) can be obtained which then can be utilized for linearization.

\[ V_{cR,ref}^g (k) = -\sin \theta_{PLL} \cdot V_{cd,ref}^c (k) \cdot \cos \theta_{PLL} \cdot V_{eq,ref}^c (k) \]  
\[ V_{cl,ref}^g (k) = \cos \theta_{PLL} \cdot V_{cd,ref}^c (k) - \sin \theta_{PLL} \cdot V_{eq,ref}^c (k) \]  

(3-38)

The phase angle \( \theta_{PLL} \) in the above set of equation is the phase difference between the filter bus voltage and grid phase reference point, which is a constant value by excluding the time varying component \( \omega_0 t \).

The linearized form of equation (3-38) can be given as

\[ \Delta V_{cR,ref}^g (k) = -\sin \theta_{PLL0} \cdot \Delta V_{cd,ref}^c (k) \cdot \cos \theta_{PLL0} \cdot \Delta V_{eq,ref}^c (k) - \Delta V_{cl,ref}^g (k) \cdot \Delta \theta_{PLL} \]  
\[ \Delta V_{cl,ref}^g (k) = \cos \theta_{PLL0} \cdot \Delta V_{cd,ref}^c (k) - \sin \theta_{PLL0} \cdot \Delta V_{eq,ref}^c (k) + \Delta V_{cl,ref}^g (k) \cdot \Delta \theta_{PLL} \]  

(3-39)

3.2.2.2 Verification of the Large Signal Mathematical Equation

To verify the frame transformation, the test model that a controlled three-phase voltage source with an inductance in series is used as shown in Figure 3-15. The main objective of this approach is to measure the filter bus voltage \( U_s \) in real-imaginary (RI) reference frame (i.e. the grid frame). Therefore, the tests involved three steps: i) directly measuring \( U_s \) by locking the phase of the grid reference point voltage \( U_G \) by PLL, and obtaining \( \theta_G \) to calculate \( U_{sR,m}^G, U_{sI,m}^G \); ii) measuring the phase \( \theta \) of the filter bus voltage \( U_s \), and the phase difference \( \theta_{PLL} \) between the grid source voltage and the filter bus voltage. Note that using the angle \( \theta \), the representation of \( U_s \) in the converter reference frame \( (U_{sd,m}^C, U_{sq,m}^C) \) can be
computed, which is then followed by a transformation to grid frame using equation (3-35). This calculation utilizes $\theta_{PLL}$ to obtain $U_{sR,\text{cal}}^G$ and $U_{sL,\text{cal}}^G$. And iii) comparing the results obtained in the previous two steps.

\[
U_G \angle \theta \quad L_G \quad U_s \angle \theta
\]

Figure 3-15 Controlled voltage source representation with an inductance

The final results are compared and shown in Figure 3-16, which successfully verify the accuracy of the mathematical formula of the frame transformation.

![Figure 3-16 Test results for grid RI reference frame transformation](image)

### 3.2.2.3 Testing for the Small Signal Mathematical Equation

In this section, only the steady state value is considered since the equations adopted to describe the relationship of the frame transformation are two algebraic equations. Therefore, the transient process can be ignored.

During the testing process a 1.0 pu large signal $u_{sq0}^c$ is first applied as an input which varied at $t=0.5s$ on q-axis of the filter bus voltage. This is followed by a secondary 0.99 pu large signal $u_{sq0}^c$ that varied at $t=0.5s$ imposed in another simulation before transforming to the grid RI reference frame. The errors in the output quantities of both simulations are given by $\Delta u_{sR,\text{Large}}^G$ and $\Delta u_{sL,\text{Large}}^G$. In addition, a 0.01pu small step change on q-axis of the filter bus voltage is applied simultaneously to the small signal model at $t=0.5s$. Then the outputs $\Delta u_{sR,\text{small}}^G$ and $\Delta u_{sL,\text{small}}^G$ are compared with the results obtained from the non-linear model (see Figure 3-17).
3.2. Characterizing the Components of VSC Small Signal Model

The simulation results are given in Figure 3-18. Note that the exponentially slow rising trend in the figure is actually caused by the combination of the voltage ramp up time which is set as 0.02s in this test and the dynamics introduced by PLL utilized in the transformation process of voltage from dq frame to RI frame. These results successfully confirm the accuracy of the developed small signal model for the grid frame transformation.

The large signal and the small signal algebraic equations for converter terminal current $I_c$ transforming from the grid RI reference frame to the converter dq reference frame are given in equations (3-40) and (3-41).

\[
I_{cd}^e = -\sin \theta_{PLL} \cdot I_c^e + \cos \theta_{PLL} \cdot I_{cl}^e \\
I_{cq}^e = -\cos \theta_{PLL} \cdot I_c^e - \sin \theta_{PLL} \cdot I_{cl}^e
\] (3-40)
\[ \Delta I_{cd}^C = -\sin \theta_{PLL} \cdot \Delta I_{cd}^C + \cos \theta_{PLL} \cdot \Delta I_{cq}^C + \Delta I_{cd0}^C \Delta \theta_{PLL} \]  
\[ \Delta I_{cq}^C = -\cos \theta_{PLL} \cdot \Delta I_{cr}^C - \sin \theta_{PLL} \cdot \Delta I_{cl}^C - \Delta I_{cd0}^C \Delta \theta_{PLL} \]  
(3-41)

Note that this transformation is similar to the VSC input voltage reference, which is simply an opposite transforming direction. Therefore, no verification studies are needed.

The large signal and the small signal models for the filter bus voltage \( u_f^C \) transforming from grid RI reference frame to converter dq reference frame can be given by

\[ u_{fd}^C = -\sin \theta_{PLL} \cdot u_{fr}^e + \cos \theta_{PLL} \cdot u_{f}^e \]  
\[ u_{fq}^C = -\cos \theta_{PLL} \cdot u_{fr}^e - \sin \theta_{PLL} \cdot u_{f}^e \]  
(3-42)

\[ \Delta u_{fd}^C = -\sin \theta_{PLL} \cdot \Delta u_{fr}^e + \cos \theta_{PLL} \cdot \Delta u_{f}^e + u_{f0}\Delta \theta_{PLL} \]  
\[ \Delta u_{fq}^C = -\cos \theta_{PLL} \cdot \Delta u_{fr}^e - \sin \theta_{PLL} \cdot \Delta u_{f}^e - \Delta u_{f0}\Delta \theta_{PLL} \]  
(3-43)

### 3.2.3 Grid Voltage Signal Filter

The transfer function for voltage signal filter \( G_{Filter}(s) \) is represented by,

\[ G_{Filter}(s) = \frac{\Delta u_{fd}^e}{\Delta u_{fd}^e + \Delta u_{fq}^e} = \frac{1}{1 + T_f s} \]  
(3-44)

The state-space equations can be established as in equation (3-45) and (3-46).

\[ \frac{du_{fd}^e}{dt} = -\frac{1}{T_f} u_{fd}^e + \frac{u_{fd}^e}{T_f} \]  
(3-45)

\[ \frac{du_{fq}^e}{dt} = -\frac{1}{T_f} u_{fq}^e + \frac{u_{fq}^e}{T_f} \]  
(3-46)

After linearizing, the small-signal state-space model for the grid voltage signal filter can be given by,

\[ \frac{d\Delta u_{fd}^e}{dt} = -\frac{1}{T_f} \Delta u_{fd}^e + \frac{\Delta u_{fd}^e}{T_f} \]  
(3-47)

\[ \frac{d\Delta u_{fq}^e}{dt} = -\frac{1}{T_f} \Delta u_{fq}^e + \frac{\Delta u_{fq}^e}{T_f} \]  
(3-48)

Note that there is no need to compare the large signal model and the small signal model with respect to this component, since they do have the same formula. The only difference is the step size to the input signals, which will naturally output proportionally results.
3.2.4 Reference Current Phase Compensation and Voltage Prediction Block

The current compensation equation and inverse transformation of the compensated current reference back to the converter dq reference frame are given in equation (3-49) and equation (3-50) respectively.

\[
\begin{bmatrix}
I_{c_{\text{dref}}}^c \\
I_{c_{\text{qref}}}^c
\end{bmatrix} =
\begin{bmatrix}
\cos(\theta_{\text{PLL}} + 2\omega_0 T_s) & -\sin(\theta_{\text{PLL}} + 2\omega_0 T_s) \\
\sin(\theta_{\text{PLL}} + 2\omega_0 T_s) & \cos(\theta_{\text{PLL}} + 2\omega_0 T_s)
\end{bmatrix}
\begin{bmatrix}
I_{c_{\text{dref}}}^c \\
I_{c_{\text{qref}}}^c
\end{bmatrix}
\]  
(3-49)

\[
\begin{bmatrix}
I_{c_{\text{dref}}}^c \\
I_{c_{\text{qref}}}^c
\end{bmatrix} =
\begin{bmatrix}
\cos \theta_{\text{PLL}} & \sin \theta_{\text{PLL}} \\
-\sin \theta_{\text{PLL}} & \cos \theta_{\text{PLL}}
\end{bmatrix}
\begin{bmatrix}
I_{c_{\text{dref}}}^c \\
I_{c_{\text{qref}}}^c
\end{bmatrix}
\]  
(3-50)

If we substitute equation (3-49) into equation (3-50), the transformation relationship between the compensated current and the original current in the converter dq reference frame can be obtained,

\[
\begin{align*}
I_{c_{\text{dref}}}^c &= \cos(2\omega_0 T_s) \cdot I_{c_{\text{dref}}}^c - \sin(2\omega_0 T_s) \cdot I_{c_{\text{qref}}}^c \\
I_{c_{\text{qref}}}^c &= \sin(2\omega_0 T_s) \cdot I_{c_{\text{dref}}}^c + \cos(2\omega_0 T_s) \cdot I_{c_{\text{qref}}}^c
\end{align*}
\]  
(3-51)

The below set of equation denotes the linearized form of the above equations,

\[
\begin{align*}
\Delta I_{c_{\text{dref}}}^c &= \cos(2\omega_0 T_s) \cdot \Delta I_{c_{\text{dref}}}^c - \sin(2\omega_0 T_s) \cdot \Delta I_{c_{\text{qref}}}^c \\
\Delta I_{c_{\text{qref}}}^c &= \sin(2\omega_0 T_s) \cdot \Delta I_{c_{\text{dref}}}^c + \cos(2\omega_0 T_s) \cdot \Delta I_{c_{\text{qref}}}^c
\end{align*}
\]  
(3-52)

To verify these equations, a 0.01pu (1pu-0.99pu) step change is applied to the inputs of both the large signal model and the small signal model, and the tests results are given in Figure 3-19, which shows a good agreement.

![Figure 3-19 Current compensation block verification](image)
For the voltage prediction block in Figure 3-1, the relationship between the input voltage \( u_{fd}^C \), \( u_{fq}^C \) and the output predicted voltages in \( \alpha \beta \) reference frame \( v_{\alpha\beta\text{ref}_2}^C \), \( v_{\alpha\beta\text{ref}_2}^C \) can be given by,

\[
\begin{bmatrix}
   v_{\alpha\text{ref}_2}^C \\
   v_{\beta\text{ref}_2}^C \\
\end{bmatrix} =
\begin{bmatrix}
   \cos(\theta_{PLL0} + 1.5\omega_0 T_s) & -\sin(\theta_{PLL0} + 1.5\omega_0 T_s) \\
   \sin(\theta_{PLL0} + 1.5\omega_0 T_s) & \cos(\theta_{PLL0} + 1.5\omega_0 T_s) \\
\end{bmatrix} \begin{bmatrix}
   u_{fd}^C \\
   u_{fq}^C \\
\end{bmatrix}
\]

(3-53)

Similarly, the back transformation from the \( \alpha \beta \) reference frame to the converter dq reference frame for the predicted voltages can be written as,

\[
\begin{bmatrix}
   v_{\alpha\text{ref}_2}^C \\
   v_{\beta\text{ref}_2}^C \\
\end{bmatrix} =
\begin{bmatrix}
   \cos(\theta_{PLL0}) & \sin(\theta_{PLL0}) \\
   -\sin(\theta_{PLL0}) & \cos(\theta_{PLL0}) \\
\end{bmatrix} \begin{bmatrix}
   v_{\alpha\text{ref}_2}^c \\
   v_{\beta\text{ref}_2}^c \\
\end{bmatrix}
\]

(3-54)

Substituting equation (3-54) into equation (3-53), the direct link between the input voltage and output predicted voltage are obtained as equation (3-55),

\[
\begin{align*}
   v_{\alpha\text{ref}_2}^c &= \cos(1.5\omega_0 T_s) \cdot u_{fd}^C - \sin(1.5\omega_0 T_s) \cdot u_{fq}^C \\
   v_{\beta\text{ref}_2}^c &= \sin(1.5\omega_0 T_s) \cdot u_{fd}^C + \cos(1.5\omega_0 T_s) \cdot u_{fq}^C
\end{align*}
\]

(3-55)

The linearized form of the set of equations is given by,

\[
\begin{align*}
   \Delta v_{\alpha\text{ref}_2}^c &= \cos(1.5\omega_0 T_s) \cdot \Delta u_{fd}^C - \sin(1.5\omega_0 T_s) \cdot \Delta u_{fq}^C \\
   \Delta v_{\beta\text{ref}_2}^c &= \sin(1.5\omega_0 T_s) \cdot \Delta u_{fd}^C + \cos(1.5\omega_0 T_s) \cdot \Delta u_{fq}^C
\end{align*}
\]

(3-56)

The verification process for the accuracy of the linearization of this component is similar to the current compensation block. Hence, it will not be repeated.

### 3.2.5 Discrete DB Current Feedback Control Block and Current Input Generation

The feedback transfer function for the discrete DB current controller yields to,

\[ G_f(s) = e^{-2(R_s/L_s)T_s} \]

(3-57)

where, \( R_s \) and \( L_s \) represent the resistance and inductance of converter reactance, \( T_s \) stands for the sampling time. The resultant large signal model and small signal model for the feedback block are

\[
\begin{align*}
   I_{cd-d}^c(k) &= G_f I_{cd-d}^c(k) \\
   I_{eq-d}^c(k) &= G_f I_{eq-d}^c(k)
\end{align*}
\]

(3-58)
3.2. CHARACTERIZING THE COMPONENTS OF VSC SMALL SIGNAL MODEL

\[ \Delta I_{cd-d}^e(k) = G_{v} \Delta I_{cd}^e(k) \]
\[ \Delta I_{cq-d}^e(k) = G_{i} \Delta I_{cq}^e(k) \]  

(3-59)

Note that, there is also no need to verify the linearization of this feedback loop since it is only a coefficient gain.

The large signal model and the small signal model for generation of the DB current input errors can be given by

\[ I_{cd-e}^e(k) = I_{cdref}^e(k) - I_{cd-d}^e(k) \]
\[ I_{cq-e}^e(k) = I_{cqref}^e(k) - I_{cq-d}^e(k) \]  

(3-60)

\[ \Delta I_{cd-e}^e(k) = \Delta I_{cdref}^e(k) - \Delta I_{cd-d}^e(k) \]
\[ \Delta I_{cq-e}^e(k) = \Delta I_{cqref}^e(k) - \Delta I_{cq-d}^e(k) \]  

(3-61)

3.2.6 Characterizing ZOH Block, Sampling Block and Inner Current Control

3.2.6.1 From Discrete to Continuous Approximation

VSCs are inherently discontinuous and they are typically equipped with digital controllers. It is therefore necessary to develop the techniques to adequately approximate the behaviour of these devices in the continuous domain within the bandwidth of interest. The bandwidth of interest for small-signal rotor-angle stability analysis of power systems is in the order of 0 to 5 Hz (31 rad/s). It is on this basis that the algebraic average responses of the VSCs are used in power system analysis applications where rotor-angle dynamics are of primary concern.

To develop the approximations of the digital controllers in the continuous domain it is necessary to investigate linear transfer function approximations of the delay (i.e. \( e^{-sT} \)).

Then equivalent continuous-time linear transfer function model for the zero order holding (ZOH) block is developed utilizing the pure delay approximation. Then the discrete time inner current controller model is converted to a continuous domain model using the same approach. Finally, the characteristic of the ZOH block together with the digital controller are investigated by its linear equivalence.
A. Pure One Sample Delay

The transfer function of the pure one-sample delay in the z-domain is $F_1(z) = z^{-1}$ and the non-rational transfer function of the delay in the s-domain is $F_1(s) = e^{-sT}$. It is necessary to develop a rational s-domain transfer-function approximation of the delay. Here, i) the first order Padé Approximation $F_1(s) = (1-sT_s/2)/(1+sT_s/2)$, ii) the third order Padé Approximation $F_3(s) = (1-sT_s/6)/(1+sT_s/6)^3$ and iii) a comparably crude approximation given by a first order lag $F_5(s) = 1/(1+sT_s)$ are investigated. The frequency responses of the delay are compared with that of the above three approximations. Furthermore, the time-responses of the exact delay and the approximations are compared for (i) a step signal; and (ii) a sinusoidal input signal.

a) Frequency Response

Figure 3-20 shows the frequency responses of the pure one sample delay in s- and z-domain and the three s-domain approximations. It can be seen from the figure, the $z^{-1}$ and $e^{-sT}$ are overlaid with each other as expected. The third order Padé approximation is the most accurate equivalence among the three approximations. However, for the power-system modeling purposes outlined in section 3.2.6.1, the first order Padé Approximation is more than adequate (where the sampling time $T_s$ equals to 1ms) since it matches the exact delay at least up to 389rad/s (62Hz), and our interested frequency range is within this limit.

![Figure 3-20 Frequency responses of pure one sample delay](image-url)
3.2. Characterizing the Components of VSC Small Signal Model

b) Step Response

The unit step responses of the one sample delay and its approximations are shown below in Figure 3-21.

![Figure 3-21 Step responses of pure one sample delay](image)

Table 3-3 Characteristics of the step response corresponding to the pure one sample delay

<table>
<thead>
<tr>
<th></th>
<th>Rise Time</th>
<th>Settling Time</th>
<th>Settling Min</th>
<th>Settling Max</th>
<th>Over Shoot</th>
<th>Under Shoot</th>
<th>Peak</th>
<th>Peak Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>$e^{-st}$</td>
<td>8T$_s$</td>
<td>9.8T$_s$</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>100 T$_s$</td>
</tr>
<tr>
<td>$z^{-1}$</td>
<td>0 T$_s$</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>T$_s$</td>
<td></td>
</tr>
<tr>
<td>Third order Padé</td>
<td>1.1T$_s$</td>
<td>1.3T$_s$</td>
<td>0.8026</td>
<td>1.0138</td>
<td>1.3755</td>
<td>100</td>
<td>1.0138</td>
<td>1.7T$_s$</td>
</tr>
<tr>
<td>First order Padé</td>
<td>1.1T$_s$</td>
<td>2 T$_s$</td>
<td>0.8057</td>
<td>1</td>
<td>0</td>
<td>100</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>First order lag</td>
<td>2.2T$_s$</td>
<td>3.9 T$_s$</td>
<td>0.9029</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>10.5 T$_s$</td>
</tr>
</tbody>
</table>

Table 3-3 presents the characteristics of the step response. As it can be observed in Figure 3-21, the one sample delay $e^{-st}$ and $z^{-1}$ performed very well as expected (exactly as one sample delay). Among the three approximation methods, the first-order lag has the longest settling time and rise time. The third order Padé Approximation and the first-order Padé Approximation have the same rise time which is 1.1T$_s$. It was found that the third order Padé Approximation has a comparably shorter settling time which is preferred. However this approximation also has a higher overshoot which is undesirable. Note that, both approximation methods have a common defect that imposes a positive zero (RHP
zero) to the system. Reflected on the unit step response performance, the plots start arising from -1. Taking all the factors into consideration, the first-order Padé Approximation is found to be the most suitable and sufficiently accurate to approximate the pure one sample delay in this study.

B. Zero Order Holding Block

a) Transfer Function of Zero Order Holding Block in S Domain

The mathematical representation of zero order holding block is

\[ e(nT_s + \Delta t) = e(nT_s), \text{ where } 0 \leq dT \leq T_s \]  

(3-62)

If we input an ideal unit impulse signal to the ZOH block, a rectangular impulse with magnitude 1 and the lasting time \( T_s \) will be obtained as shown in Figure 3-22, which can be divided into a unit step followed by a delayed negative unit step with a time constant \( T_s \). Note that, the ZOH output signal has two typical characteristics in Figure 3-22: i) contain high frequency component (single frequency input) and ii) has the fundamental frequency shifted by \( T_s/2 \).

![Figure 3-22 Demonstration of ZOH function](image)

For a better explanation, a typical sampled data system is shown below in Figure 3-23. Note that the continuous signal is sampled to be a discrete signal with a sampling time \( T_s \), which then goes through a signal processing block, and being held by a ZOH block to be transformed to a continuous signal again. It should be noted that the result of the processed signal \( y[k] \) is kept constant during each sampling time.
3.2. CHARACTERIZING THE COMPONENTS OF VSC SMALL SIGNAL MODEL

Figure 3-23 A typical sampled data system structure

The mathematical model of the processed continuous signal result \( y(t) \) can be described as in equation (3-63), and can be illustrated as in Figure 3-24.

\[
y(t) = y[k](u(t - kT_s) - u(t - (k + 1)T_s))
\]  
(3-63)

where, \( u(t) \) is a step function, which can be defined by

\[
u(t) = \begin{cases} 
0, & t < 0 \\
0.5, & t = 0 \\
1.0, & t > 0 
\end{cases}
\]  
(3-64)

Figure 3-24 Composition of a rectangular impulse

If we take the Laplace transform of equation (3-63),

\[
\mathcal{L}(y(t)) = \frac{1}{s} \left( e^{-skT_s} - e^{-s(k+1)T_s} \right) \cdot y[k] \\
= y[k] \cdot e^{-skT_s} \cdot \frac{1 - e^{-sT_s}}{s} \\
= y(T_s) \frac{1 - e^{-sT_s}}{s}
\]  
(3-65)

The transfer function of ZOH block can be obtained as

\[
G_{ZOH}(s) = \frac{1 - e^{-sT_s}}{s}
\]  
(3-66)
b) First Order Padé Approximation for Transfer Function of ZOH Block

Substituting the one sample delay first-order Padé Approximation equation into equation (3-66), the first-order Padé Approximation of ZOH can be obtained as

\[
G'_{ZOH}(s) = \frac{1 - e^{-sT_s}}{s} = \frac{1 - (1 - sT_s/2) / (1 + sT_s/2)}{s} = \frac{T_s}{1 + sT_s/2}
\]  

(3-67)

c) Frequency Response of the ZOH and its Approximation

Figure 3-25 shows the frequency response of ZOH and its first-order Padé Approximation. It can be seen in the figure that the Bode plots of the exact one and the approximate one are matched well up to 500 rad/s which is sufficient for the interested frequency range. The attenuation at 50 Hz for the exact one is -0.0358dB and -0.108dB for the approximate one. Furthermore, the phase shifts are found to be identical for both models, which is 9 degree for half of the sampling period.

![Frequency response of ZOH block and its approximation](image)

Figure 3-25 Frequency responses of ZOH block and its approximation

d) Step Response of Zero Order Holding Block and its Approximation

As given in Figure 3-26 and Table 3-4, the ZOH block and its first-order Padé Approximation are in a good agreement on the step responses. The reaction of the ZOH block being subject to a step change is almost instantaneous.
3.2. Characterizing the Components of VSC Small Signal Model

Figure 3-26 Step responses of ZOH block and its approximation

<table>
<thead>
<tr>
<th></th>
<th>Rise Time (s)</th>
<th>Settling Time (s)</th>
<th>Settling Min</th>
<th>Settling Max</th>
<th>Over Shoot</th>
<th>Under Shoot</th>
<th>Peak</th>
<th>Peak Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZOH</td>
<td>0.4605</td>
<td>0.5641</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>262.5</td>
</tr>
<tr>
<td>First order Padé</td>
<td>0.4605</td>
<td>0.5641</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0.5756</td>
</tr>
</tbody>
</table>

**e) Response to the Sinusoid Input for ZOH**

i. Verification by Matlab

According to the Bode plot of ZOH, the magnitude passing through the exact transfer function should be 99.6% of the input magnitude and 98.8% for the approximate function. The phase shift is 9 degree which is equal to half sampling time. Figure 3-27 shows the Matlab simulation results, in which the amplitudes for the exact transfer function and the first-order Padé Approximation are 98.8% and 99.6% respectively. These results match the desirable outputs in the frequency analysis.
ii. Verification by PSCAD

PSCAD simulation studies are presented in Figure 3-28. The magnitude of the signal passing through sampling block built in PSCAD is 1pu, which is ideal. The peak amplitude of the output from the exact ZOH is 99.3% of the input signal and the output from the first order Padé Approximation is 98.8% of the input signal. The output amplitudes also match well with the attenuation value observed in the frequency response analysis.

f) Comparison of the Results in Matlab and PSCAD

The combined simulation results from Matlab and PSCAD are given in Figure 3-29a, which are acceptable. However, the Matlab results are found to be more accurate since they match the predicted results well with the results obtained from the frequency response analysis. The exact ZOH simulated results in PSCAD have a 0.3% error in output.
amplitude and a period of oscillation (harmonics), which is acceptable. This conclusion was observed in Figure 3-29 (b) that is enlarged from a portion of Figure 3-29 (a).

(a) Combined simulation results

(b) Enlarged section of Figure 3-29 (a) for peak point

Figure 3-29 Comparison of the simulation results

C. Inner DB Current Controller

The algorithm of the inner current DB controller, also known as the AC current tracker, has also discussed in depth in [52], and has been applied successfully in [53, 126]. The control block diagram of the DB current control method in the z domain was given in chapter 2.
CHAPTER 3: ANALYTICAL MODELING OF DB CONTROLLED VSC

a) Transfer function of Inner Current Controller First Order Padé Approximation

Substituting the one sample delay first order Padé Approximation into equation (2-40), the transfer function of inner DB current control block based on the first order Padé Approximation can be represented as,

\[
G_{in}(s) = \frac{N_1}{(1 + N_2 \cdot (1 - sT_s/2)) / (1 + sT_s/2)} = \frac{(N_1 + N_1 \cdot T_s \cdot s / 2) / [(1 + N_2) + T_s \cdot (1 - N_2) \cdot s / 2]}{(a + b \cdot s) / (c + d \cdot s)}
\]

where,

\[
a = N_1; \quad b = N_1 \cdot \frac{T_s}{2}; \quad c = (1 + N_2); \quad d = \frac{T_s}{2} \cdot (1 - N_2)
\]

b) Frequency Response of Inner Current Controller and its Approximation

The z domain controller and its first order Padé approximation are the main focus of this sub-section. However, for the comparison purpose, the first-order lag is also included here.

As it can be observed in Figure 3-30, the first-order lag approximation performs poorly compared to the first-order Padé Approximation. Therefore, the first-order Padé Approximation can still be considered as the most appropriate method. The attenuation and phase shift for both the inner current DB controller and its first-order Padé Approximation are found to be identical at 50 Hz.
c) Step Response of Inner DB Current Control and Its Approximation

Figure 3-31 shows the step responses of the inner DB current controller and its approximation. It can be seen that the step response of Z-domain DB current controller is an oscillatory pulse train, this can be explained as follows.

Since the transfer-function of the inner DB current controller is equation (2-48), the Z transform of the unit step response is

\[
G_{db}(z) = \frac{N_1}{1+N_2 z^{-1}} \cdot \frac{z}{z-1} = \frac{N_1}{N_2} \frac{z}{(z+1/N_2)(z-1)} = N_1 z \left( \frac{A}{z+N_2} + \frac{B}{z-1} \right)
\]  

(3-69)

where,

\[
A = \left. \frac{z}{z-1} \right|_{z=-N_2}, \quad B = \left. \frac{z}{z+N_1} \right|_{z=1}
\]  

(3-70)

Hence,

\[
G_{db}(z) = N_1 A \frac{1}{1+N_2 z^{-1}} + N_1 B \frac{1}{1-z^{-1}}
\]  

(3-71)

Therefore, the unit step response of the z domain controller can be easily obtained in time domain by using inverse of equation (3-71).

In this study, by substituting the parameter listed in Appendix A, the coefficient \( N_1 \) and \( N_2 \) of the DB current controller are able to be obtained which are -24.904 and 0.9997 respectively. \( A \) and \( B \) are both 1/2. Therefore, the step response of the z domain DB current controller is,

\[
y(t) = -12.4695 - 12.4695(-0.9997) T_{s}
\]  

(3-72)

Figure 3-31 Step response of inner DB current controller and its approximation
Hence, the step response of the inner current controller should be a pulse train (high frequencies oscillation) with an exponentially reduced magnitude to which the time constant is long, as shown in Figure 3-31.

d) Response to the Sinusoid Input for Inner Current Controller together with ZOH

The aim of this section is to compare the actual discrete system with the continuous Padé Approximation model and also to examine the feasibility of replacing the discrete inner current DB controller with the continuous approximation to be utilized in power system simulation. Figure 3-32 shows the continuous and discrete implementation schemes of the inner current control strategy.

![Diagram of inner DB current controller](image)

(a) Continuous approximation of inner DB current controller

![Diagram of discrete implementation block](image)

(b) Discrete implementation block of inner current DB current controller in PSCAD

Figure 3-32 Implementation of the inner DB current controller scheme in continuous domain and in the z domain

The simulation results are given in Figure 3-33. The grey line in the figure is the sinusoidal input to the system. The red line is the result of the discrete controller implemented in PSCAD, and the green line shows the discrete controller output simulated in Matlab. The blue line is the result of the equivalent continuous Padé Approximation using Matlab. Note that the discrete controller has the same phase shift both in PSCAD and MATLAB simulations and very small error in magnitude that can be ignored. The result
also shows that the continuous Padé Approximation of the discrete DB current-controller is an accurate equivalent for the type of power-system analysis considered in this research.

Figure 3-33: Comparison of the responses of (i) the discrete DB current controller and (ii) its first order Padé Approximation to a sinusoidal input signal.

3.2.6.2 Transformation of DB Controller from αβ Reference Frame to dq Reference Frame

In the previous discussion, the discrete controller has been successfully transformed to continuous domain. However, the DB current controller considered was defined in abc natural reference frame as shown in Figure 3-34, which contains time-varying terms or sinusoidal components which are inappropriate for developing the small signal model. Therefore, it is necessary to transform the controller to dq reference frame. This will be done in four steps as will be explained below.

Figure 3-34 The abc natural reference frame DB current control block
CHAPTER 3: ANALYTICAL MODELING OF DB CONTROLLED VSC

Step 1: The model is simplified by reducing all the sampling blocks (circled area in Figure 3-34), moving to behind the computation block, and leaving the rest of the model remained unchanged, as illustrated Figure 3-35.

![Figure 3-35 The simplified abc natural reference frame DB current control block](image)

Step 2: The abc natural reference frame controller is transformed to αβ reference frame by using Clark Transformation (see equation (2-2)) as shown in Figure 3-36.

![Figure 3-36 The simplified αβ reference frame DB current control block](image)

Step 3: The αβ reference frame DB control block is modified by using inputs/outputs in dq reference frame, which is done by adding with modulator/demodulator as shown in Figure 3-37.

![Figure 3-37 Simplified dq reference frame DB current control block including the time-varying terms (modulator/de-modulator) (image)
Step 4: The modulator sectors are eliminated and transformed to dq reference frame which do not contain time varying terms (modulator/de-modulator).

Note that after these transformations, each variable in αβ reference frame going through the modulator system is transformed to dq reference frame which is a linear time invariant (LTI) system. The next step is to shift the rotary factor $e^{j\omega t}$ to the right hand through three blocks: i) DB block; ii) sampling block and iii) delay block step by step until reaching to $e^{j\omega t}$. During this process both of the terms are nullified without containing the time-varying term since $e^{j\omega t} \cdot e^{-j\omega t} = 1$. Therefore, the controller then can be transformed to dq synchronous reference frame.

A. Methodology Development for Cancelation of Modulator/De-modulator

The primary question is how to eliminate the modulator/de-modulator to achieve the equivalent linearized small-signal model system. Figure 3-38 illustrates a generic modulator/de-modulator system. The objective here is to derive the transfer function or state-space equation for $G(s) = Y_{dq}(s)/U_{dq}(s)$ of the system. It should be noted that the derivation process with respect to the elimination of the system modulator/de-modulator is one of the original contributions of this thesis. It should be emphasized that two approaches are developed from different point of views which result in the same conclusion. The first methodology accommodates the transfer matrix state-space equation, which avoids the presence of the imaginary components during the derivation process but is comparably more complicated, which will be discussed in the rest of this section. The second approach is derived from the rotary viewpoint which is also based on the state space equations. Due to the space consideration in this thesis, this approach is not included in the main text but included in Appendix B.

![Figure 3-38 Modulator/de-modulator system](image-url)
It should be noted that the transmission path between the modulator and de-modulator is represented by a linear set of time dependent state equations. Therefore, to facilitate the development of the linearized system of equation, they can be defined as

\[
\dot{z}_{dq} = A_{dq} z_{dq} + B_{dq} u_{dq}
\]

\[
y_{dq} = C_{dq} z_{dq} + D_{dq} u_{dq}
\]

where, \( z_{dq} = [z_{d1}, z_{d2}, \ldots z_{dn}, z_{q1}, z_{q2}, \ldots z_{qn}]^T \), \( u_{dq} = [u_{d1}, u_{q1}]^T \), \( y_{dq} = [y_{d1}, y_{q1}]^T \).

Then, we can define the following state-variable transformation:

\[
X_{ai} + jX_{bi} = (Z_{di} + jZ_{qi}) \cdot e^{j\theta(t)}
\]

\[
= (Z_{di} + jZ_{qi})(\cos(\theta(t)) + j \sin(\theta(t)))
\]

\[
= (Z_{di} \cos \theta - Z_{qi} \sin \theta) + j(Z_{di} \sin \theta + Z_{qi} \cos \theta)
\]

If we rewrite above equation in matrix form, we get

\[
\begin{bmatrix}
X_{ai} \\
X_{bi}
\end{bmatrix} = \begin{bmatrix}
\cos \theta & -\sin \theta \\
\sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix}
Z_{di} \\
Z_{qi}
\end{bmatrix}
\]

(3-76)

In the below paragraphs the complete set of the state variables, \( X_{ai}, X_{bi} \Leftrightarrow Z_{di}, Z_{qi} \) (i=1,...,n), developed in matrix form are given.

If we apply equation (3-76) to each \( X_{ai}, X_{bi} \Leftrightarrow Z_{di}, Z_{qi} \) pair, the following equation will be obtained

\[
\begin{bmatrix}
X_{ai} \\
X_{a2} \\
\vdots \\
X_{an} \\
X_{bi} \\
X_{b2} \\
\vdots \\
X_{bn}
\end{bmatrix} = \begin{bmatrix}
\cos \theta & 0 & \cdots & 0 \\
0 & \cos \theta & 0 & \vdots \\
\vdots & \ddots & \ddots & \ddots \\
0 & \cdots & 0 & \cos \theta \\
\sin \theta & 0 & \cdots & 0 \\
0 & \sin \theta & 0 & \vdots \\
\vdots & \ddots & \ddots & \ddots \\
0 & \cdots & 0 & \sin \theta
\end{bmatrix} \begin{bmatrix}
\sin \theta & 0 & \cdots & 0 \\
0 & \sin \theta & 0 & \vdots \\
\vdots & \ddots & \ddots & \ddots \\
0 & \cdots & 0 & \sin \theta
\end{bmatrix} \begin{bmatrix}
Z_{di} \\
Z_{d2} \\
\vdots \\
Z_{dn} \\
Z_{qi} \\
Z_{q2} \\
\vdots \\
Z_{qn}
\end{bmatrix}
\]

(3-77)

Further, simplification of the above equation yields to

\[
\begin{bmatrix}
X_{ai} \\
X_{bi}
\end{bmatrix} = \begin{bmatrix}
\cos In & -\sin In \\
\sin In & \cos In
\end{bmatrix} \begin{bmatrix}
Z_{d} \\
Z_{q}
\end{bmatrix}
\]

(3-78)

where \( In=\text{diag}(1,1,\ldots,1) \) is identity matrix.

* Drop \((t)\) and take it as implied in the sequel
If we take the partial derivative of this equation using

\[
R_n = \begin{bmatrix}
\cos In & -\sin In \\
\sin In & \cos In
\end{bmatrix},
\frac{d}{dt} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \frac{d}{dt} R_n \begin{bmatrix} Z_d \\ Z_q \end{bmatrix} + R_n \frac{d}{dt} \begin{bmatrix} Z_d \\ Z_q \end{bmatrix}
\]

We can obtain

\[
\frac{d}{dt} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \begin{bmatrix}
-\sin \theta \cos In & -\cos \theta \cos In \\
\cos \theta \cos In & -\sin \theta \cos In
\end{bmatrix} \frac{d}{dt} \begin{bmatrix} Z_d \\ Z_q \end{bmatrix} + \begin{bmatrix}
\cos \theta \sin In & \sin \theta \sin In \\
\sin \theta \sin In & -\cos \theta \sin In
\end{bmatrix} \frac{d}{dt} \begin{bmatrix} Z_d \\ Z_q \end{bmatrix}
\]

In Figure 3-38, the modulator inputs can be rewritten as,

\[
U_\alpha + jU_\beta = (U_d + jU_q)(\cos \theta(t) + j\sin \theta(t))
\]

\[
\begin{bmatrix}
u_\alpha \\
u_\beta
\end{bmatrix} = \begin{bmatrix}
\cos \theta & -\sin \theta \\
\sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix} u_d \\ u_q \end{bmatrix}
\]

\[(a)\]

\[
\begin{bmatrix}
u_d \\ u_q
\end{bmatrix} = \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix}
\]

\[(b)\]

\[
\begin{bmatrix}
\dot{X}_\alpha \\ \dot{X}_\beta
\end{bmatrix} = \begin{bmatrix}
A & 0 \\ 0 & A
\end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} + \begin{bmatrix}
B & 0 \\ 0 & B
\end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix}
\]

\[(3-82)\]

Hence, substituting \([u_\alpha, u_\beta]^T\) in equation (3-82) from equation (3-81a), we can obtain

\[
\begin{bmatrix}
\dot{X}_\alpha \\ \dot{X}_\beta
\end{bmatrix} = \begin{bmatrix}
A & 0 \\ 0 & A
\end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} + \begin{bmatrix}
B & 0 \\ 0 & B
\end{bmatrix} \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix} u_d \\ u_q \end{bmatrix}
\]

\[(3-83)\]

Substituting \([\dot{X}_\alpha, \dot{X}_\beta]^T\) in equation (3-80) into equation (3-83), substituting \([X_\alpha, X_\beta]^T\) in equation (3-78) into equation (3-83), substituting \([X_\alpha, X_\beta]^T\) in equation (3-78) into equation (3-84), substituting \([u_\alpha, u_\beta]^T\) in equation (3-81a) into equation (3-85), and substituting \([y_\alpha, y_\beta]^T\) in equation (3-85), equation (3-86) can be obtained referring to Appendix C.

\[
\begin{bmatrix}
y_\alpha \\ y_\beta
\end{bmatrix} = \begin{bmatrix}
C & 0 \\ 0 & C
\end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} + \begin{bmatrix}
D & 0 \\ 0 & D
\end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix}
\]

\[(3-84)\]

\[
\begin{bmatrix}
y_\alpha \\ y_\beta
\end{bmatrix} = \begin{bmatrix}
\cos \theta & -\sin \theta \\ \sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix} y_d \\ y_q \end{bmatrix}
\]

\[(3-85)\]

\[
\dot{Z}_{dq} = A_{dq} Z_{dq} + B_{dq} u_{dq}
\]

\[
y_{dq} = C_{dq} Z_{dq} + D_{dq} u_{dq}
\]

\[(3-86)\]
where, 

\[
A_{dq} = \begin{bmatrix}
A & I\omega_0 \\
-\omega_0 & A
\end{bmatrix},
B_{dq} = \begin{bmatrix}
B & 0 \\
0 & B
\end{bmatrix},
C_{dq} = \begin{bmatrix}
C & 0 \\
0 & C
\end{bmatrix},
D_{dq} = \begin{bmatrix}
D & 0 \\
0 & D
\end{bmatrix}
\]

The equivalent transfer function of the modulator/de-modulator system in dq reference frame can then be easily derived from the state-space equation (3-86), which is a group of TFs presented in equation (3-87). Figure 3-39 shows the block diagram for the transformed dq reference frame modulator/de-modulator system. Although some details are given here, the detailed derivation process for the equivalent dq frame state space equation or transfer function can be found in Appendix C.

\[
G_{dd}(s) = C(sI - A)[(sI - A)^2 + \omega_0^2]^{-1}B + D
\]

\[
G_{dq}(s) = C\omega_0[(sI - A)^2 + \omega_0^2]^{-1}B
\]

\[
G_{qd}(s) = -G_{dq}(s)
\]

\[
G_{qq}(s) = G_{dd}(s)
\]

Figure 3-39 Transfer function representation of the modulator/de-modulator system transform from \(\alpha\beta\) reference frame to dq reference frame

Note that the equivalent dq reference frame transfer function can be given in a much simpler format if it is written in a complex form as shown by

\[
G(s) = C_0[(s + j\omega) - A]^{-1}B_0 + D_0
\]  

(3-88)

This equation indicates that the transfer function transforming from \(\alpha\beta\) reference frame to dq reference frame can be done simply by adding a \(j\omega\) term to the Laplace factor.

Although the above methodology is given for state-space equation transforming from \(\alpha\beta\) reference frame to dq reference frame, similar relationship is also valid for abc natural reference frame to dq reference frame transformation since the abc natural reference frame
and αβ reference frame is simply related by the Clark Transformation matrix which is a constant matrix (see equation(2-2)). However, the dq reference frame rotates at a frequency \( \omega \) corresponding to the αβ and abc reference frame variables. It can be noted that this approach is valid for any linear component with transfer function derived in abc stationary natural frame such as a grid filter, or linear controllers implemented in abc reference frame or even in a physical grid model.

**B. Small Signal Model for DB Current Controller, Sampling and Delay Blocks**

As is discussed previously there is a common characteristic for the equivalent continuous domain models references to the DB controller, sampling block and delay block, since all of them can be written either in the lead-lag format or in the lead-lag-gain format which are summarized in Table 3-5. Note that the third column in Table 3-5 is a case example obtained by substituting the parameter listed in Appendix G and which will be used for simulation verifications later in this chapter.

**Table 3-5 Summary of transfer functions for DB current controller, sampling block and delay block**

<table>
<thead>
<tr>
<th>Block</th>
<th>Lead-Lag</th>
<th>Lead-Lag-Gain</th>
<th>Case Study</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB Block</td>
<td>( a + bs ) ( c + ds )</td>
<td>( k \frac{1 + Ts}{1 + Ts} )</td>
<td>(-0.01247 - 24.94 - 0.000001566 1.997)</td>
</tr>
<tr>
<td>Sampling</td>
<td>( 1 ) ( 1 + sT_s / 2 )</td>
<td>( 1 ) ( 1 + sT_s / 2 )</td>
<td>( 1 ) ( 1 + 0.0005s )</td>
</tr>
<tr>
<td>Delay Block</td>
<td>( 1 - sT_s / 2 ) ( 1 + sT_s / 2 )</td>
<td>( 1 - sT_s / 2 ) ( 1 + sT_s / 2 )</td>
<td>(-0.0005s + 1 ) ( 0.0005s + 1 )</td>
</tr>
</tbody>
</table>

**Equivalent transfer function in dq reference frame**

As is explained above, the equivalent dq reference frame transfer function was simplified by replacing s term with \( s + j \omega \) term. For a general lead-lag block, the consequential shift for the αβ reference frame is presented in Table 3-6. Substituting the parameter listed in the case study column of Table 3-5, the equivalent dq frame transfer
functions for the target blocks can be obtained as shown in Figure 3-40. It should be noted that so far, the transfer functions of the DB controllers are successfully transformed to dq reference frame.

![Small signal model for DB current controller in equivalent dq reference frame](image)

**Figure 3-40** Small signal model for DB current controller in equivalent dq reference frame

**Table 3-6** Equivalent dq reference frame transfer function for the lead-lag block

<table>
<thead>
<tr>
<th>αβ reference frame transfer function</th>
<th>dq reference frame transfer function</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Y(s) = \frac{a + bs}{c + ds}$</td>
<td>$\frac{Y(s)}{X(s)}_{dq} = \frac{a + b(s + j\omega)}{c + d(s + j\omega)} = G_1(s) + j \cdot G_2(s)$</td>
</tr>
<tr>
<td>Main loop</td>
<td>$G_1(s) = \frac{bds^2 + (ad + bc)s + (ac + bd\omega_1^2)}{d^2s^2 + 2dcs + c^2 + d^2\omega_2^2}$;</td>
</tr>
<tr>
<td>Cross-coupling</td>
<td>$G_2(s) = \frac{ad\omega_1 - cb\omega_1}{d^2s^2 + 2dcs + c^2 + d^2\omega_2^2}$;</td>
</tr>
</tbody>
</table>

**C. Simulation Verification**

To test the accuracy of the DB controller in terms of equivalent transfer function and state space equations in the dq reference frame, two step tests are performed: i) -0.02pu step change on $U_q$ and ii) -0.02pu step change on $U_d$ imposed on the three target blocks in series (which included DB control block, sampling block and computation delay block).
3.2. Characterizing the Components of VSC Small Signal Model

Figure 3-41 Compare $Y_d/Y_q$ outputs from (i) the modulator/de-modulator system; (ii) the small-signal equivalent transfer function and (iii) the small-signal equivalent state space. (a) $U_{d\text{STEP}} = 0$, $U_{q\text{STEP}} = -0.02$ and (b) $U_{d\text{STEP}} = -0.02$, $U_{q\text{STEP}} = 0$;

Figure 3-42 Difference between $Y_d/Y_q$ outputs from (i) the modulator/de-modulator system versus the small-signal equivalent transfer function; (ii) the modulator/de-modulator system versus the small-signal equivalent state space. (a) $U_{d\text{STEP}} = 0$, $U_{q\text{STEP}} = -0.02$ and (b) $U_{d\text{STEP}} = -0.02$, $U_{q\text{STEP}} = 0$;

The results presented in Figure 3-41 indicate that there is a good agreement on the test results, since the difference between $Y_d/Y_q$ outputs from the modulator/de-modulator system compared with the small-signal equivalent transfer function is small. In addition, the calculated errors in the modulator/de-modulator system compared to the small-signal
CHAPTER 3: ANALYTICAL MODELING OF DB CONTROLLED VSC

equivalent state-space model further confirm the conclusion drawn above, as shown in Figure 3-42.

Equivalent State-Space Equation in dq Frame

To obtain the equivalent state-space equations in dq reference frame, the state-space equation for the $\alpha\beta$ reference frame transfer function should be defined first which is written in the lead-lag-gain format (see Appendix D),

$$\begin{align*}
\begin{cases}
sz = Az + Bx \\
y = Cz + Dx
\end{cases}
\end{align*}
$$

(3-89)

Where $A = \frac{1}{T_b} I_b; B = \frac{k}{T_b} I_{\text{ref}}; C = 1; D = \frac{k}{T_b} I_{\text{ref}}$

| Table 3-7 State space equations for DB controller in equivalent dq reference frame |
|-----------------------------------------------|-----------------------------------------------|
| **Dead-Beat Block**                          | **Small signal state space model**             |
| $\frac{dw_{\alpha, \text{cb}}}{dt} = A_{\alpha, \text{cb}} w_{\alpha, \text{cb}} + \omega w_{\alpha, \text{cb}} + B_{\alpha, \text{cb}} I_{d\text{,ref}}$ | $\frac{d\Delta w_{\alpha, \text{cb}}}{dt} = A_{\alpha, \text{cb}} \Delta w_{\alpha, \text{cb}} + \alpha \Delta w_{\alpha, \text{cb}} + B_{\alpha, \text{cb}} \Delta I_{\text{d,ref}}$ |
| $V_{\text{d,ref}}(k) = C_{\alpha, \text{cb}} w_{\alpha, \text{cb}} + D_{\alpha, \text{cb}} \Delta I_{\text{d,ref}}$ | $\Delta V_{\text{d,ref}}(k) = C_{\alpha, \text{cb}} \Delta w_{\alpha, \text{cb}} + D_{\alpha, \text{cb}} \Delta I_{\text{d,ref}}$ |
| $\frac{dw_{\beta, \text{cb}}}{dt} = -\omega w_{\beta, \text{cb}} + A_{\beta, \text{cb}} w_{\beta, \text{cb}} + B_{\beta, \text{cb}} \Delta I_{\text{q,ref}}$ | $\frac{d\Delta w_{\beta, \text{cb}}}{dt} = -\omega \Delta w_{\beta, \text{cb}} + A_{\beta, \text{cb}} \Delta w_{\beta, \text{cb}} + B_{\beta, \text{cb}} \Delta I_{\text{q,ref}}$ |
| $V_{\text{q,ref}}(k) = C_{\beta, \text{cb}} w_{\beta, \text{cb}} + D_{\beta, \text{cb}} \Delta I_{\text{q,ref}}$ | $\Delta V_{\text{q,ref}}(k) = C_{\beta, \text{cb}} \Delta w_{\beta, \text{cb}} + D_{\beta, \text{cb}} \Delta I_{\text{q,ref}}$ |

**Sampling block**

$\frac{dZ_{d, \text{sp}}}{dt} = A_{\text{p,sp}} Z_{d, \text{sp}} + \omega Z_{q, \text{sp}} + B_{\text{p,sp}} V_{\text{d,ref}}$

$V_{\text{d,ref}}(k) = C_{\text{p,sp}} Z_{d, \text{sp}} + D_{\text{p,sp}} V_{\text{d,ref}}$

$\frac{dZ_{q, \text{sp}}}{dt} = -\omega Z_{d, \text{sp}} + A_{\text{p,sp}} Z_{q, \text{sp}} + B_{\text{p,sp}} V_{\text{d,ref}}$

$V_{\text{q,ref}}(k) = C_{\text{p,sp}} Z_{q, \text{sp}} + D_{\text{p,sp}} V_{\text{d,ref}}$

**Delay block**

$\frac{dM_{d, \text{al}}}{dt} = A_{d, \text{al}} M_{d, \text{al}} + \omega M_{q, \text{al}} + B_{d, \text{al}} V_{\text{d,ref}}(k)$

$V_{\text{d,ref}}(k) = C_{d, \text{al}} M_{d, \text{al}} + D_{d, \text{al}} V_{\text{d,ref}}(k)$

$\frac{dM_{q, \text{al}}}{dt} = -\omega M_{d, \text{al}} + A_{d, \text{al}} M_{q, \text{al}} + B_{d, \text{al}} V_{\text{q,ref}}(k)$

$V_{\text{q,ref}}(k) = C_{d, \text{al}} M_{q, \text{al}} + D_{d, \text{al}} V_{\text{q,ref}}(k)$

$\frac{dM_{d, \text{al}}}{dt} = A_{d, \text{al}} \Delta M_{d, \text{al}} + \omega \Delta M_{q, \text{al}} + B_{d, \text{al}} \Delta V_{\text{d,ref}}(k)$

$\Delta V_{\text{d,ref}}(k) = C_{d, \text{al}} \Delta M_{d, \text{al}} + D_{d, \text{al}} \Delta V_{\text{d,ref}}(k)$

$\frac{dM_{q, \text{al}}}{dt} = -\omega \Delta M_{d, \text{al}} + A_{d, \text{al}} \Delta M_{q, \text{al}} + B_{d, \text{al}} \Delta V_{\text{q,ref}}(k)$

$\Delta V_{\text{q,ref}}(k) = C_{d, \text{al}} \Delta M_{q, \text{al}} + D_{d, \text{al}} \Delta V_{\text{q,ref}}(k)$
3.2. Characterizing the Components of VSC Small Signal Model

By adding with the cross-coupling term $j\omega$, we can obtain the state space equation in dq reference frame for lead-lag block as shown in equation (3-90). The state-space equations for DB control block, sampling block and delay block in equivalent dq reference frame are obtained reference to Table 3-5, and equations (3-89) and (3-90), which are summarized in Table 3-7 (in which the second column stands for the large signal models, while the third column denotes the small signal models).

$$\begin{align*}
\frac{d\Delta z_d}{dt} &= A_{LL}\Delta z_d + \omega\Delta z_q + B_{LL}\Delta x_d \\
\Delta y_d &= C_{LL}\Delta z_d + D_{LL}\Delta x_d \\
\frac{d\Delta z_q}{dt} &= -\omega\Delta w_q + A_{LL}\Delta z_q + B_{LL}\Delta x_q \\
\Delta y_q &= C_{LL}\Delta z_q + D_{LL}\Delta x_q
\end{align*}$$

(3-90)

where, the subscript LL denotes lead-lag.

D. Limitation of the Equivalent State Space Equation

It is important to understand the impact of the varying frequency to the modulator/de-modulator elimination approach. Therefore, two types of tests have been performed: i) small step on frequency (1%), (where $\omega = \omega_0 + 2\pi Ku(t)$, $K=0.01$, $t=0.01s$) and ii) sinusoidal disturbance with small magnitude (where $\omega = \omega_0 + K\sin(\Omega t)$, $K=0.01$, $\Omega=10\text{Hz}$, $t=0.01s$); Before conducting these tests, a step change ($u_d=0$, $u_q=-0.02\text{pu}$, $t=0.001s$) is initially applied to the system input. By examining the output differences between the $\alpha\beta$ frame TF and dq frame TF, the limitation of the dq equivalence can be easily observed.
Figure 3-43 Compare $Y_d/Y_q$ outputs from the (i) modulator/de-modulator system; (ii) the small-signal equivalent transfer function and iii) the small-signal equivalent state space. (a) $Y_d$ computes from $U_{dSTEP} = 0, U_{qSTEP} = -0.02, (\omega = \omega_0 + 2\pi Ku(t), K=0.01, t=0.01s)$; (b) $Y_q$ computes from $U_{dSTEP} = 0, U_{qSTEP} = -0.02, (\omega = \omega_0 + 2\pi Ku(t), K=0.01, t=0.01s)$; c) $Y_d$ computes from $U_{dSTEP} = 0, U_{qSTEP} = -0.02, (\omega = \omega_0 + K\sin(\Omega t), K=0.01, \Omega=10Hz, t=0.01s)$; (d) $Y_q$ computes from $U_{dSTEP} = 0, U_{qSTEP} = -0.02, (\omega = \omega_0 + K\sin(\Omega t), K=0.01, \Omega=10Hz, t=0.01s)$;

From the tests results shown in Figure 3-43a and b, it can be seen that the value of the output is smaller than the exact one, which results in an under compensation on the generated voltage reference. The problem can be solved by using the PLL output frequency as a feedback to the TF coefficient calculation, or by increasing the controller’s gain to enhance the compensation. Therefore, it can be concluded that the increase or decrease in frequency can cause the outputs to be under or over compensated in the equivalent dq reference frame. Moreover, the results given in Figure 3-43c,d for sinusoidal input frequency disturbance test reveal that the magnitude of the consequential oscillation increases with the simulation time. Finally, it can be concluded that it is better to design the linear controller in dq reference frame but implemented in abc natural reference frame as it can offer better capability on frequency sensitiveness resistance.

### 3.2.7 Reference Voltage Generation of the Converter

Based on the voltage prediction model developed in section 3.2.4 and the DB predicted voltage in section 3.2.6, the input reference voltage of the converter can be easily obtained as,
3.2. CHARACTERIZING THE COMPONENTS OF VSC SMALL SIGNAL MODEL

\[
V_{cd \_ ref}^e = V_{cd \_ ref1}^e + V_{cd \_ ref2}^e \\
V_{cq \_ ref}^e = V_{cq \_ ref1}^e + V_{cq \_ ref2}^e
\]  

(3-91)

Then, linearized version of the above equation can be given by,

\[
\Delta V_{cd \_ ref}^e = \Delta V_{cd \_ ref1}^e + \Delta V_{cd \_ ref2}^e \\
\Delta V_{cq \_ ref}^e = \Delta V_{cq \_ ref1}^e + \Delta V_{cq \_ ref2}^e
\]  

(3-92)

Since the small signal model is accurate, no simulation verification is required.

3.2.8 Voltage Source Converter

It is necessary to characterize the two-level three phase VSC which is also a non-linear component of the system. Therefore, the mathematical model of the VSC is developed using the average-value modeling (AVM) approach and the small signal model for VSC is in dq0 reference frame. Note that, the AVM approach is appropriate enough when the switching frequency of the PWM is much greater than the grid frequency. The simplified linearized model is verified by comparing the outputs of the AVM model and the non-linear model built in PSCAD/EMTDC.

3.2.8.1 Small Signal Model for VSC

Using the approach adopted in [129, 130], it is assumed that there is no energy storage component in VSC, moreover, since the reaction speed is extremely fast compared to the frequency range of interest, the relationship between the ac voltages/currents and the dc side variables can be considered purely algebraic.

Therefore in a balanced system, the averaged model of the three phase two-level VSC can be given by,

\[
V_{c\_ abc}(t) = \frac{V_{dc}(t)}{2} m_{abc}(t)
\]  

(3-93)

where, the \( V_{c\_ abc}(t) \) is the vector of VSC terminal voltages, \( V_{dc}(t) \) represents the dc voltage, and the \( m_{abc}(t) \) is the modulation signal, which can be given by,

\[
m_a(t) = M \cos(\theta + \delta) \\
m_b(t) = M \cos(\theta + \delta - 2/3\pi) \\
m_c(t) = M \cos(\theta + \delta + 2/3\pi)
\]  

(3-94)

Note that in the above equation M controls the magnitude of the AC output voltage, \( \theta \) is the angle of the bus voltage at PCC point that is provided by a PLL and the derivative of
$\theta$ (d$\theta$/dt) is the angular frequency $\omega$ of the AC supply. In addition, $\delta$ is the relative angle of VSC terminal voltage $V_{c,dc}$ which is controlled by the control system of the converter.

Hence, the dq reference frame averaged model of three-phase two-level VSC can be given by [2, 72],

$$V_{cq} = M \cos \theta \frac{V_{dc}}{2} = M_q \frac{V_{dc}}{2}$$

$$V_{cd} = M \sin \theta \frac{V_{dc}}{2} = M_d \frac{V_{dc}}{2}$$

(3-95)

where, the magnitude $M$ is equal to $\sqrt{V_{cd}^2 + V_{cq}^2} / (V_{dc} / 2)$ and the angle $\theta$ is equal to $\tan^{-1}(V_{cd} / V_{cq})$ which is known as the modulation ratio or VSC’s terminal voltage angle.

If we substitute $M$ and $\theta$ into the above equation, we will obtain,

$$V_{cd}^{c} = V_{cd,\text{ref}}^{c} \cdot V_{dc} / V_{dc0}$$

$$V_{cq}^{c} = V_{cq,\text{ref}}^{c} \cdot V_{dc} / V_{dc0}$$

(3-96)

which can be written in grid RI reference frame as

$$V_{cR}^{g} = V_{cR,\text{ref}}^{g} \cdot V_{dc} / V_{dc0}$$

$$V_{cI}^{g} = V_{cI,\text{ref}}^{g} \cdot V_{dc} / V_{dc0}$$

(3-97)

If we linearize the above equations, we can obtain the small signal model that provides the link between the AC and the DC voltages of VSC.

$$\Delta V_{cR}^{g} = \Delta V_{cR,\text{ref}}^{g} (k) \cdot V_{cR,\text{ref}}^{g} + V_{cR,\text{ref}}^{g} \cdot \Delta V_{dc} / V_{dc0}$$

$$\Delta V_{cI}^{g} = \Delta V_{cI,\text{ref}}^{g} (k) \cdot V_{cI,\text{ref}}^{g} + V_{cI,\text{ref}}^{g} \cdot \Delta V_{dc} / V_{dc0}$$

(3-98)

Since the efficiency of the converters is high in such power applications, the conduction losses can often be ignored. Therefore, the DC-side and AC-side terminal quantities of the two-level VSC can be interconnected by the power balance equation as

$$P_{dc}(t) = P_{ac}(t)$$

which can be written using terminal quantities as [72, 77].

$$U_{dc}(t) i_{dc}(t) = \frac{3}{2} [V_{cq}(t)i_{cq}(t) + V_{cd}(t)i_{cd}(t)]$$

(3-99)

If we substitute equation (3-95) into the above equation, we can obtain the DC link current as,

$$i_{dc}(t) = \frac{3}{4} [M_q(t)i_q(t) + M_d(t)i_d(t)]$$

(3-100)
3.2. CHARACTERIZING THE COMPONENTS OF VSC SMALL SIGNAL MODEL

Similarly, linearized version of the above equation can provide the small signal model as [56],

$$\Delta i_{dc} = \frac{3}{4}(i_{q} \Delta M_{q} + M_{q} i_{q} \Delta q + i_{d} \Delta M_{d} + M_{d} \Delta i_{d})$$  (3-101)

The advantage of this model is that it does not include the complex switching states and ignore the influence of the high frequency harmonics. Therefore, such model can run faster than the detailed model simply acting as a voltage filtered model. However, ignoring the high frequency harmonics will also ignore the impact of high harmonics on the grid and the control. It should be noted that such model is only valid for frequencies up to about one-third of the VSC switching frequency and the switched model operates in the linear modulation region without over modulation, which is \(\sqrt{V_{dc}^2+V_{cq}^2} \leq V_{dc}/2\) [131].

It should be reported that the above assumption will not represent the real operation. However, a more accurate model is a very challenging task, since it depends on specific operating point as well as the loading conditions. As reported in paper [130], a parametric AVM model can be used for an accurate model. However, the establishment of the parametric AVM model requires simulations of a wide range of loading conditions based on a detailed model (closed loop simulation involving the control functions) to restore the coefficients (\(\alpha(\cdot), \beta(\cdot), \phi(\cdot)\)) as functions. Note that \(\alpha(\cdot)\) represents the algebraic function coefficient between the DC voltage and AC terminal voltage of the loading conditions; \(\beta(\cdot)\) represents the algebraic function coefficient between the AC terminal current and the DC current of the loading conditions, and \(\phi(\cdot)\) is the power factor angle. This angle can be expressed in terms of the dq components of the AC side voltage and the current as,

$$\phi(\cdot) = \tan^{-1}(\frac{\partial V}{\partial i_{dq}}) - \tan^{-1}(\frac{\partial V}{\partial i_{dq}})$$  (3-102)

If we replace the original constant value with these new algebraic coefficient functions as in [130], we can obtain a more accurate AVM model suitable for various loading conditions and operating points. However, it should be emphasized that these coefficients which vary with the operating points and load conditions can only be evaluated for a specific case, which cannot be formulated to represent all the operating conditions.
3.2.8.2 Simulation Verification

Since the small signal model is an ideal AVM model, it is expected to observe inaccuracies using the detailed model simulation. This is also due to the fact that the rated operating switching frequency in this study is 2000Hz which is not an ideal case. As it is mentioned above, the coefficients will vary with the operating points and loading conditions which cannot defined analytically. Note that the constant coefficient 1 used in this study for $V_{cd}/V_{cdref}$ and $V_{cq}/V_{cqref}$ is an approximation.

Figure 3-44 illustrates the test circuit for the detailed VSC model. In this method a small step change $\Delta V_{cq}$ (from $V_{cqref0}$ to $V_{cqref0} + \Delta V_{cq1}$) is applied to the q-axis voltage input reference $V_{cqref}$, while for d-axis voltage input reference $V_{cdref}$ is set to be $V_{cdref0}$. Then the reference voltage is transformed to abc reference frame as an input to the converter. To ensure the linearity of the VSC, the on-state resistance of the transistor and diode in the converter has to be small enough, which is set as 0.001Ω in the case study. The converter terminal output voltage $V_{c,abc}$ is in the abc natural reference frame needs to be transformed to dq reference frame before connecting to the first order low-pass filter to eliminate the high switching frequency harmonics. In the first stage, dq reference frame converter terminal voltages $V_{cd}, V_{cq}$ are obtained.

The simulation results are given in Table 3-8. Note that the coefficients vary slightly from case to case. This suggests that there are some cross-coupling effects between d-q axes which are different from the AVM suggested coefficient 0, given earlier for $V_{cq}/V_{cdref}$ and $V_{cd}/V_{cqref}$. However, the discrepancies are found to be small once the loops of the
whole system are closed. But it should be noted that the AVM model causes an inaccurate loop gain which should be considered in the controller design.

Table 3-8 Simulation results for VSC model verification

<table>
<thead>
<tr>
<th>Test</th>
<th>Vcqref(Vcqref=-8.11)</th>
<th>Vcq</th>
<th>Vcd</th>
<th>ΔVcq/ΔVcqref</th>
<th>ΔVcd/ΔVcdref</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-49.6566</td>
<td>-49.7538</td>
<td>-8.1407</td>
<td>0.864</td>
<td>-0.02</td>
</tr>
<tr>
<td>2</td>
<td>-50.5129</td>
<td>-50.501</td>
<td>-8.1169</td>
<td>0.8173</td>
<td>0.0178</td>
</tr>
<tr>
<td>3</td>
<td>-50.67</td>
<td>-50.6294</td>
<td>-8.1197</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>-50.8271</td>
<td>-50.7472</td>
<td>-8.1183</td>
<td>0.7498</td>
<td>-0.0089</td>
</tr>
<tr>
<td>5</td>
<td>-51.6834</td>
<td>-51.7274</td>
<td>-8.1319</td>
<td>1.0835</td>
<td>0.012</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test</th>
<th>Vcdref(Vccdref=-50.67)</th>
<th>Vcd</th>
<th>Vcq</th>
<th>ΔVcd/ΔVcdref</th>
<th>ΔVcq/ΔVcqref</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-7.9478</td>
<td>-7.9607</td>
<td>-50.6363</td>
<td>0.9803</td>
<td>-0.0425</td>
</tr>
<tr>
<td>2</td>
<td>-8.0849</td>
<td>-8.0799</td>
<td>-50.6218</td>
<td>1.5857</td>
<td>0.302</td>
</tr>
<tr>
<td>3</td>
<td>-8.11</td>
<td>-8.1197</td>
<td>-50.6294</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>-8.1351</td>
<td>-8.1465</td>
<td>-50.6271</td>
<td>1.0678</td>
<td>-0.0916</td>
</tr>
<tr>
<td>5</td>
<td>-8.2722</td>
<td>-8.2757</td>
<td>-50.6166</td>
<td>0.9618</td>
<td>-0.079</td>
</tr>
</tbody>
</table>

3.2.9 Grid Model

Figure 3-45 is given to present the topology of the AC grid, in which $U_s^g$ and $i_g^s$ represent the voltage and the current of the grid source respectively, while the $R_g$ and $L_g$ denote the resistance and the inductance of the grid. Note that, the capacitance $C_f$ and the resistance $R_f$ in series in the figure represent the grid filter, and $R_c$ and $L_c$ are the resistance and the inductance of the converter reactor. The converter terminal voltage and the current are given by $V_c^g$ and $i_c^g$.
Using the circuit analysis (KVL, KCL) for the grid circuit given above, a set of equations can be obtained as given in the second column of Table 3-9. As concluded in section 3.2.6.2, the method used to obtain the equivalent linearized small-signal model of modulator/de-modulator system is also suitable for the grid model. This can be done by replacing the $A_{0\beta}$ matrix with a new $A_{dq}$ matrix which involves the cross coupling components $j\omega$, which is listed in the third column of Table 3-9. Figure 3-46 illustrates the small signal model of the grid.

**Figure 3-46 Small signal model of the grid**

**Table 3-9 Summary of the large signal model of the AC grid in abc reference frame and small signal model in dq reference frame**

<table>
<thead>
<tr>
<th>abc reference frame large signal model</th>
<th>RI reference frame small signal model</th>
</tr>
</thead>
</table>
| $\frac{di_{e,abc}}{dt} = -\frac{R_e}{L_e}i_{e,abc} + \frac{1}{L_e}(u_{f,abc} - V_{e,abc})$ | $\begin{align*}
\frac{d\Delta i_{e,R}}{dt} &= -\frac{R_e}{L_e}\Delta i_{e,R} + \omega L_e\Delta i_{e,I} + \frac{1}{L_e}(\Delta u_{f,R} - \Delta V_{e,R}) \\
\frac{d\Delta i_{e,I}}{dt} &= -\omega L_e\Delta i_{e,R} - \frac{R_e}{L_e}\Delta i_{e,I} + \frac{1}{L_e}(\Delta u_{f,I} - \Delta V_{e,I})
\end{align*}$ |
| $u^s_{f,abc} = F_{fabc} + (i^s_{g,abc} - i^s_{e,abc})\cdot R_f$ | $\begin{align*}
\Delta u^s_{f,R} &= \Delta F_{j,RR} + (\Delta i^s_{g,R} - \Delta i^s_{e,R})\cdot R_f \\
\Delta u^s_{f,I} &= \Delta F_{j,RI} + (\Delta i^s_{g,I} - \Delta i^s_{e,I})\cdot R_f
\end{align*}$ |
| $\frac{dF_{fabc}}{dt} = \frac{1}{C_f}(i^s_{g,abc} - i^s_{e,abc})$ | $\begin{align*}
\frac{d\Delta F_{j,RR}}{dt} &= (1/C_f)\Delta i^s_{g,R} - (1/C_f)\Delta i^s_{e,R} + \omega L_e\Delta F_{j,RI} \\
\frac{d\Delta F_{j,RI}}{dt} &= (1/C_f)\Delta i^s_{g,I} - (1/C_f)\Delta i^s_{e,I} - \omega A_{0\beta}
\end{align*}$ |
| $\frac{di^s_{g,abc}}{dt} = \frac{1}{L_g}(U_{e,abc} - u_{f,abc}) - \frac{R_g}{L_g}i_{g,abc}$ | $\begin{align*}
\frac{d\Delta i^s_{g,R}}{dt} &= \frac{1}{L_g}(\Delta U_{e,R} - \Delta u_{f,R}) - \frac{R_g}{L_g}\Delta i^s_{g,I} + \omega L_e\Delta i^s_{g,I} \\
\frac{d\Delta i^s_{g,I}}{dt} &= \frac{1}{L_g}(\Delta U_{e,I} - \Delta u_{f,I}) - \frac{R_g}{L_g}\Delta i^s_{g,R} - \omega A_{0\beta}
\end{align*}$ |
3.3 COMPARISON OF THE SMALL SIGNAL LINEAR MODEL AND PSCAD SIMULATION

Figure 3-47 shows the test results of the i) grid side current and ii) filter bus voltage responses of the VSC model, which are obtained by applying a small step change -0.56kV on the input of the grid model $\Delta V_{G}^{C}$. Note that there is a good agreement on the results of the large signal model and the small signal model.

![Figure 3-47](image)

Figure 3-47 (a) Grid side current and (b) filter bus voltage responses of i) large signal model ii) small signal model following a input voltage step change order on $\Delta V_{Cq} = -0.56kV$.

Finally, the characterization and validation tasks with regards to all the individual component of the VSC small signal model are complete and prepared so far for the whole system validation.

3.3 Comparison of the Small Signal Linear Model and PSCAD Simulation

Before conducting the small signal analysis, the Newton Raphson method (self-developed in m-file) is employed to solve the operating (equilibrium) point of the set of non-linear algebraic equations. The results are compared with the outputs obtained from the Matlab tool-box (f solve) which is also a functional tool for solving non-linear equations.

Figure 3-48 shows the comparison between the small-signal model and detailed non-linear PSCAD simulation following a step change in q axis of the converter current reference for AC systems with two different SCRs. Figure 3-48a,b are the results for a
strong system with SCR equals to 20 following a -0.0095pu step change on $\Delta I_{cq,\text{ref}}$, while the results for a weak AC system with SCR equals to 2 following a 0.095pu step change on $\Delta I_{cq,\text{ref}}$ are denoted by Figure 3-48c and d. Note that, for Figure 3-48a, the green line denotes the reference value, the cyan line represents the output from the large signal model, the purple line represents the and q-axis converter terminal current in the converter reference frame $\Delta I_{cq}^c$ outputs from the small signal model; for Figure 3-48b, the blue line denotes the reference value, the red line stands for the output from the large signal model, the black line represents the d-axis converter terminal current in the converter reference frame $\Delta I_{cd}^c$ outputs from the small signal model; for Figure 3-48c, the d- and q- axes converter terminal currents in the converter reference frame, $\Delta I_{cd}^c$ and $\Delta I_{cq}^c$, are the outputs for an AC system with SCR=2; and a zoomed in figure for the initial section of Figure 3-48c is presented in Figure 3-48d.

The results presented in Figure 3-48a and b (where the VSC is simplified as a controlled voltage source in PSCAD) for a strong AC system indicate that the method has a limitation as it displays an extra error that is introduced when using the padé Approximation. Note that the d-axis cost nearly 9 times sampling period (where the sampling frequency is 4000Hz), while the q-axis settles within about 7 sampling periods. However, the discrete controller itself only cost 2 sampling time to settle down as designed. Despite these limitations, the dynamic simulation results reveal a good agreement on the system performance. However, in a weak AC system, Figure 3-48 (c) and (d), the dynamic simulation results reveal a better agreement on the system performance. Both of the d and q axes cost 4 times sampling periods to closely track the current output from the PSCAD large signal model. In addition, the DB controller presents a slower current tracking ability in the weak AC system compared to the strong AC system.

![Diagram](a) ![Diagram](b)
3.3. COMPARISON OF THE SMALL SIGNAL LINEAR MODEL AND PSCAD SIMULATION

Figure 3-48 Comparison of the converter output current $\Delta I_{cd}^c, \Delta I_{cq}^c$ using the (i) large signal model simulating with VSC simplified as a controlled voltage source; (ii) the small-signal model for AC system with different SCRs.

It can be easily seen from the results shown in Figure 3-49 more harmonics with switching frequency appeared in the plots (due to switched converter modeling) compared with that of the results shown in Figure 3-48. However, it can be clearly concluded that the linear small signal model for the DB controlled VSC demonstrates an accurate approximation of the detailed model developed in PSCAD within the frequency range of interest.
3.4 Extension of the DB Controlled VSC Together with DC Link

3.4.1 Model of DC Link

The detailed model of the DC transmission system has already been studied in [53, 63, 71, 72, 74, 75, 77, 132, 133]. The model of the DC circuit is given in Figure 3-50, and Table 3-10 summarises the relationship between the DC side current, voltage and load current for both large and small signal models. As stated in section 3.2.8.1, the AC/DC side can be linked through equation (3-101). Therefore, the equivalent circuit of the AC side can be modelled as constant current sources $I_{dc\_rec}$ and $I_{dc\_inv}$ in the DC side modeling. If we linearize these equations, the small signal model equations for DC link are obtained, which are given in the second column of Table 3-10.
Figure 3-50 The model DC transmission link

Table 3-10 The model DC transmission link

<table>
<thead>
<tr>
<th>Large signal model for DC link</th>
<th>Small signal model for DC link</th>
</tr>
</thead>
<tbody>
<tr>
<td>$dV_{dc_{rec}} \over dt = \frac{I_{dc_{rec}}}{C_{dc_{rec}}} - \frac{I_{cde_{rec}}}{C_{dc_{rec}}}$</td>
<td>$dV_{dc_{rec}} \over dt = \frac{\Delta I_{dc_{rec}}}{C_{dc_{rec}}} - \frac{\Delta I_{cde_{rec}}}{C_{dc_{rec}}}$</td>
</tr>
<tr>
<td>$dI_{cde_{rec}} \over dt = \frac{V_{dc_{rec}}}{L_{dc_{rec}}} - \frac{V_{cde}}{L_{dc_{rec}}} - \frac{R_{dc_{rec}}I_{cde_{rec}}}{L_{dc_{rec}}}$</td>
<td>$dI_{cde_{rec}} \over dt = \frac{\Delta V_{dc_{rec}}}{L_{dc_{rec}}} - \frac{\Delta V_{cde}}{L_{dc_{rec}}} - \frac{R_{dc_{rec}}\Delta I_{cde_{rec}}}{L_{dc_{rec}}}$</td>
</tr>
<tr>
<td>$dV_{cde} \over dt = \frac{I_{dc_{rec}}}{C_{dc_{line}}} - \frac{I_{cde_{inv}}}{C_{dc_{line}}}$</td>
<td>$dV_{cde} \over dt = \frac{\Delta I_{dc_{rec}}}{C_{dc_{line}}} - \frac{\Delta I_{cde_{inv}}}{C_{dc_{line}}}$</td>
</tr>
<tr>
<td>$dI_{cde_{inv}} \over dt = \frac{V_{cde}}{L_{dc_{inv}}} - \frac{V_{de_{inv}}}{L_{dc_{inv}}} - \frac{R_{dc_{inv}}I_{cde_{inv}}}{L_{dc_{inv}}}$</td>
<td>$dI_{cde_{inv}} \over dt = \frac{\Delta V_{cde}}{L_{dc_{inv}}} - \frac{\Delta V_{de_{inv}}}{L_{dc_{inv}}} - \frac{R_{dc_{inv}}\Delta I_{cde_{inv}}}{L_{dc_{inv}}}$</td>
</tr>
<tr>
<td>$dV_{de_{inv}} \over dt = \frac{I_{cde_{inv}}}{C_{dc_{inv}}} - \frac{I_{de_{inv}}}{C_{dc_{inv}}}$</td>
<td>$dV_{de_{inv}} \over dt = \frac{\Delta I_{cde_{inv}}}{C_{dc_{inv}}} - \frac{\Delta I_{de_{inv}}}{C_{dc_{inv}}}$</td>
</tr>
</tbody>
</table>

Note that, although the established DC link model appears to represent a mono-polar link, it is also applicable to represent bi-polar links. But we need to apply the following two rules to specify the line, cable and shunt capacitors parameters when representing a bipolar link [134],

- sum the respective quantities for each line and capacitance to specify the total line, cable resistance, inductance and capacitance.
- specify the shunt capacitance by summing the capacitance between the positive polar to neutral point and the capacitance between the negative polar to neutral point.
Figure 3-51 illustrates the block diagram of the small signal model for the DC link, which will be verified against the PSCAD large signal model. In the verification study, the parameters given Table 3-11 are used.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rectifier Side Constant Current Source</td>
<td>75/130 = 0.577 [kA]</td>
</tr>
<tr>
<td>Rectifier Side Capacitor</td>
<td>500.0 [uF]</td>
</tr>
<tr>
<td>Rectifier Side Transmission Line resistance</td>
<td>7 [ohm]</td>
</tr>
<tr>
<td>Rectifier Side Transmission Line Inductance</td>
<td>0.5968 [H]</td>
</tr>
<tr>
<td>Transmission Line Capacitor</td>
<td>26.0 [uF]</td>
</tr>
<tr>
<td>Inverter Side Transmission Line resistance</td>
<td>7 [ohm]</td>
</tr>
<tr>
<td>Inverter Side Transmission Line Inductance</td>
<td>0.5968 [H]</td>
</tr>
<tr>
<td>Inverter Side Capacitor</td>
<td>500.0 [uF]</td>
</tr>
<tr>
<td>Inverter Side Constant Current Source</td>
<td>[75-(75/130)²]/130 = 0.574 [kA]</td>
</tr>
</tbody>
</table>

Figure 3-51 Test circuit for DC link test

Figure 3-52 The converter currents behind the DC capacitor from both of the rectifier side and inverter side (circle: Large signal model; rectangular: Small signal model)
The results shown in Figure 3-52 are obtained by applying a step change 0.577kA to the input of the DC grid model \( I_{dc,rec} \), which indicate the accuracies of the small signal model since the large signal model and the small signal model currents are very similar.

### 3.4.2 Interconnection of Subsystems

So far the models of all system components have been transformed into their state space form. A single state-space model can be obtained by grouping these sub-models appropriately and facilitating the application of the linear control design techniques. Although this has been maintained in [80, 87, 135] before, they were all based upon the matrix substitution technique. Therefore, this thesis offers an approach which is self-developed and adopted as given below.

\[
\begin{bmatrix}
\Delta X_i \\
\Delta Z_i
\end{bmatrix} =
\begin{bmatrix}
J_{XXi} & J_{XZi} \\
J_{ZXi} & J_{ZZi}
\end{bmatrix}
\begin{bmatrix}
\Delta X_i \\
\Delta Z_i
\end{bmatrix} +
\begin{bmatrix}
J_{XU_i} \\
J_{ZU_i}
\end{bmatrix}
\Delta U_i +
\begin{bmatrix}
J_{XUE_i} \\
J_{ZUE_i}
\end{bmatrix}
\Delta U_{iEXT}
\]

\[
\begin{bmatrix}
\Delta X_j \\
\Delta Z_j
\end{bmatrix} =
\begin{bmatrix}
J_{XXj} & J_{XZj} \\
J_{ZXj} & J_{ZZj}
\end{bmatrix}
\begin{bmatrix}
\Delta X_j \\
\Delta Z_j
\end{bmatrix} +
\begin{bmatrix}
J_{XU_j} \\
J_{ZU_j}
\end{bmatrix}
\Delta U_j +
\begin{bmatrix}
J_{XUE_j} \\
J_{ZUE_j}
\end{bmatrix}
\Delta U_{jEXT}
\]

Figure 3-53 Demonstration of sub-modular interconnection

Figure 3-53 shows a set of state space equations and algebraic equations to demonstrate the sub-modular interconnection approach.

The state space equations are defined by

\[
\begin{align*}
\begin{bmatrix}
\Delta X_i \\
\Delta Z_i
\end{bmatrix} &=
\begin{bmatrix}
J_{XXi} & J_{XZi} \\
J_{ZXi} & J_{ZZi}
\end{bmatrix}
\begin{bmatrix}
\Delta X_i \\
\Delta Z_i
\end{bmatrix} +
\begin{bmatrix}
J_{XU_i} \\
J_{ZU_i}
\end{bmatrix}
\Delta U_i +
\begin{bmatrix}
J_{XUE_i} \\
J_{ZUE_i}
\end{bmatrix}
\Delta U_{iEXT} \\
\Delta U_{jEXT} &=
\end{align*}
\]

(3-103)
\[ \Delta Y_i = J_{xi} \Delta X_i + J_{zi} \Delta Z_i + J_{ui} \Delta U_i; \]
\[ \Delta U_j = \Delta Y_j; \]  
\[ \Delta Y_j = J_{xy} \Delta X_j + J_{yz} \Delta Z_j + J_{yu} \Delta U_j; \]
\[ \Delta U_i = \Delta Y_i; \]  

The above equations can be written as,

\[ \Delta \dot{X}_i = \begin{bmatrix} J_{xx} & J_{xz} \\ J_{zx} & J_{zz} \end{bmatrix} \Delta X_i + \begin{bmatrix} \Delta U_i \\ J_{xu} \end{bmatrix} + \begin{bmatrix} J_{xu} \\ J_{zu} \end{bmatrix} \Delta U_{ext} \]  
\[ 0 = [J_{xy} J_{yz}] \Delta X_j + [J_{xz} J_{zz}] \Delta Z_j + [J_{xu} J_{zu}] \Delta U_j - [\Pi] \Delta Y_j \]  
\[ \Delta \dot{X}_j = \begin{bmatrix} J_{xy} & J_{xz} \\ J_{yx} & J_{yz} \end{bmatrix} \Delta X_j + \begin{bmatrix} \Delta U_j \\ J_{xj} \end{bmatrix} + \begin{bmatrix} J_{xj} \\ J_{zj} \end{bmatrix} \Delta U_{ext} \]  
\[ 0 = [J_{xy} J_{yz}] \Delta X_j + [J_{xz} J_{zz}] \Delta Z_j + [J_{xj} J_{zj}] \Delta U_j - [\Pi] \Delta Y_j \]  
\[ 0 = [\Pi] \Delta U_j - [\Pi] \Delta Y_j \]  
\[ 0 = [\Pi] \Delta U_i - [\Pi] \Delta Y_i \]  

Then they can be combined in a matrix form as,

\[ \begin{bmatrix} \Delta \dot{X}_i \\ \Delta \dot{X}_j \end{bmatrix} = \begin{bmatrix} J_{xx}(C) & 0 \\ 0 & J_{xz}(C) \end{bmatrix} \begin{bmatrix} \Delta X_i \\ \Delta X_j \end{bmatrix} + \begin{bmatrix} \Delta U_i \\ \Delta U_j \end{bmatrix} + \begin{bmatrix} \Delta U_{ext} \\ 0 \end{bmatrix} \]  

and

\[ \Delta X_{(C)} = \begin{bmatrix} \Delta X_i \\ \Delta X_j \end{bmatrix}^T; \]
\[ \Delta Z_{(C)} = \begin{bmatrix} \Delta Z_i \\ \Delta Z_j \\ \Delta Y_i \\ \Delta Y_j \\ \Delta U_i \\ \Delta U_j \end{bmatrix}^T; \]

Note that this allows us to obtain a single set of equation from two separate sets of equations. Hence, using this block interconnection approach, all the sub-components of the
system can be mathematically linked together, which completes the interconnection task of the subsystems.

### 3.4.3 Model of the DB Controlled VSC Including a DC Link

Before studying the outer loop controller design, the accuracy of base model for the controller design is determined as reference to the PSCAD large signal model. The circuit topology of the converter side outer loop controller is given in Figure 3-54, which takes into account the dynamics of the DC link.

![Figure 3-54 The base model for the converter side controller](image)

Similar to the results given in Figure 3-49, Figure 3-55 also reveals a good agreement on the system dynamic that includes the dynamics of the DC link, which is needed for the outer loop controller design. The results are obtained by applying a 0.095pu small step change on the q-axis of the input current reference of the converter.
Figure 3-55 Comparison of the converter output currents $\Delta I_{cd}^C, \Delta I_{cq}^C$ using the (i) large-signal model simulated in the detailed VSC model including the DC link, and (ii) the small-signal model for a weak AC system together with the DC link. The representations of the abbreviation in terms of D and D-FIR are the same as in Figure 3-49.

3.5 Conclusion

This chapter developed a complete small signal model for the DB controlled VSC including the DC link. In order to obtain the small signal model for the three phase discrete controller, four steps are involved. In the first step, the Padé Approximation is adopted to transfer the discrete controller to the continuous domain controller. In the second step, the abc three phase continuous domain controller is transformed to the $\alpha\beta$ reference frame controller, which is followed by transforming the controller from the $\alpha\beta$ reference frame to dq reference frame. In order to transform the controller from $\alpha\beta$ reference frame to dq reference frame, a frame transformation approach to eliminate the modulator and demodulator block was proposed in this chapter which has also been verified. It was noticed that, although the implementation of the Padé Approximation introduces a degree of error, it can still capture the main properties of the system, which can be a valid tool for the controller design. The small signal model development is presented systematically in the chapter including the derivation of the entire system equations which are then verified against the PSCAD simulations. In the simulation studies both of the large signal model
and small signal model are verified for every individual system components, as well as the entire integrated VSC system. It is demonstrated that the contribution of this study can be used as a solid foundation work that will be used in the remaining chapters of this thesis.
Chapter 3 has established the analytical base model for outer loop controller design, which will be used in this chapter to demonstrate the outer loop controller design for VSC-HVDC link integrated with a weak AC grid as it is a most likely scenario in planning the future Australian Network. In addition, the selected parameters sensitivity analysis will also be conducted. The small-signal stability analysis is performed to provide a powerful tool to predict the dynamics and stabilities of the system in detail. Using the eigenvalue analysis and participation factor analysis, the main causes of a system oscillation can be isolated and studied.

4.1 Introduction

Integrating a VSC-HVDC into a weak AC system which is characterized by large grid impedance and its corresponding control system design were a challenging task for the researchers. Traditionally, a cascade control scheme involving outer loop control and inner current loop control is utilized. In such an approach, the performance of the system predominantly depends on the performance of the inner current control, since a fast inner
current controller can provide sufficient frequency space for the outer power loop controller design.

It can be noted that the behavior of the inner current controller highly depends on the interaction of the current control, PLL control and filter bus capacitor. Specifically, under weak AC condition, the dynamics of PLL and filter bus capacitor play a critically important role. This is due to the success of a control system is based on the accuracy and speed response of PLL. However, the control of PLL is also highly governed by the voltage that is being locked to. In such a case, however, the filter bus voltage fluctuates dramatically, which is extremely sensitive to the converter current. This posed significant challenges to the PLL controller design. Therefore, it can be concluded that it is a highly complex control issue. Although two papers [54, 68] addressed this problem using simulation studies, it has not been studied systematically and quantitatively so far.

One of the motivations of this thesis is to perform a complete analysis for VSCs operating in weak AC grids by using a detailed accurate mathematical model from the small signal stability point of view. Furthermore, another motivation was to develop a fixed parameter controller with a simple structure (e.g. PI or PID). Although this is constrained by the limited bandwidth of the inner current controller it can still perform sufficiently well for a wide range of operating points.

4.2 Issues for VSC-HVDC Embedded in a Weak AC Grid

In a strong power system, the impact of grid impedance and filter dynamics can be ignored. Therefore, the filter bus voltage $u_f^g$ is independent of the converter current change. In such a system, the plant to be controlled is only the converter reactor which is a first-order system. However, the controlled plant becomes a third-order system since the dynamics of the grid impedance and the filter capacitance are taken into account, such as in a weak AC grid. The explicit circuit analysis in a weak AC grid is given in the following section.
### 4.2.1 Circuit Analysis

The single phase circuit diagram and its equivalent control circuit are given in Figure 4-1 [136, 137]. Note that the VSC is modelled by a controlled voltage source, in which the resistance loss is ignored and the transformer leakage \( L_\text{tr} \) is added to the grid side inductance \( L_g \).

\[ s \frac{L_g}{1} = L_g + L_\text{tr} \]

![Circuit Diagram](image)

**Figure 4-1 Single phase equivalent circuit**

From the analysis of the above circuits, the input voltage can be given by

\[
\begin{bmatrix}
E_g^g \\
V_c^g
\end{bmatrix} =
\begin{bmatrix}
z_{11} & z_{12} \\
\overline{z}_{21} & \overline{z}_{22}
\end{bmatrix}
\begin{bmatrix}
i_g^g \\
-i_c^g
\end{bmatrix}
\]

where, the impedance matrix is equal to

\[
\begin{bmatrix}
z_{11} & z_{12} \\
\overline{z}_{21} & \overline{z}_{22}
\end{bmatrix} =
\begin{bmatrix}
sL_g + \frac{1}{sC_f} + R_f & \frac{1}{sC_f} + R_f \\
\frac{1}{sC_f} + R_f & sL_c + \frac{1}{sC_f} + R_f
\end{bmatrix}
\]

(4-2)

Hence, the currents can be calculated as

\[
\begin{bmatrix}
i_g^g \\
-i_c^g
\end{bmatrix} =
\begin{bmatrix}
Y_{11} & Y_{12} \\
Y_{21} & Y_{22}
\end{bmatrix}
\begin{bmatrix}
E_g^g \\
V_c^g
\end{bmatrix} =
\begin{bmatrix}
z_{11} & z_{12} \\
\overline{z}_{21} & \overline{z}_{22}
\end{bmatrix}^{-1}
\begin{bmatrix}
E_g^g \\
V_c^g
\end{bmatrix}
\]

(4-3)

If we expand the above equation, the individual current functions can be given by

\[
\begin{aligned}
i_g^g &= Y_{11} \cdot E_g^g + Y_{12} \cdot V_c^g \\
-i_c^g &= Y_{21} \cdot V_c^g + Y_{22} \cdot V_c^g
\end{aligned}
\]

(4-4)

Hence, the admittance \( Y_{22} \) becomes...
The above equation shows that the plant to be controlled is a third-order system by taking into account the grid impedance \(L_s\) and filter capacitance \(C_f\). If it is applied to a strong AC grid, these two factors can be ignored and equation (4-5) is simply reduced to \(1/sL_c\) only, which is a first-order system.

### 4.2.2 System Stability Analysis based on A Simplified Model

To study the system stability, a simplified DB current controlled VSC block diagram is given in Figure 4-2, in which \(G_{db}(z)\) represents the DB current controller, \(G_{ZOH}(Z)\) represents the ZOH block, \(G_p(z)\) is the full representation of the plant to be controlled (i.e. the discrete form of equation (4-5)) and \(G_F(z)\) represents the feedback co-efficient.

As shown in Figure 4-3 and Figure 4-4a, the bandwidth of the system becomes narrower as the SCR decreases which corresponds to increase of the grid impedance. This results in a relatively long time to track the current reference as shown in Figure 4-4b (blue line). This narrow inner loop bandwidth poses further challenges to outer loop controller design, which also inevitably results in relatively slow responses of the control system when being subject to disturbances.
4.3 Controller Design Methodology

In the controller design, a set of detailed linear models of the open-loop transfer functions of VSC-HVDC control system are employed due to their simple and robust characteristics. The PI/PID compensator parameters are chosen such that the gain margin (GM) and phase margin (PM) of the compensated open-loop systems are within the ranges
of GM >= 6dB and PM >= 40° respectively. Figure 4-5 shows the flow chart of the process for designing such controllers.

4.3.1 Scenarios Considered in Controllers Design

The primary objective of control system design is to design robust controllers that can allow VSC operating in a wide range of operating conditions while considering various grid states and PQ capability of a VSC system. Two factors in the grid: i) SCRs and ii) X/R ratios are considered in this section.

The valid operating points of VSC-HVDC links can be defined by a PQ capability chart. Three major different limits are applied to VSC-HVDC links: i) maximum current through the converter ii) DC voltage and iii) Australian automatic access standard (see Figure 4-6a). By varying the rated voltages 1.02pu, 1.0pu and 0.98pu, three PQ charts are
obtained with different radiuses. This can help us to understand how the VSC terminal voltage will affect the PQ capability chart of VSC system.

The Automatic Access Standard in Australia states that [138]:

‘Any level of active power and any voltage at the connection point within the limits established under cause S5.1a.4 without a contingency event, must be capable of supplying and absorbing continuously at its connection point an amount of reactive power of at least the amount equal to the product of the rated active power of the generating system and 0.395.’

To meet the above requirement, an additional vertical purple line in Figure 4-6a is added. In this study, the DC voltage is chosen reasonably high, which is not a limiting factor. Therefore, only two limits are imposed on the system as shown in Figure 4-6b. The operating scenarios in terms of VSC PQ capability considered in this section are shown in Figure 4-6b which involves different loading conditions (P_{max}, P_{half} and P_0) and various level of power factors (leading, unity and lagging). In addition, the grid conditions that SCR and X/R ratios are also considered as operating scenarios which are listed in Table 4-1.

For weak AC system, the SCR is chosen as SCR=2, while for a strong system it is chosen as SCR=7.5. For X/R ratios, the pure impedance condition (at 90°) and line resistor Rg with an impedance angle 75° are considered. The combination of these conditions allows us to study 36 different operating scenarios, which covers a wide range of operating points in such grid-connected VSC system.
4.3. CONTROLLER DESIGN METHODOLOGY

Table 4-1 Equivalent Thevenin impedance of the AC grid

| SCR = \( \frac{U^2}{|Z|P_{dc}} \) | | Angle of | \( R_g : (|Z|\cos0) (\Omega) \) | \( L_g : (|Z|\sin0/2\pi f) \) (H) |
|---|---|---|---|---|
| 2 | 26.042 | 90° | 0 | 0.083 |
| | | 75° | 6.740 | 0.080 |
| 7.5 | 6.944 | 90° | 0 | 0.022 |
| | | 75° | 1.797 | 0.021 |

4.3.2 Calculation of the Steady State Operating Points

As it was stated before, Newton-Raphson method is used to solve the set of non-linear equations. The output results can be further compared with the results output from the ‘fsolve’ functions in MATLAB. It should be emphasized that a set of operating scenarios are taken into account for solutions during the calculation processes.

In this section, a set of functions \( F \) are defined over the unknown variables \( X \) that start with an initial guess of \( X_0 \) which is reasonably close to the roots of the set of function \( F \). A better approximation \( X_1 \) is obtained using the below equation which iterates many times until convergence is reached [139].

\[
X_{n+1}^{(i)} = X_n - \frac{F(X_n)}{F'(X_n)}
\]  

Table 4-2 Basic power flow equation

<table>
<thead>
<tr>
<th>( \hat{I}_c )</th>
<th>( \hat{I}_c = \frac{-\hat{V}_c + \hat{U}_f}{Z_c} = \frac{2}{3} \cdot \frac{P_c - jQ_c}{V_c^*} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \hat{I}_g )</td>
<td>( \hat{I}_g = \frac{-\hat{U}<em>f + \hat{E}<em>g}{Z_g} = \frac{2}{3} \cdot \frac{P</em>{ge} - jQ</em>{ge}}{U_f^*} )</td>
</tr>
<tr>
<td>( \hat{I}_g = \hat{I}_g + \hat{I}_f )</td>
<td>( \frac{2}{3} \cdot \frac{P_{ge} - jQ_{ge}}{U_f^<em>} = \frac{2}{3} \cdot \frac{P_c - jQ_c}{V_c^</em>} + jB \cdot \hat{U}_f )</td>
</tr>
</tbody>
</table>

Figure 4-7 shows a single line of the AC side of the converter that includes a high-pass filter. Using the Kirchhoff’s voltage law and the power balance relationship, the converter current, the filter current and the grid side current can easily be obtained as shown in Table
4-2. If we expand these equations and apply linearization, the F(X) and its Jacobian Matrix equations F'(X) can be defined which are summarized in Table 4-3, which form the basis for steady-state operating point calculation.

<table>
<thead>
<tr>
<th>No.</th>
<th>Power Flow Study Equations F(X)</th>
<th>Jacobian Matrix Equations F'(X)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( P_c = \frac{3}{2} (V_{cr} I_{cr} + V_{cl} I_{cl}) )</td>
<td>( \Delta P_c = \frac{3}{2} \left( \Delta V_{cr} \cdot I_{cr,0} + \Delta I_{cr} \cdot V_{cr,0} + \Delta V_{cl} \cdot I_{cl,0} + \Delta I_{cl} \cdot V_{cl,0} \right) )</td>
</tr>
<tr>
<td>2</td>
<td>( Q_c = \frac{3}{2} (V_{cl} I_{cr} - V_{cr} I_{cl}) )</td>
<td>( \Delta Q_c = \frac{3}{2} \left( \Delta V_{cl} \cdot I_{cr,0} + \Delta I_{cr} \cdot V_{cr,0} - \Delta V_{cr} \cdot I_{cl,0} - \Delta I_{cl} \cdot V_{cl,0} \right) )</td>
</tr>
<tr>
<td>3</td>
<td>( I_{cr} = \frac{R_c}{R_c^2 + X_c^2} (U_{cr} - V_{cr}) + \ldots \left( \frac{X_c}{R_c^2 + X_c^2} (U_{\beta} - V_{\beta}) \right) )</td>
<td>( \Delta I_{cr} = \frac{R_c}{R_c^2 + X_c^2} (\Delta U_{\beta} - \Delta V_{\beta}) + \frac{X_c}{R_c^2 + X_c^2} (\Delta V_{\beta} - \Delta V_{\beta}) )</td>
</tr>
<tr>
<td>4</td>
<td>( I_{cl} = \frac{R_c}{R_c^2 + X_c^2} (U_{cr} - V_{cr}) + \ldots \left( \frac{X_c}{R_c^2 + X_c^2} (U_{\beta} - V_{\beta}) \right) )</td>
<td>( \Delta I_{cl} = \frac{R_c}{R_c^2 + X_c^2} (\Delta U_{\beta} - \Delta V_{\beta}) + \frac{X_c}{R_c^2 + X_c^2} (\Delta V_{\beta} - \Delta V_{\beta}) )</td>
</tr>
<tr>
<td>5</td>
<td>( P_{ge} = \frac{3}{2} (U_{jr} I_{gr} + U_{\beta} I_{gl}) )</td>
<td>( \Delta P_{ge} = \frac{3}{2} \left( \Delta U_{jr} \cdot I_{gr,0} + \Delta I_{gr} \cdot U_{jr,0} + \Delta U_{\beta} \cdot I_{gl,0} + \Delta I_{gl} \cdot U_{\beta,0} \right) )</td>
</tr>
<tr>
<td>6</td>
<td>( Q_{ge} = \frac{3}{2} (U_{jr} I_{gr} - U_{\beta} I_{gl}) )</td>
<td>( \Delta Q_{ge} = \frac{3}{2} \left( \Delta U_{jr} \cdot I_{gr,0} + \Delta I_{gr} \cdot U_{jr,0} - \Delta U_{\beta} \cdot I_{gl,0} - \Delta I_{gl} \cdot U_{\beta,0} \right) )</td>
</tr>
<tr>
<td>7</td>
<td>( I_{gr} = \frac{R_g}{R_g^2 + X_g^2} (E_{gr} - U_{jr}) + \ldots \left( \frac{X_g}{R_g^2 + X_g^2} (E_{\beta} - U_{\beta}) \right) )</td>
<td>( \Delta I_{gr} = \frac{R_g}{R_g^2 + X_g^2} (\Delta E_{\beta} - \Delta U_{\beta}) + \frac{X_g}{R_g^2 + X_g^2} (\Delta E_{\beta} - \Delta U_{\beta}) )</td>
</tr>
<tr>
<td>8</td>
<td>( I_{gl} = \frac{R_g}{R_g^2 + X_g^2} (E_{gr} - U_{jr}) + \ldots \left( \frac{X_g}{R_g^2 + X_g^2} (E_{\beta} - U_{\beta}) \right) )</td>
<td>( \Delta I_{gl} = \frac{R_g}{R_g^2 + X_g^2} (\Delta E_{\beta} - \Delta U_{\beta}) + \frac{X_g}{R_g^2 + X_g^2} (\Delta E_{\beta} - \Delta U_{\beta}) )</td>
</tr>
<tr>
<td>9</td>
<td>( I_{gr} = I_{cr} - B \cdot U_{\beta} )</td>
<td>( \Delta I_{gr} = \Delta I_{cr} - B \cdot \Delta U_{\beta} )</td>
</tr>
<tr>
<td>10</td>
<td>( I_{gl} = I_{cl} - B \cdot U_{\beta} )</td>
<td>( \Delta I_{gl} = \Delta I_{cl} - B \cdot \Delta U_{\beta} )</td>
</tr>
<tr>
<td>11</td>
<td>( U_{jr} = U_{f0} \cdot \cos(\theta_{PLL}) )</td>
<td>( \Delta U_{jr} = -U_{f0} \cdot \sin(\theta_{PLL,0}) \cdot \Delta (\theta_{PLL}) )</td>
</tr>
<tr>
<td>12</td>
<td>( U_{\beta} = U_{f0} \cdot \sin(\theta_{PLL}) )</td>
<td>( \Delta U_{\beta} = -U_{f0} \cdot \cos(\theta_{PLL,0}) \cdot \Delta (\theta_{PLL}) )</td>
</tr>
</tbody>
</table>
4.3.3 Controller Design for Rectifier

It can be noted that the bandwidth of the outer loop is highly influenced by the sub-systems. Therefore, the complete VSC-HVDC model is developed as a base study for outer loop controller design. However, the model of the long transmission line is also involved in this model, which has to be included in the design procedure for the accuracy purpose. This is particularly suitable for the Australian grid, where the renewable energy sources such as geothermal and wind energy resources are far away from the major load centres.

Figure 4-8 shows the pole-zero map and Bode plots of the inner DB current controller with and without the DC link model. As it can be seen in the Figure 4-8a that there are two more pole-zero pairs presented in the model with DC link than the model without DC link at very low frequency, which are nearly cancelled with each other. However, at frequency
around 30 rad/s, a pair of cancellable pole-zero pair exists in the model without DC link, while in the model with DC link there is only one pole pair which is un-cancellable (see the circled area in the Bode plot). In addition, small magnitude difference was observed in the Bode plots of two systems. The results reveal that it is possible to develop more accurate and realistic controllers when the dynamics of DC link are being considered.

4.3.3.1 Controller Design Circuit for Rectifier

The model adopted for the outer power controller design at the rectifier side is shown in Figure 4-9. The DC side transmission line is modelled as a T-section ended with a constant DC voltage source.

![Figure 4-9 Basic structure for outer power controller design](image)

Note that the control scheme used here is a cascade control strategy. The DB control scheme is adopted as the inner current control for both of the rectifier and inverter sides, while for the outer loops, the rectifier is responsible for controlling the active power and the constant filter bus AC voltage, and the inverter controls the DC voltage and the filter bus AC voltage to be constant.

The above circuit diagram is the basis for rectifier side controllers design. Due to the fact that the objective of the controller design is to control the DC voltage at the inverter end, the inverter can be simplified as a constant DC voltage source. Although the assumptions made here that the constant DC voltage controller is implemented ideally and the response speed of the DC voltage controller is sufficiently fast does not 100 per cent hold it is still adequate to be used as a start point in the controller design.
4.3.3.2 Inner Current Controller Analysis

The eigenvalues and their sensitivities are investigated to determine how the system parameters and loading conditions contribute to the small signal stabilities of the entire system.

A. Eigen-value Analysis

Table 4-4 shows all of the eigenvalues associated with the base loading scenario (at maximum power, unity power factor and for SCR equals to 2). As listed in the Table 4-4, all the eigenvalues have the negative real parts, which imply that the base loading scenario is stable. The dominant modes of the system are the modes 15 and 16 without adequate damping. The participation factors shown in Table 5-5 indicate that the DC link states have a dominant impact on the conjugate complex pair 15 and 16 with a damping ratio of 0.033 and a natural frequency of 28.949Hz. The modes 19 and 20 are the root causes of the small dip appeared in the frequency response plot of the weak AC system locating around 27.37 rad/s (see circled area in Figure 4-8b).

<table>
<thead>
<tr>
<th>Mode</th>
<th>Eigenvalue</th>
<th>Damping Ratio</th>
<th>Nature Frequency (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,2</td>
<td>-2.04·10^7±314j</td>
<td>1</td>
<td>50</td>
</tr>
<tr>
<td>3,4</td>
<td>-7.91·10^3±307j</td>
<td>1</td>
<td>48.834</td>
</tr>
<tr>
<td>5,6</td>
<td>-1.625·10^3±3.03·10^3j</td>
<td>0.473</td>
<td>482.18</td>
</tr>
<tr>
<td>7,8</td>
<td>-1.62·10^3±2.48·10^3j</td>
<td>0.547</td>
<td>394.78</td>
</tr>
<tr>
<td>9,10</td>
<td>-3·10^3±3.04·10^2j</td>
<td>0.994</td>
<td>48.345</td>
</tr>
<tr>
<td>11,12</td>
<td>-2.79·10^2±6.64·10^2j</td>
<td>0.387</td>
<td>105.69</td>
</tr>
<tr>
<td>13,14</td>
<td>-78.7±263.6j</td>
<td>0.286</td>
<td>41.955</td>
</tr>
<tr>
<td>15,16</td>
<td>-6.094±182j</td>
<td>0.033</td>
<td>28.949</td>
</tr>
<tr>
<td>17,18</td>
<td>-25.379±18.384j</td>
<td>0.81</td>
<td>2.926</td>
</tr>
<tr>
<td>19,20</td>
<td>-12.21±27.37j</td>
<td>0.407</td>
<td>4.3558</td>
</tr>
</tbody>
</table>

As shown in Table 4-5, the above mentioned modes 15, 16, 19 and 20 are also greatly influenced by the DC link states. Therefore, any attempts to improve these modes must
take into accounts these DC link states. PLL is mainly associated with the modes 17 and 18. While, the time constant of the AC voltage signal filter and the AC grid states are the main contributors to modes 11-14. The participation factor table also suggests that the states with respect to the circuit in adjacent area of VSC terminal (converter-reactance and grid voltage filter) and the DB controller have dominant impacts on modes 5-10. Lastly, the modes 1-4 are solely determined by the DB control block. In the following section, the eigen-sensitivity analysis in terms of these states will be explicitly discussed.

Table 4-5 Participation factors of dominant state variables for selected modes of the inner DB current controller

<table>
<thead>
<tr>
<th>Sub-System</th>
<th>State</th>
<th>Mode</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
<th>17</th>
<th>18</th>
<th>19</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid Controller</td>
<td>PLL</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td></td>
<td>TF</td>
<td>1.139</td>
<td>2.37</td>
<td>3.22</td>
<td>5.19</td>
<td>19.1</td>
<td>36.2</td>
<td></td>
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</tr>
<tr>
<td>DB control</td>
<td>DeadBeat</td>
<td>100</td>
<td>93.31</td>
<td>14</td>
<td>13.8</td>
<td>19.7</td>
<td>3.079</td>
<td>1.54</td>
<td></td>
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<tr>
<td></td>
<td>Sampling</td>
<td>2.24</td>
<td>14.2</td>
<td>14.2</td>
<td>17.1</td>
<td>2.772</td>
<td>2.58</td>
<td></td>
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</tr>
<tr>
<td></td>
<td>Delay</td>
<td>2.253</td>
<td>22.6</td>
<td>22.6</td>
<td>25</td>
<td>5.352</td>
<td>5.1</td>
<td></td>
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</tr>
<tr>
<td>AC network</td>
<td>Con-Reactance</td>
<td>33.7</td>
<td>33.4</td>
<td>22.5</td>
<td>10.87</td>
<td>5.32</td>
<td></td>
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<tr>
<td></td>
<td>Cf</td>
<td>1.054</td>
<td>12.1</td>
<td>12</td>
<td>9.62</td>
<td>11.55</td>
<td>12.3</td>
<td>0.34</td>
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</tr>
<tr>
<td></td>
<td>AC grid</td>
<td>0.97</td>
<td>0.92</td>
<td>0.87</td>
<td>46.39</td>
<td>29.3</td>
<td></td>
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B. Selected Parameter Sensitivity Effects on Main and Cross-Coupling Control Loops

In the below paragraphs, an in-depth analysis of the impact of the system parameters, the loading conditions and the power factor on system small-signal stability is given.

a) *SCR with Pure Impedance at Full Loading Condition*

The impact of SCR on system small-signal stability is investigated in this section. It is assumed that only the inner DB current loop is in operation, and operating under the full loading condition $P_{\text{max}}$. For simplicity, the loss of the transmission line is ignored. Therefore, the AC grid model is represented by an AC voltage source behind impedance through the Thevenin’s equivalence. The eigenvalue evolution map of the system with SCR reducing from 7.5 to 0.5 at a step -1 is shown in Figure 4-10a. As it can be seen in the figure, two modes move to the right half plane (RHP) which makes the system tending to be unstable as SCR reduces. Moreover, the bandwidth of the inner current loop is narrowed
down as the consequence of the high frequency modes evolving to the low frequency region. This makes the design of outer loop controller design even more complex and challenging.

![Figure 4-10](image)

Figure 4-10 (a) In the DB current controlled VSC with P=P_max (a) eigenvalue maps with SCR reduced from 7.5 to 0.5 at a step of -1 (i.e. A to G); (b) Bode plots of the TF (blue: SCR=7.5, red: SCR=4.5, cyan: SCR=2).

Figure 4-10b shows the Bode plots of the transfer function for the DB current controlled VSC. The upper left figure plot shows the magnitude plot for power. Note that, only the magnitude plot is shown here for simplicity purpose. It can be observed that the magnitude of the strong system has a higher gain compared with that of the weak AC system. However, it should be noted that this is not a regular pattern for all loading conditions. The test results of the zero loading condition (static synchronous compensator (STATCOM) mode) show a reverse pattern. Nevertheless, the Bode plots of the filter bus AC voltage (the lower plots of Figure 4-10b) confirm that it is more sensitive to the power variation in a weak AC grid. Furthermore, the upper right and lower left plots also confirm the fact that the cross-coupling effects increase as SCR reduces.

Figure 4-11 shows the time-domain simulation results in MATLAB and PSCAD/EMTDC following a 0.01pu step change on i_{qref} at t=0s. The PSCAD simulation confirms the accuracy of the small signal model again. In addition, the results also suggest that the time domain simulation agrees with the conclusion drawn from the frequency response analysis. For example, the speed of the current tracking response of the weak AC grid is slower compared with that of the strong AC grid, since the weak AC system has a
narrower bandwidth. As it is can be seen in the middle power plot of Figure 4-11, the system with a higher SCR has more reduction since the un-shown phase angle plot for the power curve starts from -180°. Furthermore, the third plot in Figure 4-11 shows that a much higher filter bus voltage (black and red plots) increase for weak AC system is observed compared with that of the strong system (see blue and cyan plots).

Figure 4-11 The time-domain simulation results: PSCAD SCR=7.5 (solid cyan line); Matlab SCR=7.5 (dash-dot blue line); PSCAD SCR=2 (solid black line); Matlab SCR=2(dash-dot red line).

b) $X/R$ Ratio for SCR=2 at Full Loading Condition

The second impact factor discussed is the equivalent grid impedance angle, which is equals to $X/R$ ratio. Four main low frequency modes are shown in Figure 4-12. The results reveal that the higher the resistance of the grid impedance, the more damping is added to the system regardless of the modes of operation (rectifier or inverter). This also implies that the system is more stable by solely inspecting Mode I1 at relatively high frequency. However, by observing Modes I3 and I4, a common trend can be summarized that the damping effects for the inverter are less than that of the rectifier. This also means the observed oscillation of the inverter should be a little higher than that of the rectifier when system being subject to transient disturbances.
4.3. Controller Design Methodology

Figure 4-12 Four main low frequency modes for A: rectifier mode with a 90° angle; B: rectifier mode with a 75° angle; C: rectifier mode with a 60° angle; a: inverter mode under 90° angle; b: inverter mode under 75° angle; c: inverter mode under 60° angle;

Figure 4-13 The Bode plots of the DB current controlled VSC. blue: rectifier mode under 90° angle; cyan: Rectifier mode under 75° angle; red: rectifier mode under 60° angle; magenta: inverter mode under 90° angle; black: inverter mode under 75° angle; green: inverter mode under 60° angle;

The Bode plots of the DB current controlled VSC are shown in Figure 4-13. As it can be observed in the top-left figure, the rectifier mode operation, the system with higher
impedance has the highest gain in the active power loop. At the inverter side the system with a higher resistance has the highest gain. It should also be emphasized here that a main trend can be observed the inverter has a relatively higher gain in comparison with that of the rectifier. Alternatively, for a rectifier, it can be interpreted as to transmit the same amounts of power the system with a higher resistance experiences larger current variation which results in the current level reaching its limit. Therefore, it can be concluded that the minimum SCR required in such system is higher than the more inductive system, while such trend reverses at the inverter reference to the Bode plots analysis. Moreover, the inverter is more robust when embedded in a weak AC system since it generally has a much higher gain than that of the rectifier side as shown in Figure 4-13a. The same conclusions have also been reported in ref [140].

It was also observed that the rate of change in $\Delta P/\Delta I_d$ or $\Delta U_f/\Delta I_d$ has a similar trend as in $\Delta P/\Delta I_q$. However, under above two conditions, the change in the relative gain is found to be not as big as that of in the power loop. Similarly, the rate of change in $\Delta U_f/\Delta I_q$ has an inverse trend. The more resistive system has the highest gain reference to the rectifier side, vice versa for the inverter side. In conclusion, the rectifier mode has a higher gain, but the inverter mode has a wider relative gain change. The time domain simulation results shown in Figure 4-14 also confirm the above conclusions.

![Step responses of DB current controlled VSC for the rectifier (left) and the inverter (right). rectifier mode at angle 90° (blue); rectifier mode at angle 75° (cyan); rectifier mode at angle 60° (red); inverter mode at angle 90° (magenta); inverter mode at angle 75° (black); inverter mode at angle 60° (green);](image-url)
c) Operation under Various Loading Condition at SCR=2

Figure 4-15 shows the eigen-value map and Bode plots of the DB current controlled VSC system embedded in a weak AC system at SCR=2 and under varying loading conditions. It is found that the loading condition has a significant impact on the cross-coupling behaviour of the system. As seen in Figure 4-15 (a), the mode I1 is relatively the most sensitive mode to the loading condition since it moves to the left with smaller damping ratio. However, it does not significantly affect the system stability.

![Figure 4-15](image)

Figure 4-15 For DB controlled VSC with SCR=2 (a) the eigenvalue map with P equals to be 1pu (A), 0.5pu (B) and 0pu (C); (b) Bode plots of the TF with different loading conditions. blue: P=1pu, cyan: P=0.5pu, red: P=0pu).

It can also be observed that the magnitude of the transfer function of the cross-coupling behaviors increased dramatically with loading conditions (see upper right and lower left plots in Figure 4-15b). This indicates that more interaction between active and reactive power loops could be observed once the outer power loops are closed.

d) Operation under Various Power Factors at SCR=2

As shown in Figure 4-16 modes I1 and I2 move to the opposite direction when varying the operating modes of VSC from receiving reactive power from grid to sending reactive power to grid. However, Mode I1 is the main limitation of the bandwidth of the $G_{Plq}(s)$. Note that the system with a leading power factor (case C in Figure 4-16a) has the narrowest bandwidth. Moreover, the impacts of changing power factor are more significant on the active power related loop (left column of Figure 4-16b), whereas the impacts on the reactive power loop are comparably small (right column of Figure 4-16).
It can be concluded from these results that SCR, X/R ratios, loading conditions and various power factors all have significant impacts on system small signal stabilities. Therefore, it is expected that these analyses can provide a better understanding on the characteristics of the plant to be controlled and facilitate ongoing controller design.

4.3.3.3 Power Controller Design for Rectifier

As it was mentioned at the beginning of this chapter, the primary aim of this chapter is to design a linear controller with a set of fixed parameter that can work under a wide range of operating conditions. However, it is important to note that the inner DB current controller of the weak AC grid connected VSC has a limited bandwidth as mentioned before.

A. Frequency Response Analysis of all the Covering Operating Points

It is important to examine the characteristics of the transfer functions for 36 scenarios mentioned earlier before conducting the controller design.

As shown in Figure 4-17a, b, c and d, the gain varies from 31.97dB to 36.79dB, which corresponds to a difference of 4.82dB (factor of 1.7418 which is acceptable under steady state). Under the weak AC system condition, the gain varies from 31.97dB to 36.77dB, which is much wider than the case of a strong system (in which the gain varies from 36.79 dB to 36.3 dB).
Figure 4-17 The analysis of the transfer functions using Bode plots and at 36 operating conditions in total (a) SCR=2 at 90°; (b) SCR=2 at 75°; (c) SCR=7.5 at 90°; (d) SCR=7.5 at 75°.

It can be seen in Figure 4-17a that the operating points under the same loading levels belong to the same group. In other words, the system delivering the same amounts of power have similar gains. For example, the operating points 7-9 which transfer zero power to the DC side have the highest set of gains. Similarly, the operating points 4-6 (half loading condition) have a set of moderate gains in the middle group, and the remaining 3 operating points which are the full-loading modes have the lowest set of gains. Moreover, the operating modes which absorb the maximum reactive power from grid has a comparably higher gains compared with the modes where the maximum reactive power is
sent to grid. Figure 4-17b has a similar trend with that of Figure 4-17a, while the rest of the results c and d of Figure 4-17 have reverse trends compared with the pattern observed in Figure 4-17a, b.

B. RHP Zero Limitation on Outer Loop Bandwidth

It is well known that the poles of a system have significant impact on system stability. However, there are limited studies on how the zeros of a system limit the controller design of a VSC-HVDC system. It was reported in [63] that the bandwidth of the closed-loop system should be chosen at least lower than half position of the RHP zero. A more accurate analysis was given in [141] indicated that the achievable bandwidth $\omega_b$ of the outer loop controller is significantly limited by the RHP zeros, which are

$$\omega_b \approx \omega_c \begin{cases} |z|/4 & \text{Re}(z) \gg \text{Im}(z) \\ |z|/2.8 & \text{Re}(z) = \text{Im}(z) \\ |z| & \text{Re}(z) \ll \text{Im}(z) \end{cases} \quad (4-7)$$

where, $z$ denotes the complex form of the system zero which is the closest to the origin. It can be summarized that to have RHP zeros close to origin is inappropriate, and it is even worse to have RHP zeros closer to the real axis rather than the imaginary axis [141]. It was also found in [141] that the root causes resulting in the RHP zeros is the competing effects among sub-components of a system.

As given in the figure below, there are 4 RHP zeros in Figure 4-18a and 1 RHP zero in Figure 4-18b involved in case C and F locating in different frequency range. This caused $1080^\circ$ change crossing low frequency to high frequency (see Figure 4-17a). It should be noted that the cases A-I given in Figure 4-18 correspond to the cases 1-9 given earlier in Figure 4-6b. Note that, these cases impose limits to the achievable bandwidth of the outer loop controller. The case F has the closest zero to the origin, which is located at $44.28 \text{ Np/s}+264.4 \text{ rad/s}$. This indicates that the designed outer loop controller should not exceed the value $|Z|/2$ which corresponds to $134.04 \text{ rad/s}$. In other words, a controller with an extremely fast responding speed is hard to achieve. Similarly, 3 RHP zeros included in the cases A, B, D, E, and G, induce $720^\circ$ change varying from low frequency to high frequency. Similarly, only 1 RHP zero in the cases H and I produce $360^\circ$ change in the phase plot.
4.3. Controller Design Methodology

Figure 4-18 Right half-plane zeros for the transfer function of the open loop power controller

C. Power Controller Design and its Small Signal Model

As indicated previously, the main aim of this sub-section is to design a power controller and then to develop its small signal model. Therefore, the design methodology is proposed first, which is not just limited to the power controller design, followed by step tests to evaluate the performance of the designed power controller.

a) Design Methodology

The proposed design methodology is composed of four steps:

Step 1: Observe the frequency responses of \( \frac{P(s)}{I_{qref}(s)} \), and then choose the cases with the lowest bandwidth, the highest bandwidth and the bandwidth in the middle of those two.

Step 2: Add a low-pass filter to ensure the open-loop gain is substantially less than DC gain at all frequencies (above the gain cross-over frequency, if necessary).

Step 3: Apply the classic loop-shaping technique to the system obtained in Step 2, and obtain the controller parameters \( K_p, K_i, K_d \) depending on the type of controller designed.

Step 4: Evaluate the controller performance thoroughly against the detailed model established on PSCAD/EMTDC simulator considering different size steps, operating points and SCRs.

In the first step, the frequency response plots presented in Figure 4-17 are analysed. In this design, cases 4, 6 and 9 are chosen as a reference for the design as given in Figure 4-19.
In step 2, a first-order low-pass filter (see Figure 4-20a) is added to the system. This indicates that an additional attenuation (where 20dB/decay rolling off when exceeding 60rad/s) is added to the gain plot (see Figure 4-20b). To meet the stability criteria mentioned in section 4.3 (in which the gain margin (GM) and the phase margin (PM) of the compensated open-loop systems are required to be within the ranges GM >= 6dB and PM >=40° respectively), a set of PI parameters are selected. Using the PI compensator designed in Figure 4-20c, these transfer functions yield a phase margin of better than about 62° at a gain cross-over frequency of about 7.46 rad/s (a little bit lower than the first dip in the magnitude plot that is actually a zero caused by DC link) and a gain margin better than about 27 dB (see Figure 4-20d). This suggests that the corner frequency may exceed the frequency where zero occurs, which is caused by the dynamics of the DC link, and may cause an inadequate performance or even instability due to the ignored dynamics, therefore the dynamics of DC link should be considered in the controller design.
Figure 4-20 The Bode plots with (a) low-pass filter; (b) DB current controlled VSC with a low-pass filter; (c) designed PI compensator; (d) open loop transfer function of $P(s)/P_{ref}(s)$.

The closed loop responses of $P(s)/P_{ref}(s)$, including all 36 loading scenarios being subject to a 1pu step change in the power reference are employed to evaluate the performance of the designed power controller which is given in Figure 4-21.

Figure 4-21 Step responses of $P(s)/P_{ref}(s)$
CHAPTER 4: CONTROLLER DESIGN FOR VSC-HVDC CONNECTED TO A WEAK AC GRID

Not that the responses are satisfactory as they settle to within ±2% of the final value at about 0.506s (the maximum settling time for the entire transfer functions). The overshoot (height of peak relative to the final value) is about 4.35% which is within the acceptable range (< 10%) suitable for the reference tracking.

b) Small Signal Model of Power Controller

Figure 4-22 shows the control block diagram of the power controller, where \( \Delta P_m \) denotes the measured value of power and \( \Delta P_x \) represents the power state. \( T_{f,p}, K_{p,p} \) and \( K_{i,p} \) denote the control parameters derived from the previous sub-section. Hence, the corresponding small signal model is given by the below equations.

\[
\frac{d\Delta P_f}{dt} = \frac{\Delta P_{ref} - \Delta P_m - \Delta P_f}{T_{f,p}} \quad (4-8)
\]

\[
\frac{d\Delta P_x}{dt} = K_{i,p} \cdot \Delta P_f \quad (4-9)
\]

\[
\Delta i_{qref} = K_{p,p} \cdot \Delta P_f + \Delta P_x \quad (4-10)
\]

Figure 4-22 Control block for the power controller

4.3.3.4 AC Voltage Controller Design for the Rectifier and its Small Signal Model

Note that the power control loop should be taken into account when designing the AC voltage controller to improve the accuracy.

Figure 4-23 A typical MIMO system, in which the hidden feedback loop is shown in red lines
4.3. Controller Design Methodology

Figure 4-23 shows the typical multi-in multi-out (MIMO) system, where \( G_{p11}, G_{p22} \) are two main inner loops, while \( G_{p12}, G_{p21} \) denote the transfer functions of two cross-coupling loops, and \( G_{c1}, G_{c2} \) represents the transfer functions of two outer loops. In addition, \( Y_{sp1}, Y_{sp2} \) are inputs of the outer-loops, while \( U_1(s) \) and \( U_2(s) \) are the outputs of the outer-loops and the inputs to the inner loops and \( Y_1, Y_2 \) are the outputs of the MIMO system.

The closed-loop transfer function of the output \( Y_1(s) \) to the input \( Y_{sp1}(s) \) can be given by,

\[
Y_1(s) \over U_1(s) = G_{p11} \tag{4-11}
\]

For simplicity purpose, all the \((s)\) are ignored in the following analysis. Hence, the following equations can be given.

\[
Y_1 = U_1 \cdot G_{p11} + U_2 \cdot G_{p12} \tag{4-12}
\]

\[
U_2 = (Y_{sp2} - Y_2) \cdot G_{c2} \tag{4-13}
\]

\[
Y_2 = U_1 \cdot G_{p21} + U_2 \cdot G_{p22} \tag{4-14}
\]

Rearranging equation (4-14), we can obtain

\[
Y_2(1 + G_{c2} \cdot G_{p22}) = U_1 \cdot G_{p21} + Y_{sp2} \cdot G_{c2} \cdot G_{p22} \tag{4-15}
\]

And assuming \( Y_{sp2} = 0 \),

\[
Y_2 = \frac{U_1 \cdot G_{p21}}{1 + G_{c2} \cdot G_{p22}} \tag{4-16}
\]

Substituting (4-16) into equation (4-13),

\[
U_2 = -Y_2 \cdot G_{c2} = -\frac{G_{c2} \cdot G_{p21}}{1 + G_{c2} \cdot G_{p22}} \cdot U_1 \tag{4-17}
\]

Similarly, substituting equation (4-17) into equation (4-12), we can obtain

\[
Y_1 = U_1 \cdot G_{p11} - \frac{G_{c2} \cdot G_{p21} \cdot G_{p12}}{1 + G_{c2} \cdot G_{p22}} \cdot U_1 \tag{4-18}
\]

\[
Y_1 = (G_{p11} - \frac{G_{c2} \cdot G_{p21} \cdot G_{p12}}{1 + G_{c2} \cdot G_{p22}}) \cdot U_1 \tag{4-19}
\]

Without considering the feedback loop in red in Figure 4-23, which means leaving the outer loop appended, then the transfer function becomes,
\[ Y_i = G_{p_{11}} U_i \]  \hspace{1cm} (4-20)

By comparing equation (4-19) and equation (4-20), we can come to the conclusion that that to involve the power controller in the model can achieve a more precise basement for AC voltage controller design.

**A. AC Voltage Controller Design**

Using the methodology proposed in section 4.3.3.3 for power controller design, the first step is to choose the baselines for controller design. Scenarios 3, 7, 9 and 36 (i.e. \( P_{\text{max}} Q_{\text{max}} \), \( P_0 Q_{\text{max}} \), \( P_0 Q_{\text{min}} \) for SCR=2 with angle 90° and \( P_0 Q_{\text{min}} \) for SCR=7.5 with angle 75°) are chosen in this study as shown in Figure 4-24.

![Figure 4-24 Bode plots of selected cases in the AC voltage controller design](image)

\[ \text{Frequency response of } U_{f_{\text{sec}}}(s)/I_{d_{\text{ref}}}(s) \text{-open loop} \]
4.3. **Controller Design Methodology**

Figure 4-25 The Bode plots of (a) low-pass filter; (b) $U_f(s)/I_{dref}(s)$ of DB current controlled VSC with a low-pass filter; (c) the designed PI compensator and (d) open loop transfer function of $U_f(s)/U_{fref}(s)$ at the rectifier side.

Similar to the power controller design, a first-order low-pass filter (see Figure 4-25a) is added to the system to provide an additional attenuation that 20dB/decay which rolls off when exceeding 133.33rad/s (see Figure 4-25b). Then a set of PI parameters $K_p=0.0314252$ and $K_i=1.575$ are chosen, which yield a phase margin of better than about 60.9 degree at a gain cross-over frequency of about 41.7 rad/s and a gain margin better than about 9.6 dB (see Figure 4-25d). The closed-loop responses of $U_f(s)/U_{fref}(s)$ (including all 36 scenarios) being subject to a 1pu step change in the AC voltage reference are employed to evaluate the performance of the designed AC voltage controller as shown in Figure 4-26.
CHAPTER 4: CONTROLLER DESIGN FOR VSC-HVDC CONNECTED TO A WEAK AC GRID

Figure 4-26 Step responses of \( U_f(s) / U_{\text{ref}}(s) \)

Note that the simulation results of the step change responses demonstrate a satisfactory performance, since it settles to the final value within ±2% until after 0.336s and with a maximum overshoot of 9.91% (better than the basic requirement 10%).

B. Small Signal Model for AC Voltage Controller

The block diagram of the AC voltage controller is shown in Figure 4-27. The error of the reference value \( \Delta U_{\text{ref}} \) and the measured value \( \Delta U_m \) of the AC voltage go through a low pass filter \( 1/(1+T_{\text{U},uc} \cdot s) \), followed by a PI compensator \( (K_{P,\text{U}} + K_{I,\text{U}} / s) \). Finally, the current reference of the reactive power loop \( \Delta i_{\text{ref}}(s) \) is obtained according to equation (4-23). The small signal model of the AC voltage controller is given by the equations (4-21) - (4-23).

\[
\frac{d\Delta U_{f-f}}{dt} = \frac{\Delta U_{\text{ref}} - \Delta U_m - \Delta U_{f-f}}{T_{\text{U},uc}} \quad (4-21)
\]

\[
\frac{d\Delta U_{\phi}}{dt} = K_{I,\text{U}} \cdot \Delta U_{f-f} \quad (4-22)
\]

\[
\Delta i_{\text{ref}} = K_{P,\text{U}} \cdot \Delta U_{f-f} + \Delta U_{\phi} \quad (4-23)
\]

4.3.4 Controller Design for Inverter

After designing the controllers for the rectifier converter, it is time to design the DC voltage controller and the AC voltage controller for the inverter. However, since the controllers designed for the rectifier converter in the above sections are also being included in the complete model, it is important to understand how the operating points of the rectifier side converter can affect the inverter side controller-design.
Figure 4-28 The frequency responses of (a) \(\frac{U_{dc}(s)}{I_{qref}(s)}\); (b) \(\frac{U_{dc}(s)}{I_{dref}(s)}\); (c) \(\frac{U_{f\text{_inv}}(s)}{I_{q\text{_ref}\text{_inv}}(s)}\) and (d) \(\frac{U_{f\text{_inv}}(s)}{I_{d\text{_ref}\text{_inv}}(s)}\) being subject to the operating point variation of the rectifier side converter (36 scenarios), but with a constant operating point at the inverter side converter that is \(P_{\text{max}}Q_0\), \(\text{SCR}=2\) and with angle equals to 90°.

Note that 36 operating points are considered in the controller design for the rectifier. However, it is not feasible to consider 36 operating points for both of the inverter and rectifier operating points together (36²) when designing an inverter side controller. Therefore, to reduce the number of the total operating points considered it is necessary to examine the sensitivity of the transfer functions for a given frequent operating point of the inverter first. In such an approach, if the sensitivity is less, any operating point can be chosen as a base operating point for further controller design, normally the most frequent operating point is chosen as the base scenario. In such a case, only 36 inverter side operating points are considered, which significantly reduce the initial total number 36².

Figure 4-28 shows the frequency responses of the transfer functions \(\frac{U_{dc}(s)}{I_{qref}(s)}\), \(\frac{U_{dc}(s)}{I_{dref}(s)}\), \(\frac{U_{f\text{_inv}}(s)}{I_{q\text{_ref}\text{_inv}}(s)}\) and \(\frac{U_{f\text{_inv}}(s)}{I_{d\text{_ref}\text{_inv}}(s)}\) which correspond to the 36
operating point variations of the rectifier. In this figure, a constant operating point of the inverter \((P_{\text{max}}, Q_{\text{b}}, \text{SCR}=2, 90^\circ \text{angle})\) is assumed. Note that no significant discrepancies are observed in the results of the two main loops up to 100 rad/s (Figure 4-28a, d). However, results are found to be different in the cross-coupling loops (Figure 4-28b, c). This indicates that the outer loop controllers for the main loops need a careful design approach to minimize the cross-coupling effects. Anyhow, it can be concluded that the sensitivity of the transfer functions of operating points is low, in fact, of which the impact can be ignored for simplification purpose. Therefore, based on this assumption, only a single frequent operating point \((P_{\text{max}}, Q_{0}, \text{SCR}=2, 90^\circ \text{angle})\) is sufficient for the base scenario of the rectifier.

It should be emphasized that the VSC losses are not considered in the small signal model. However, the VSC losses cause inaccuracies in the steady state calculation. This results in a minor power imbalance further causing minor inaccuracies in the filter bus voltage. Consequently, the DC voltage also becomes inaccurate, since the calculated DC voltage is utilized rather than the real DC transmission line feedback data in modeling of the control system. This approach avoids the potential problems caused by the feedback dynamics of the transmission line which can complicate the calculation process. Although the above approach reduced the accuracy of the model, the deviation in the final results is found small once the loops of the entire system are closed.

### 4.3.4.1 DC Voltage Controller Design for the Inverter and its Small Signal Model

Figure 4-29a shows the frequency responses of the selected cases in the DC voltage controller design. By employing the compensator shown in Figure 4-29b, it can be predicted that a satisfactory performance can be achieved when being subject to a step change in the DC voltage reference (see Figure 4-29d) based on the analysis of the Bode plots of the compensated system (see Figure 4-29c).

By testing the frequency response for all 36 scenarios, it is found that the system using the designed controller yields a phase margin of better than 85.9 degree at a gain crossover frequency of about 9.71 rad/s and a gain margin of better than 24.3 dB (see Figure 4-29c). Furthermore, the results of the step response tests reveal that a fairly low maximum overshoot 1.89% (at t=0.212s) is obtained in the scenario that \(P_{\text{min}}Q_{\text{min}}, \text{SCR}=2\) and angle \(\varphi=90^\circ\). In addition, a satisfactory maximum settling time at t=0.532 is obtained at the scenario that \(P_{\text{min}}Q_{\text{max}}, \text{SCR}=7.5\) and angle \(\varphi=90^\circ\).
4.3. CONTROLLER DESIGN METHODOLOGY

Figure 4-29 (a) The Bode plots of the selected cases of the DC voltage controller design $U_{dc}(s)/I_{qref\_inv}(s)$; (b) designed PID compensator $(K_{p\_dc} + K_{i\_dc}/s + K_{d\_dc} \cdot s/(1+T_{fUdc} \cdot s)) = -0.024 - 0.088/s + 0.0009 \cdot s/(1+0.06 \cdot s)$; (c) frequency responses of open loop transfer functions of $U_{dc}(s)/U_{dc\_ref}(s)$ and (d) step responses of the closed-loop $U_{dc}(s)/U_{dc\_ref}(s)$.

The control block diagram of the DC voltage controller is shown in Figure 4-30 and its small signal model is given by equation (4-24).

![Control Block Diagram](image)

Figure 4-30 The control block diagram of the DC voltage controller
\[
G_{pid}(s) = K_p + K_i/\tau + K_d \cdot s / (1 + T_f \cdot s) \\
\frac{(K_p \cdot T_f + K_d) \cdot s^2 + (K_p + K_i \cdot T_f) \cdot s + K_i}{T_f \cdot s^2 + s} \tag{4-24}
\]

For facilitating the derivation of the state space equations, it can be written as a second-order transfer function as given in equation (4-24).

If we substitute the values \(A = K_p \cdot T_i + K_d\); \(B = K_p + K_i \cdot T_f\); \(C = K_i\); \(D = T_f\); \(E = 1\) and \(F = 0\) into equation (4-24), the general form of the second order form transfer function can be given by

\[
G_{pid}(s) = \frac{A \cdot s^2 + B \cdot s + C}{D \cdot s^2 + E \cdot s + F} \tag{4-25}
\]

The state space equation for a general form second order transfer function can be given by

\[
\frac{d}{dt} \begin{bmatrix} w_{d1} \\ w_{d2} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-F}{D} \\ 1 & \frac{-E}{D} \end{bmatrix} \begin{bmatrix} w_{d1} \\ w_{d2} \end{bmatrix} + \begin{bmatrix} \frac{C}{D} - \frac{AF}{D} \\ -AE/B + \frac{AE}{D} \end{bmatrix} \cdot u_d \\
\begin{bmatrix} y_d \end{bmatrix} = \begin{bmatrix} 1 \\ \frac{1}{D} \end{bmatrix} \begin{bmatrix} w_{d1} \\ w_{d2} \end{bmatrix} + \frac{A}{D} \cdot u_d \tag{4-26}
\]

Hence, if by i) substituting two states of the general form of the second order transfer function \(w_{d1}\) and \(w_{d2}\) with \(\Delta U_{dx1}\) and \(\Delta U_{dx2}\); ii) relacing \(u_d\) with \(\Delta U_{dcref} - \Delta U_{dcm}\) and iii) substituting \(y_d\) with \(\Delta i_{qref}(s)\), the small signal for the DC-PID controller can be obtained as

\[
\frac{d}{dt} \begin{bmatrix} \Delta U_{dx1} \\ \Delta U_{dx2} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-F}{D} \\ 1 & \frac{-E}{D} \end{bmatrix} \begin{bmatrix} \Delta U_{dx1} \\ \Delta U_{dx2} \end{bmatrix} + \begin{bmatrix} \frac{C}{D} - \frac{AF}{D} \\ -AE/B + \frac{AE}{D} \end{bmatrix} \begin{bmatrix} \Delta U_{dcref} \\ \Delta U_{dcm} \end{bmatrix} \\
\Delta i_{qref} = \begin{bmatrix} 0 \\ \frac{1}{D} \end{bmatrix} \begin{bmatrix} \Delta U_{dx1} \\ \Delta U_{dx2} \end{bmatrix} + \begin{bmatrix} \frac{A}{D} \\ -\frac{A}{D} \end{bmatrix} \begin{bmatrix} \Delta U_{dcref} \\ \Delta U_{dcm} \end{bmatrix} \tag{4-27}
\]

### 4.3.4.2 AC Voltage Controller Design for Inverter and its Small Signal Model

Note that the model used in the AC voltage controller design is a MIMO model by placing the designed rectifier side power controller, AC voltage controller and the inverter side DC voltage controller in service. This approach ensures the design is more accurate
since the impacts of the dynamics of the co-operating controllers are also being taken into account.

![Bode plots of selected cases for inverter end AC voltage controller design](image)

**Figure 4-31(a)** Bode plots of selected cases for inverter end AC voltage controller design $U_{f_{\text{inv}}}(s)/I_{\text{ref}_{\text{inv}}}(s)$; (b) designed filter+PI compensator; (c) frequency responses of open loop transfer functions of $U_{f_{\text{inv}}}(s)/U_{f_{\text{inv}}_{\text{ref}}}(s)$; (d) step responses of closed-loop $U_{f_{\text{inv}}}(s)/U_{f_{\text{inv}}_{\text{ref}}}(s)$.

The same methodology is used in this controller design as proposed earlier in section 4.3.3.3 and shown in Figure 4-31a. Using the loop-shaping technique, a set of PID parameters ($K_{p_{\text{f_{Uf_{inv}}}}}=0.00842$, $K_{i_{\text{f_{Uf_{inv}}}}}=0.752$, $K_{d_{\text{f_{Uf_{inv}}}}}=8.9\times10^{-5}$ and $T_{f_{\text{Uf_{inv}}}}=0.018$) are selected for the PID compensator. The frequency responses of the designed AC voltage...
controller is shown in Figure 4-31b, and the compensated system is shown in Figure 4-31c. Note that, the AC voltage loop yields a phase margin of better than $63.2^\circ$ at a gain crossover frequency of 27.3 rad/s and a gain margin better than 17.8 dB.

The small signal model with respect to the AC voltage is similar to the method explained earlier in section 4.3.4.1. Figure 4-31d shows the step test responses of the system operating under 36 different scenarios following a 1pu step change in the reference value of the filter bus voltage. A satisfactory performance is obtained with a maximum rise time of 0.404s (reaching to 90% of the final value). In addition, a settling time of better than 0.73s is obtained in the STATCOM mode in which VSC is embedded in a strong system which is represented as an inductance in series with a resistance. Moreover, a maximum overshoot of 7.02% is also obtained within the satisfactory range.

### 4.3.5 Cross-Coupling Effects Examination

So far, all the initial values of the four controllers of the converters are designed individually without taking into account the dynamic behaviours of the integrated system. Therefore, it is important to examine the behaviours of the main loops as well as the cross-coupling loops.

#### 4.3.5.1 Controllers for Rectifier

Two tests are considered to examine the controllers, which are i) for the rectifier: 1% step change in the filter bus AC voltage reference and ii) 1% step change in the power reference.

The results given in Figure 4-32 and Figure 4-33 indicate that there is a fairly short transient change less than 0.4s maximum in the power plots (see Figure 4-32a). Note that 1% AC voltage reference step change causes a comparable change (maximum 0.686%) in the power plot, which might be a concern. Although the change disappears quickly (reducing to 1/3 in 0.1s), it should be treated as a not insignificant variation. However, considering the responses of the power reference step change, the resulted AC voltage change is found to be very small (see Figure 4-33, b). It should be noted that the levels of the cross-coupling effects observed in the above mentioned two step test are remarkably different. Note that a certain cross-coupling effects are also observed between the power and the DC voltage, but this will not significantly affect the AC grid. It was observed that 10% change in the power reference causes 2.23% increase in the DC voltage response in
which half of the DC voltage step change occurred within a short time 0.5s. It can be concluded that the cross-coupling effects between the power and the AC voltage induced by changing the power reference are low. However, the cross-coupling effects between the rectifier side AC voltage and the power or DC voltage caused by changing the voltage reference are not insignificant, which is noticeable.

Figure 4-32 1% step of AC voltage reference at the rectifier end; (a) responses of power at the rectifier end; (b) responses of the filter bus voltage $U_{f\_rec}$ at the rectifier end; (c) responses of DC voltage $U_{dc\_inv}$ at the inverter end; (d) responses of the filter bus voltage $U_{f\_inv}$ at the inverter end.
Figure 4-33 1% step of power reference at the rectifier end; (a) responses of the power at the rectifier end; (b) responses of the filter bus voltage $U_{\text{f,rec}}$ at the rectifier end; (c) responses of the DC voltage $U_{\text{dc,inv}}$ at the inverter end; (d) responses of the filter bus voltage $U_{\text{f,inv}}$ at the inverter end.

### 4.3.5.2 Controllers for Inverter

Two tests are also considered for the inverter side controllers, which are i) 1% step change in the filter bus AC voltage reference and ii) 1% step change in the DC voltage reference.

The simulation results shown in Figure 4-34 and Figure 4-35 indicate that only a small magnitude change is observed in the induced DC step voltage during transients. Although, it recovers slowly only the DC side is affected, which is not so significant for a point to point VSC-HVDC transmission link. If there has to have any cross-coupling in the system, the cross-coupling in terms of DC voltage is desirable since it is the least important.
4.3. **Controller Design Methodology**

coupling. Although it is not the case in a DC meshed power grid, this is beyond the scope of this research. The peak of the DC voltage transient is found to be about 5 times less than the AC voltage change, and the rising time is less than 0.05s. In addition, it settles down to half of the change in less than 0.5s, which are all satisfactory.

![Figure 4-34](image)

Figure 4-34 1% Step of the AC voltage reference at the inverter end: (a) response of the power at the rectifier end; (b) response of filter bus voltage $U_{f, rec}$ at the rectifier end; (c) response of the DC voltage $U_{dc, inv}$ at the inverter end and (d) response of the filter bus voltage $U_{f, inv}$ at the inverter end.
Figure 4-35 1% step of the DC reference voltage at the rectifier side; (a) the responses of power at the rectifier; (b) the responses of the filter bus voltage $U_{f_{rec}}$ at the rectifier; (c) the responses of the DC voltage $U_{dc_{inv}}$ at the inverter end; (d) the responses of the filter bus voltage $U_{f_{inv}}$ at the inverter end.

By observing Figure 4-35d, it is found that the 1% step change in the DC voltage reference results in about 0.196% change in the AC voltage which is not quite satisfactory but acceptable. However, the cross-coupling effects can be improved by further slowing down the DC voltage controller through multiplying the controller coefficient with a gain less than 1 (e.g. 0.8), but at cost of reducing the response speed of the DC voltage controller. Moreover, further reducing the speed of the AC voltage controller can also provide another alternative solution to reduce the cross-coupling effects.

From the above analysis, it can be concluded that the overall performance of the system controllers’ behaviour is a trade-off between the primary controller performance...
and the cross-coupling effects. In other words, a better cross-coupling effect can be achieved by slowing down the primary controller, meanwhile the performance of the primary controllers have to be ensured as well. This requires further fine tuning of the controller parameters by iterating the controller design procedure to get the final desirable control system. Also, the root locus analysis and PSCAD simulation verifications can also assist in tuning such controllers.

**4.3.5.3 Analytical Model Verification against Detailed Nonlinear Simulation**

It is well known that the small signal models are only accurate around a certain operating points. Therefore the analytical model verification against detailed nonlinear simulation (such as PSCAD) is always required.

Since 36 operating scenarios are involved in this research, the bunch file simulations are required. However, PSCAD is only applicable for a single case simulation. The Multi-run block of PSCAD is also not applicable for this particular application. Hence, a self-defined ‘multi-study’ component needs to be developed to successively read the input data from a text file. The procedures for the PSCAD verification is given below,

- Compute grid operating points and generate a text file containing these data points in a form that is suitable as an input to PSCAD.
- Create a “multi-study” component that will read a file from an input file, and read the operating-point values of the system successively from the above file, and modify grid impedance, and set control input references accordingly.
- Generate a separate Matlab readable output file for each simulation.
- Proceed the simulation results in Matlab for comparison of PSCAD results with the small signal model at various step sizes, operating points and SCRs.

Performing the step tests for 36 operating points and with different step sizes, it is found that the developed small single model is accurate enough to capture the main characteristics of the system model developed in PSCAD. It was also observed that the developed small signal model can be used as a powerful tool for controller design as well as in the small signal stability analysis of the system. However, due to the space limitations, for verification purpose, the results are only given for two operating points of the inverter: i) $P_{\text{max}}Q_{\text{max}}$, SCR=2 with $\varphi=90^\circ$ and ii) $P_0Q_{\text{min}}$, SCR=7.5 with $\varphi=75^\circ$ for various step size changes of 1%, 2%, 4% and 8%.
Figure 4-36 shows the closed-loop responses of the complete control system, under the step size changes of 1%, 2%, 4% and 8% of the reference value of the inverter side filter bus voltage (Figure 4-36 a) and the DC voltage (Figure 4-36b). As it can be seen in the figure the inverter side filter bus voltage results obtained from both of the small signal and the non-linear model match very well with each other. Although some minor errors are observed in the cross-coupling loops at the rectifier side, the small signal model does capture the main characteristic of the system. It can be deduced that the errors may be due to the inaccuracy introduced during the calculation process of the steady-state value, since the losses on both side of the converters are not included. However, the level of error is acceptable and cannot significantly affect the controller design.
Figure 4-36 The step responses of $U_{\text{finv\_ref}}$ (a) and $U_{\text{dcinv\_ref}}$ (b) and their induced performances in their cross-coupling loops as the system working at an operating point $P_{\text{max}}, Q_{\text{max}}, \text{SCR}=2$ with $\phi=90^\circ$. red: Matlab 1%; cyan: PSCAD 1%; black: PSCAD 2%/2; magenta: PSCAD 4%/4; green: PSCAD 8%/8.

Figure 4-37 is another step test performed in the STATCOM mode. Firstly, a 1% step change is applied to the small signal model of the inverter side DC voltage reference, which is then compared with four results from the detailed PSCAD non-linear model. The testes set on PSCAD include 1%, 2%, 4% and 8% step changes on both of the AC filter bus reference voltage and the DC reference voltage. While, the final output results are manipulated by dividing 1, 2, 4 and 8 respectively. To do in such a way is to examine the linearity of the PSCAD model. The results especially forcefully confirm the accuracy of the developed small signal model.
Figure 4-37 The step responses of $U_{dcinv_{ref}}$ (a) and $U_{finv_{ref}}$ (b) and their induced performances in their cross-coupling loops as the system working at an operating point $P_0Q_{min}$, $SCR=7.5$ with $\varphi=75^\circ$. red: Matlab 1%; cyan: PSCAD 1%; black: PSCAD 2%/2; magenta: PSCAD 4%/4; green: PSCAD 8%/8.
4.4 Discussions and Conclusions

In summary, the main focus of this chapter is to design three different types of outer loop controllers i) power controller, ii) AC voltage controller and iii) DC voltage controller for a VSC-HVDC system. First of all, the causes of the failure operation of a VSC-HVDC current controller in weak AC grids are examined and it is found that the limited bandwidth of the system results in the main challenges of such application. Then, the selected parameter sensitivity (such as SCRs, X/R ratios, loading conditions and power factors) effects on the main and cross-coupling inner current loops are discussed. In addition, the limitations imposed by the RHP zero on the bandwidth of the outer loop controllers are also investigated and discussed. The study and resolution of these issues provided an in-depth understanding on the characteristics of the plant to be controlled and facilitate a more precise controller design.

It is known that one of the drawbacks of the controller design using a simplified model is the dynamics of the PLL and the filter bus voltage with respect to the entire system performance are not considered. The secondary drawback is that it does not take into account the operating points of the system. Therefore, to implicitly understand the operation of the VSCs working in weak AC grids, it is crucial to carry out a complete analysis using an accurate representation of the nonlinearities of the PLL, controllers and the network. Therefore, a robust controller design methodology was firstly proposed in this chapter by taking into account a set of operating points covering the converter operating capability (PQ chart) and the various grid conditions in terms of different SCR and X/R ratios of the grid reactances. In general in this chapter it is stated each part of the control design is better if it is done with the previously designed controller in place. While, if unsatisfactory performance were observed of the earlier designed controller when the later controllers were implemented, it can be re-designed to obtain better performance. By going through several iteration design process, we can definitely get controllers with improved performance.

The initial value of the controller is obtained by applying the classical frequency response technique to a set of open-loop transfer functions of the VSC-HVDC systems which are obtained by changing the operating points of the developed small signal model in Chapter 3. This technique is applied to power, AC voltage and DC voltage controller design respectively. It should also be emphasized that it is more accurate to design a
controller with the previous designed controller in service, since the more detailed model employed will result in a more accurate design for the later controller. In addition, such approach also allows the cross-coupling effects to be considered.

Finally, a self-defined block is developed in PSCAD to enable the successive PSCAD simulations for verification purpose. The co-operating performance of the various designed controllers are examined against the time domain verification. It is found that the designed power and voltages controllers work very well within all the considered 36 operating points.
Chapter 5: Stability of VSC-HVDC Links Embedded with the Weak Australian Grid

This chapter evaluates the small signal stability performance of an expanded Australian grid, in which the DB current controlled VSC-HVDC stations are embedded in parallel with the existing longitudinal and weak Australian AC grid. In this study, it was found that the introduction of the new source of geothermal power generation has an adverse impact on the damping performance of the system. Therefore, this chapter aims to answer how a VSC-HVDC system can assist in enhancing the system small-signal rotor-angle stability in a weak multi-machine system.

5.1 Introduction

As is known, the limited availability and environmental concern of fossil fuels, as well as the continuous growing demand of electricity, have caused renewable energy to become commercially attractive. Meanwhile, as a result of increasing greenhouse gas emissions, the Australian government has announced an emissions trading scheme in 2010 termed as the Carbon Pollution Reduction Scheme [142] and setup new green energy targets to
increase the share of renewable and sustainable electricity generation from 2% in 2004-05 [143] to 20% in 2020 [142].

Among all the potential renewable energy sources, geothermal as a zero-emission, base load renewable source of electricity, wind and solar energies as environmental friendly resources offer attractive solutions to long term CO2-e emission reduction scheme. However, the large-scale integration of renewable energies poses significant challenge on the existing shared transmission systems, especially in Australia where the grid is one of the world’s longest interconnected power systems between Port Douglas of Queensland and Port Lincoln of South Australia with an end-to-end distance of more than 4000 km as shown in Appendix E [144]. In addition, the potential Paralana Geothermal source is located very remote from the existing shared transmission network. There are several investigations [145-147] on exploring the potential network extension solution upon integrating the staged Innamincka generation of 500MW, 2000MW and 5000MW [145, 146].

This chapter examines the small signal stability performance of this potential extended Australian grid using an alternative HVDC transmission solution assuming that a 2000MW capacity is available at Innamincka. It is assumed that the generation 200MW is consumed locally, and the remaining 1200MW is delivered via a ± 500kV, 1100km, bi-pole VSC-HVDC links to Armadale converter substation located at the half way between Queensland and New South Wales. It is considered that this arrangement can make full utilization of the existing transmission corridor, consequently benefiting both States. The remaining 600 MW are transferred to Roxby Down from Innamincka, using the 490km 275kV transmission line, and then being integrated to the main grid at Port Augusta by a 290km transmission line. The proposed diagram of the extended South-East Australian power system with VSC-HVDC links is illustrated in Figure 5-1, which is obtained based on an IEEE 14 generator 59 bus test system. The test system represents a simplified model of the Southern and Eastern Australian network which is composed of five areas in which 14 large generators and 5 static var compensators (SVCs) are involved. The data for this system is available in [148]. Comparing with the other possible solutions, it is considered that this approach is a realistic option and will be investigated here.
5.2 Preparation Tasks for Interconnection

This study considers the VSC-HVDC small signal model developed in Chapters 3 and 4. However, for the purpose of obtaining a high accuracy of VSC controllers design, a dynamic model is utilized to represent the interconnected simplified grid model which is...
represented by a source behind impedance or with additional resistance depending on system short circuit ratio (SCR) and X/R ratio. Nevertheless, the frequency range of interest in this study is the modal frequency related to electromechanical oscillations which is more likely encountered in practice i.e. from low frequency inter-area mode of 1.5 rad/s to higher local frequencies of 12 rad/s [148]. Therefore, it is necessary to test whether it is appropriate or not to represent the interconnected grid and PCC bus filter as an admittance matrix within the frequency range of interest.

It should be noted that it is insufficient to employ the constant admittance representation of grid for torsional oscillations in HVDC interactions studies, since the frequency of interest in this application is much higher. In [149], a “hybrid model” was proposed to offer a feasible solution to this problem. It is realized by including the detailed dynamics of the transmission network and dynamic devices in adjacent area of HVDC converters and the remanent parts are modelled as constant admittances in the modeling. It should be noted that this approach not only ensures sufficient the accuracy, while offers the simplicity as well. Therefore, the simplification process of the grid and filter dynamic model will be conducted step by step in the following section to validate the above mentioned approach.

5.2.1 Admittance Matrix Representation of the Integrated Grid and Filter

The representation of the grid dynamic model as an admittance is shown in Figure 5-2. For the explanation of the symbols, refer to Figure 3-1.

Hence, the grid impedance dynamic model can be given by the below set of equations,
\[
\begin{align*}
\frac{dE_{g,R}}{dt} &= \left(1/L_g\right)E_{g,R} - \left(1/L_g\right)u_{f,R} - \left(R_g/L_g\right)i_{g,R} + \omega L i_{g,l}, \\
\frac{dE_{g,I}}{dt} &= \left(1/L_g\right)E_{g,I} - \left(1/L_g\right)u_{f,I} - \left(R_g/L_g\right)i_{g,I} - \omega L i_{g,R} \\
\end{align*}
\]

which can be replaced with a grid admittance model and resulting in the following set of equations,

\[
\begin{align*}
i_{g,R}^g &= \frac{(E_{g,R} - jE_{g,I}) - (u_{f,R} + ju_{f,I})}{R_g + jX_g} \\
i_{g,I}^g &= \frac{(E_{g,R} - u_{f,R}) \cdot R_g + (E_{g,I} - u_{f,I}) \cdot X_g + j(E_{g,R} - u_{f,R}) \cdot X_g + (E_{g,I} - u_{f,I}) \cdot R_g}{R_g^2 + X_g^2}
\end{align*}
\]

In the above equations (5-2), the real part of the grid current \(i_{g,R}^g\) and the imaginary part of the grid current \(i_{g,I}^g\) can be expressed by the following set of equations,

\[
\begin{align*}
i_{g,R}^g &= \frac{(E_{g,R} - u_{f,R}) \cdot R_g + (E_{g,I} - u_{f,I}) \cdot X_g}{R_g^2 + X_g^2} \\
i_{g,I}^g &= \frac{-(E_{g,R} - u_{f,R}) \cdot X_g + (E_{g,I} - u_{f,I}) \cdot R_g}{R_g^2 + X_g^2}
\end{align*}
\]

After linearizing the above equations (5-3), the small signal model for the admittance representation of the grid model can be given by

\[
\begin{align*}
\Delta i_{g,R}^g &= \frac{R_g}{R_g^2 + X_g^2} \cdot (\Delta E_{g,R} - \Delta u_{f,R}) + \frac{X_g}{R_g^2 + X_g^2} \cdot (\Delta E_{g,I} - \Delta u_{f,I}) \\
\Delta i_{g,I}^g &= -\frac{X_g}{R_g^2 + X_g^2} \cdot (\Delta E_{g,R} - \Delta u_{f,R}) + \frac{R_g}{R_g^2 + X_g^2} \cdot (\Delta E_{g,I} - \Delta u_{f,I})
\end{align*}
\]

Figure 5.3 shows the simulation results of the dynamic and the admittance representation of the grid model following a 1% step change on the inverter side input DC voltage reference. As it can be seen in the figure, the responses of the DC voltage tracking and the cross-coupled rectifier side power responses are similar. However, the cross-coupling voltage responses in the rectifier and the inverter side have some minor differences which can be ignored, as highlighted by the circled areas in the graphs.
Figure 5-3 1% DC voltage step responses of the dynamic and grid admittance models (a) for rectifier side; (b) for inverter side.
Figure 5-4 illustrates the relationship of the system variables, where the grid and filter models are represented as admittances, which can be given by the set of equation (5-5). Firstly, the grid source supplies the filter bus voltages $u_{fr}^g$, $u_{fl}^g$ to the converter based on the first equation of the set of equations (5-5). In accordance with these voltages, the filter generates the output currents that $I_{fr}^g$ and $I_{fl}^g$ according to the third equation of the set of equation (5-5). Further, the converter output currents $I_{fr}^g$ and $I_{fl}^g$ can be calculated with regards to the voltage drop across the converter reactance (i.e. $u_{fr}^g - V_{cr}^g$ and $u_{fl}^g - V_{cl}^g$). Finally, obtain the injected currents to the grid source $I_{gR}^g$ and $I_{gI}^g$ according to the second equation of the set of equation (5-5).

\[
\begin{aligned}
\bar{u}_f^g &= \frac{\Delta E^g}{Z_g^g} - \Delta I_f^g \\
\bar{I}_g^g &= \bar{I}_f^g + \bar{I}_c^g \\
\bar{I}_f^g &= \bar{u}_f^g \cdot B_f j
\end{aligned}
\]  
(5-5)

If this set of equations (5-5) is expended and linearized, the small signal model of the filter and grid admittance representation of the system model can be obtained as,

\[
\begin{aligned}
\Delta u_{f-R}^g &= E_{g-R}^g - R_{g-R} \Delta I_{g-R}^g + X_g \Delta I_{g-I}^g \\
\Delta u_{f-I}^g &= E_{g-I}^g - R_{g-I} \Delta I_{g-I}^g - X_g \Delta I_{g-R}^g \\
\Delta I_{g-R}^g &= \Delta I_{f-R}^g + \Delta I_{c-R}^g \\
\Delta I_{g-I}^g &= \Delta I_{f-I}^g + \Delta I_{c-I}^g \\
\Delta I_{f-R}^g &= -\Delta u_{f-I}^g \cdot B_f \\
\Delta I_{f-I}^g &= \Delta u_{f-R}^g \cdot B_f
\end{aligned}
\]  
(5-6)-(5-8)
Figure 5.5 1% DC voltage step response comparison of the admittance representation of grid model only, and the grid and filter models adopting admittance representation: (a) the rectifier side; (b) the inverter side.
The test results presented in Figure 5-5 reveal that the further simplification of the filter model does not weaken the accuracy of the results in this application. Hence, the admittance representation of both the grid and the filter models will be set as the standard modelling methodology in the following analysis.

5.2.2 Scaling the Existing System

The model developed in chapters 3 and 4 was in SI system. This section will show how to scale the existing system to make it applicable to any system capacity and rated voltage level. Figure 5-6 shows the procedure of scaling the system parameters. The main idea of the scaling is to transfer the original system to per-unit values first, which is then followed by backing to the new international system of units (SI unit) system by employing equation (5-9). Therefore, by adopting this methodology, the established VSC-HVDC link model which is in a particular rating system is able to remain unchanged.

\[ x^{(new)} = \frac{x^{(original)}}{x^{(base)}} \cdot x^{(new)} \]  

(5-9)

Figure 5-6 System parameter scaling scheme

In the following paragraphs, how to apply the scaling technique to all kinds of participated controllers are discussed in detail.

5.2.2.1 Inner Current Controller Coefficient

The scaling of the inner current controller coefficients brought one question that whether they are still correct in comparison with the directly calculated coefficient from equation (2-48).
A. Method 1-Scaling

Reference to equation (2-48), Figure 5-7 demonstrates how to scale a system to a new SI system, where $N_1^{(p)}$ is the co-efficient of the inner current controller in per-unit system. It should be noted that all the scaling systems should have exactly the same coefficient $N_1^{(p)}$. Therefore, using the calculated values of $N_1^{(p)}$ based on two different rating systems i) original system and ii) new system (see equations (5-10) and (5-11)), the co-efficient of the new rating system can be easily obtained using equation (5-12).

Figure 5-7 Scaling of inner current controllers

\[
I^{(SI)} \quad I^{(P)} \quad N_1^{(P)} \quad V^{(P)} \quad V^{(SI)}
\]

\[
N_1^{(P)} = N_1^{(sys)} \frac{I_{base1}}{V_{base1}} = N_1^{(sys)} / Z_{base1} \quad (5-10)
\]

\[
N_1^{(P)} = N_1^{(sys2)} \frac{I_{base2}}{V_{base2}} = N_1^{(sys2)} / Z_{base2} \quad (5-11)
\]

\[
\Rightarrow N_1^{(sys2)} = N_1^{(sys1)} \frac{Z_{base2}}{Z_{base1}} \quad (5-12)
\]

B. Method 2-Directly Calculating from Equation (2-48)

This method can be demonstrated using the following steps, where the superscript (1) represents the original system, and the superscript (2) represents the new system, and the superscript (P) indicates per units system.

Firstly, calculate the key coefficient $N_1$ and the time constant $T$ of $N_2$ for both of the original system and new updated system,

\[
\left\{ \begin{array}{ll}
N_1^{(1)} & = \frac{R^{(1)}}{1 - N_2^{(1)}}, \quad \text{Set} \quad T^{(1)} = \frac{R^{(1)}}{L^{(1)}}; \\
N_1^{(2)} & = \frac{R^{(2)}}{1 - N_2^{(2)}}, \quad \text{Set} \quad T^{(2)} = \frac{R^{(2)}}{L^{(2)}};
\end{array} \right. \quad (5-13)
\]

Then, calculate the per unit value of coefficients $R^{(p)}$, $L^{(p)}$ and $T^{(p)}$ of the systems.
Then calculate the updated coefficients $R^{(2)}$ and $L^{(2)}$ of the new system

\[
\begin{align*}
R^{(2)} &= R^{(p)} \cdot \frac{R_{b2}}{R_{b1}} = \frac{R^{(1)} R_{b2}}{R_{b1}}; \\
L^{(2)} &= L^{(p)} \cdot \frac{L_{b2}}{L_{b1}} = \frac{L^{(1)} L_{b2}}{L_{b1}};
\end{align*}
\] (5-15)

Finally, it can be obtained that the coefficient $N_2$ for both systems are the same by calculating the time constant $T$ of $N_2$ and further to calculate $N_2$, 

\[
T^{(2)} = \left( \frac{R^{(2)}}{L^{(2)}} \right) = \frac{R^{(1)} R_{b2}}{L^{(1)} L_{b2}} = \frac{R^{(1)}}{L^{(1)}} = T^{(1)}
\] (5-16)

Therefore, it can be derived that $N_2^{(2)} = N_2^{(1)}$. Then using the calculated value of $N_2$, we can obtain.

\[
N_1^{(2)} = -\frac{R^{(2)}}{1 - N_2^{(2)}} = -\frac{R^{(1)} R_{b2}}{1 - N_2^{(2)}};
\] (5-17)

\[
N_1^{(2)} = N_1^{(1)} \frac{R_{b2}}{R_{b1}} = N_1^{(sys1)} \frac{Z_{base2}}{Z_{base1}}
\] (5-18)

From the above analysis, it can be concluded that the DB controller coefficient directly calculated using the equation (2-48) should be the same as the scaled value using the original system.

### 5.2.2.2 PLL Controller Coefficient

The PLL controller coefficient can be modified by multiplying by $V_b$, as given in the below equation (5-19).

\[
\frac{Y}{U}_{sl} = \theta / V_{sl} \\
\frac{Y}{U}_{pu} = \frac{\theta / \theta_b}{V_{sl} / V_b} = \theta \cdot V_b / V_{sl}
\] (5-19)

where, the base value of the angle $\theta_b$ is equal to 1.
5.2.2.3 Coefficients of the Power and the AC voltage Controller

For the type of PI with an additional filter controller as shown in Figure 5-8, there is no need for any change in the coefficient $T_f$ since it is simply a time constant. However, the unit of $K_p$ in the power controller is kA/MW, and kA/MW/s in $K_i$. Therefore, the new system PI coefficients can be given by equations (5-20) and (5-21) using equation (5-12). Similarly, by replacing the $P_{\text{base}}$ with $V_{\text{base}}$, the PI coefficients for the AC voltage controller loop can be easily obtained.

\[
K_p^{(2)} = K_p^{(1)} \left( \frac{P_{\text{base}1}}{P_{\text{base}2}} \right) \left( \frac{I_{\text{base}2}}{I_{\text{base}1}} \right)
\]

\[
K_i^{(2)} = K_i^{(1)} \left( \frac{P_{\text{base}1}}{P_{\text{base}2}} \right) \left( \frac{I_{\text{base}2}}{I_{\text{base}1}} \right)
\]

\[
\Delta P_e^{(MW)} / \Delta U_f^{(IV)} \rightarrow 1 \rightarrow \frac{1}{1 + T_f s} \rightarrow \Delta I_{\text{dref}}^{(KA)} / \Delta I_{\text{qref}}^{(KA)}
\]

\[
\Delta U_{dc}^{(IV)} \rightarrow K_p \rightarrow \Delta I_{\text{qref}}^{(KA)}
\]

\[
\Delta U_{dc}^{(IV)} \rightarrow \frac{K_i}{s} \rightarrow \frac{K_d \cdot s}{1 + T_f s}
\]

Figure 5-8 Scaling of PI controller with additional filter

Figure 5-9 Scaling of the PID controller

In order to obtain the new PID coefficients for the DC voltage loop, it is necessary to derive the units for each individual part as shown in Table 5-1.
5.2. Preparation Tasks for Interconnection

<table>
<thead>
<tr>
<th>Table 5-1 The units derivation for the PID coefficients</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Proportional part: ( \Delta U_{dc} \cdot K_p = \Delta I_{qref} \Rightarrow K_p = \frac{\Delta I_{qref}}{\Delta U_{dc}} = \frac{kA}{kV} )</td>
</tr>
<tr>
<td>- Integral part: ( \Delta U_{dc} \cdot K_i \cdot s = \Delta I_{qref} \Rightarrow \Delta U_{dc} \cdot K_i \cdot dt = d \Delta I_{qref} \Rightarrow K_i = \frac{kA}{(kV \cdot s)} )</td>
</tr>
<tr>
<td>- Derivative part: ( \Delta U_{dc} \cdot K_d / (1 + T_f \cdot s) = \Delta I_{qref} \Rightarrow \Delta U_{dc} \cdot K_d = \Delta I_{qref} + T_f \cdot \frac{d \Delta I_{qref}}{dt} \Rightarrow dt \cdot \Delta U_{dc} \cdot K_d = dt \cdot \Delta I_{qref} + T_f \cdot d \Delta I_{qref} \Rightarrow K_d = \frac{\Delta I_{qref}}{\Delta U_{dc}} \cdot (t + T_f) / t \Rightarrow K_d = \frac{kA}{kV} )</td>
</tr>
</tbody>
</table>

Therefore, according to Table 5-1, the new PID coefficients for the DC voltage loop can be given by

\[
K_p^{(2)} = K_p^{(1)} \left( \frac{V_{dc\_base1}}{V_{dc\_base2}} \right) \cdot \left( \frac{I_{base2}}{I_{base1}} \right) \quad (5-22)
\]

\[
K_i^{(2)} = K_i^{(1)} \left( \frac{V_{dc\_base1}}{V_{dc\_base2}} \right) \cdot \left( \frac{I_{base2}}{I_{base1}} \right) \quad (5-23)
\]

\[
K_d^{(2)} = K_d^{(1)} \left( \frac{V_{dc\_base1}}{V_{dc\_base2}} \right) \cdot \left( \frac{I_{base2}}{I_{base1}} \right) \quad (5-24)
\]

5.2.2.5 Description of the Methodology to Verify the Accuracy of the Model

Figure 5-10 shows the procedure to verify the accuracy of the system scaling technique, and Figure 5-11 shows the corresponding results. Note that the results confirm that all of four systems have the same eigenvalues, which can also be used to explain the results given earlier in section 5.2.1 that Figure 5-3 and Figure 5-5.

![Flow chart of the verification methodology of modeling](image-url)

Figure 5-10 Flow chart of the verification methodology of modeling
Figure 5-11 Eigenvalue map of the original and scaled systems

It should be noted that the established VSC-HVDC system is still in SI unit, but the interconnected grid model is in per-unit. Therefore, there is a need for a unit transformation block at the integrating interface. This means that the input bus voltages to the VSC links have to be multiplied by the rated voltage base value $V_{\text{base}}$. For the same reason, the output grid currents from the VSC link have to be divided by the rated current base value $I_{\text{base}}$ to transform the original SI unit system to the new per-unit system. In addition, a special attention has to be paid to identify the standard direction of the systems to be interconnected, which have to be consistent.

5.2.3 DC Link Parameter Sensitivity

As demonstrated in the previous section, the established model can be scaled to any rating system as required. However, it is important to note that the DC link parameters are not be able to be scaled since it is physically present, which create a question about the robustness and sensitivity of the designed controllers in chapter 4.

The DC link parameters utilized in this chapter are obtained from the project titled ‘The Gezhouba–Nan Qiao HVDC Project’ which is a ±500kV 1046km long Line Commutate Converter (LCC)-HVDC transmission system with a capacity of 1200MW [150]. The system data is available in [151], where $R_{\text{Link}} = 26\,\Omega$, $L_{\text{Link}} = 0.46\,\text{H}$, $C_{\text{link}} = 13.73\,\mu\text{F}$ for a single line. Although the voltage rating ±500kV is for conventional LCC-HVDC scheme, but the voltage rating for VSC-HVDC system is gradually progressing presently. As reported in [16], the highest pole voltage in a recorded operation was
350 kV (Caprivi Link, Namibia) and the highest transmission voltage was 500kV (Skagerrak 4, Denmark Norway). Therefore, the selection of the DC link parameters in this research is considered realistic.

Figure 5-12 shows the eigenvalue map of the system with a new series of updated DC link parameters. It can be seen from Figure 5-12 that there is significant changes in a pair of modes: 41.83 rad/s moves to 84.91rad/s and 184 rad/s moves towards 569.2 rad/s. Therefore, it is important to determine whether this change will affect the efficiency of the designed controllers.

To investigate this issue, a review on performance evaluation in terms of all the power and voltage controllers with a new series of DC link parameters are also undertaken, and the simulation results are given in Appendix F, which are then being compared with the results in Chapter 4. It was concluded that no significant effects are observed on the controllers within the frequency range considered. As it was also observed in the power and the DC voltage control loops, the pattern of the frequency responses is much more consistent due to the changes in the eigenvalues. It can be noted that this change decreases the difficulties of controller design for these VSC-HVDC links embedded in a weak AC system. Hence it can be concluded that the robustness and sensitivity to the DC link parameters of the designed controllers are acceptable.

![Figure 5-12](image_url)

Figure 5-12 The comparison of the system eigenvalues between the new updated DC link system and the original system

### 5.3 Integrating with the Simplified Australian Grid

In this sub-section, the small signal stability performance of the extended simplified
CHAPTER 5: STABILITY OF VSC-HVDC LINKS EMBEDDED WITH THE WEAK AUSTRALIAN GRID

Australian grid which is operating in parallel with the DB controlled VSC-HVDC links is examined. The integration of VSC-HVDC links with the simplified Australian grid is done by employing the block interconnection technique developed in section 3.4.2 according to the block diagram presented in Figure 5-4 of which the inputs is provided by the IEEE 14 generator 59 bus test system as mentioned before in section 5.1.

5.3.1 Accuracy Evaluation of Designing VSC Controllers Based on Simplified Grid Admittance Model

Prior to the investigation of the small signal stability of the system, the effectiveness of designing the VSC controllers based on the simplified grid admittance model is evaluated by comparing the performance of the Australian model and the simplified grid admittance model. Figure 5-13a,b illustrate the frequency responses of the transfer functions of $V_r(s)/I_r(s)$, $V_i(s)/I_r(s)$, $V_r(s)/I_i(s)$ and $V_i(s)/I_i(s)$ for both of the rectifier side at Innamincka and the inverter side at Armadale. Note that if the source is represented by a constant voltage behind source impedance ($Z_s=R_s+jX_s$), then the above transfer functions will have the following forms: $V_r(s)/I_r(s) = R_s$, $V_i(s)/I_r(s) = X_s$, $V_r(s)/I_i(s) = -X_s$ and $V_i(s)/I_i(s) = R_s$. This confirms the results given in Figure 5-13a ($R_s$) to be the high frequency responses of the system analyzed. Further analysis of Figure 5-13a also demonstrates the resistance and inductance values at the inverter side,

$$R_s = 10^{(-42.5/20)} = 0.0075 \text{ pu}_{M_{bus}=100\text{MW}}$$

$$X_s = 10^{(-28/20)} = 0.0398 \text{ pu}_{M_{bus}=100\text{MW}}$$

Similarly, at the rectifier side, these values are

$$R_s = 10^{(-63/20)} = 0.0007 \text{ pu}_{M_{bus}=100\text{MW}}$$

$$X_s = 10^{(-32.5/20)} = 0.0237 \text{ pu}_{M_{bus}=100\text{MW}}$$

However, at very low and at intermediate frequencies, the source cannot be represented by a voltage behind impedance. For example, at very low frequencies at the inverter side, the results of the transfer functions are,

$$V_r(s)/I_r(s) = 10^{(-12.5/20)} = 0.2371 \text{ pu}_{M_{bus}=100\text{MW}}$$

$$V_i(s)/I_r(s) = 10^{(-13/20)} = 0.2239 \text{ pu}_{M_{bus}=100\text{MW}}$$
5.3. INTEGRATING WITH THE SIMPLIFIED AUSTRALIAN GRID

\[
V_r(s)/I_r(s) = -10^{(2.5/20)} - 1.3335 \text{pu}_{M_{\text{nom}}=100\text{MW}} \quad (5-31)
\]

\[
V_i(s)/I_i(s) = 10^{(0/20)} = 1 \text{pu}_{M_{\text{nom}}=100\text{MW}} \quad (5-32)
\]

As shown above, \(V_r(s)/I_r(s)\) is not equal to \(V_i(s)/I_i(s)\), and \(V_i(s)/I_i(s)\) is not equal to \(-V_r(s)/I_r(s)\). This indicates that the VSC controllers adopted in chapter 4 are in fact to represent the source by a voltage behind equivalent impedance at high frequencies. Therefore, it is necessary to examine whether this representation is adequate in the controller design.

![Figure 5-13](image)

(a) The frequency responses for the rectifier side (a) and for inverter side (b) for the higher order grid impedance models (I to V).
The following eight figures from Figure 5-14 to Figure 5-21 present the frequency responses of the open loop transfer functions of all four controllers using the equivalent high frequency grid admittance model, and their corresponding step responses. The following two primary conclusions can be drawn from these results:

1) In the active power and DC voltage loops (Figure 5-14 and Figure 5-18), no change was observed in the major loop using different grid models. In the cross-coupling AC voltage loops, however discrepancies are observed on the transient magnitude change and the oscillation frequencies, but can be ignored in this application.

2) In the AC voltage loop results at both ends (Figure 5-16 and Figure 5-20), the step response time of the voltage of the higher order grid admittance model appears not as fast as the equivalent simplified grid admittance model. This might be caused by the interaction between the VSC-HVDC voltage controllers and the nearby SVCs. Although there are adverse impacts on the cross-coupling control loops as in the above conclusion, however, this is assumed to be acceptable since the level of the observed distinctions is small and can be ignored reasonably.

In summary, using the frequency responses of the open loop transfer function of the target system with all the controllers in service, it can be concluded that the frequency responses differ slightly at very low frequency range. This confirms to represent the grid as a source behind impedance is appropriate.

Figure 5-14 The open loop frequency responses, $P_{\text{rec}}/P_{\text{ref}}$
5.3. **INTEGRATING WITH THE SIMPLIFIED AUSTRALIAN GRID**

Figure 5-15 The step responses test of the power reference at the rectifier side

Figure 5-16 The open loop frequency responses, \( U_{\text{ref,rec}} / U_{\text{f,rec}} \)
CHAPTER 5: STABILITY OF VSC-HVDC LINKS EMBEDDED WITH THE WEAK AUSTRALIAN GRID

Figure 5-17 The step response test of the AC voltage reference at the rectifier side

Figure 5-18 The open loop frequency responses, $U_{\text{dc ref rec}}/U_{\text{dc rec}}$
5.3. Integrating with the simplified Australian grid

Figure 5-19 The step response test of the DC voltage reference at the inverter side

Figure 5-20 The open loop frequency responses, $U_{f,\text{ref_inv}}/U_{f,\text{inv}}$
5.3.2 Stability Analysis

Table 5-2 summarizes the inter-area modes of the interconnected model, in which fourteen generators are equipped with the power system stabilizers (PSSs) with an equivalent damping gain of 10 per unit, while only the three Innamincka machines are assumed to operate without PSSs.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Case: Three Generators (Innamincka) with PSSs out of service</th>
<th>Mode Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I 40</td>
<td>-0.286 3.907 0.073</td>
<td>Innamincka &amp; VIC &amp; Canberra VS SA</td>
</tr>
<tr>
<td>I 35</td>
<td>-0.290 3.417 0.085</td>
<td>Innamincka VS VIC &amp; SA</td>
</tr>
<tr>
<td>I 25</td>
<td>-0.242 2.273 0.106</td>
<td>Innamincka &amp; SA &amp; QLD VS VIC &amp; NSW &amp; Canberra</td>
</tr>
<tr>
<td>I 15</td>
<td>-0.154 1.703 0.090</td>
<td>QLD VS Innamincka &amp; SA &amp; VIC</td>
</tr>
</tbody>
</table>

The eigenvalue map of the main electro mechanical modes of the interconnected system is given in Figure 5-22, which is obtained by using Matlab m-file. The main inter-
area modes of I40, I35, I25, and I15 are found to be lightly damped in the figure. The damping criterion used here is chosen according to the Australian National Electricity Rules which require the halving time of the least damped electro-mechanical mode of oscillation is not more than five seconds \((1/T \leq \ln(2)/5)\) [144], which corresponds to a damping constant with a magnitude greater than \(-0.14\) Nepers/Second \((\text{Np}/\text{s})\).

![Figure 5-22 Eigenvalue map of the interconnected system](image.png)

A. Mode I40 Eigen Vector and Participation Factor Analysis

In the following of this paragraph, mode I40 associated figure (right eigenvector) is presented to indicate the energy exchange of the power system considered (see Figure 5-23). In the figure, the circle represents the phasor diagram of associated generators (such as ING1, ING2, ING3, YPS_3, LPS_3, HPS_1, NPS_5, TPS_5 and PPS_5). For the representations of the symbols, refer to Figure 5-1. There are nine participating generators which clearly form two groups whose phasor differ by 180°. The consequence is if oscillations were observed in one group, similar oscillations would be observed in the anti-phase group as well. For this particular mode (I40), it is implied that the Innamincka machines, the Victoria machines and the Canberra machine together oscillate against the South Australia machines.
It can be easily seen from the participation factor plot (see Figure 5-24) that the main participants are the rotor speed angles and the rotor speed frequencies of generators. The most significant participants are the generators located at SA and Victoria with a value of ranging from 15.5% to 8.68%, which are followed by the generators of Innamincka group where the participation factors are equal to 0.0553.

The expected left-shift by fitting a PSS to a particular generator in a multi-machine power system at a selected mode can be predicted by the following formula [99].

$$\Delta \delta \approx -D_{pss} \left| \frac{p}{2H} \right|$$  \hspace{1cm} (5-33)

where, $D_{pss}$ represents damping gain of the PSS on the machine rating, $|p|$ is the magnitude of the participation of the machine rotor speed in the selected electromechanical mode and $H$ is the inertia constant of the machine on the machine rating.
Therefore, by assuming $D_{\text{PSS}}$ to be equal to 1, the approximated left-shift damping ratio by introducing additional PSS at Innamincka machines can be calculated as

$$\Delta \delta \approx -3 \times \left( \frac{0.0553}{2 \times 3.2} \right) = -0.0259$$  \hspace{1cm} (5-34)

Figure 5-24 Participation factor for mode I40

B. Mode I35 Eigen-Vector and Participation Factor Analysis

The right eigenvector prototype of Mode I35 (see Figure 5-25) shows that the machines at Innamincka oscillate against with the machines in the region of Victoria and South Australia.

As suggested in the participation factor analysis plot of the mode I35 (see Figure 5-26), the main participants are the two machines locating at Victoria, LPS and YPS, which account for a factor of 23.6% and 7.17% respectively. The participation factors of the Innamincka machines are 5.6% each, followed by the machines BPS at New South Wales and PPS at the region of South Australia.

The approximate left-shift damping ratio by introducing additional PSS at Innamincka machines is

$$\Delta \delta \approx -3 \times \left( \frac{0.056}{2 \times 3.2} \right) = -0.026$$  \hspace{1cm} (5-35)
CHAPTER 5: STABILITY OF VSC-HVDC LINKS EMBEDDED WITH THE WEAK AUSTRALIAN GRID

Extended Right Eigenvector Prototype

15 Jul 2013 - 18:28
LF_CASE01_R3_S 14-GENERATOR, SIMPLIFIED SYSTEM MODEL.
AREA4->AREA2->AREA3->AREA5 500-1000-500 MW.

Speed eigenvector components for I35 mode

Figure 5-25 Right eigenvector prototype of mode I35

Participation factor for Mode:-0.28986 +/- 3.4173 j

Figure 5-26 Participation factor for mode I35
C. Mode I25 Eigenvector and Participation Factor Analysis

It can be seen from Figure 5-27 that the machines at Innamincka, South Australia and Queensland oscillate against the machines sitting in Victoria, New South Wales and Canberra.

*Figure 5-27 Right eigenvector prototype of mode I25*

By conducting participation factor analysis (see Figure 5-28), it is suggested that the important affecting factor can be classified into three categories. Firstly, the participant GPS and SPS machines at Queensland gain the most priority which account for 13.4% and 7.59% respectively. Secondly, the machines CPS and TPS located at Queensland and the machines MPS, BPS and EPS located in New South Wales take over weights ranging from 4.47% to 2.4%. Finally, the machines at Innamincka count 2.05% each.

The approximate left-shift damping ratio by introducing additional PSS to the Innamincka machines is

\[
\Delta \delta \approx -3 \times \left( \frac{0.0205}{2 \times 3.2} \right) = -0.0096
\]  

(5-36)
D. Mode I15 Eigenvector and Participation Factor Analysis

It is important to note that the Mode I15 is the least damped inter-area mode in this study. Figure 5-29 indicates that the machines in Queensland oscillate against with that in Innamincka, SA and Victoria. In addition, the participation factor analysis results as shown in Figure 5-30 also suggest that the important affecting factor can be separated into three categories. First priority gives to the machines at SA approximately 7.58%-10.7%, followed by the Innamincka machines about 6.71% each. The final group involves the NPS machine in SA, and the GPS machine and the SPS machine in Queensland and the LPS machine in Victoria ranging from 5.05% to 2.29%.

The potential left-shift damping ratio by introducing PSSs to the Innamincka machines can be calculated as

\[
\Delta \delta \approx -3 \times \frac{0.0671}{2 \times 3.2} = -0.031453
\]  (5-37)
5.3. Integrating with the Simplified Australian Grid

Extended Right Eigenvector Prototype

15 Jul 2013 - 18:15
LF_CASE01_R3_S  14-GENERATOR, SIMPLIFIED SYSTEM MODEL.
AREA4->AREA2->AREA3->AREA5 500-1000-500 MW.

Speed eigenvector components for I15 mode

Participation factor for Mode:-0.15417 +/- 1.7033 j

Figure 5-29 Right eigenvector prototype of mode I15

Figure 5-30 Participation factor for mode I15
5.3.3 Damping Controllers Design

The equivalent damping gain of the PSSs of the three Innamincka machines are set to be increased from zero (no PSSs in service) to 30 pu in 5 pu steps (see Figure 5-31). It is obvious that the supplementary PSSs equivalence fitted to the Innamincka machines can enhance the system damping performance, since all of the inter-area modes are left-shifted.

![Figure 5-31](image-url)

Figure 5-31 Eigenvalue evolution for the PSS damping gain on each generator is increased from zero (no PSS in service) to 30 pu on machine base (750MVA) in 5 pu steps.

Table 5-3 Approximate improvements on system damping: comparison of the results obtained from adding with equivalent damping torque (Figure 5-31) and the analysis for participation factor.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Figure 5-31</th>
<th>Participation factor Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>(Approximation based on 30pu)</td>
</tr>
<tr>
<td>I40</td>
<td>-0.3699-(-0.2862)= -0.0837</td>
<td>-0.0259·30·100/750= -0.1036</td>
</tr>
<tr>
<td>I35</td>
<td>-0.3771-(-0.2899)= -0.0872</td>
<td>-0.026·30·100/750= -0.104</td>
</tr>
<tr>
<td>I25</td>
<td>-0.2683-(-0.2425)= -0.0158</td>
<td>-0.0096·30·100/750= -0.0384</td>
</tr>
<tr>
<td>I15</td>
<td>-0.2638-(-0.1542)= -0.1096</td>
<td>-0.031453·30·100/750= -0.12581</td>
</tr>
</tbody>
</table>

Table 5-3 gives the comparison results of the improvements on the system damping. In the table, the third column data is calculated by the participation factor, and the data in the second column is computed by using the system model by adding an equivalent damping.
gain to the torque. In this study, the base capacity of the system ($S_{\text{base}}$) is 100MVA, while the machine base ($M_{\text{base}}$) is set to 750MVA. It is shown that both of these cases have similar results despite an error of 0.02 occurred in each mode. This also implies that the approximation based on the participation factor is an effective way to evaluate the damping performance of PSS.

5.3.3.1 PSS Design and Assessment

The approach for PSS design employed in this study is explained in detail in [99, 152]. As stated in [99],

“The objective of PSS design is to induce on the shaft of the generator a torque of electromagnetic origin which is in-phase with rotor-speed perturbations of the generator”

Here, the procedure to design the PSS is given below:

Step 1: Determine the torque coefficients induced by PSS. In other words, specify the DAMP(s) coefficient, add was out filter and low pass filter to the coefficient making the transfer function proper to obtain the transfer function of the stabilizer DAMP(s),

Step 2: Obtain the gain and phase characteristic of the excitation system, the generator and the power system (i.e. the PVr characteristic),

Step 3: Apply curve fitting to the selected PVr characteristic,

Step 4: Derive the PSS transfer function,

Step 5: Assess the performance of PSS by using eigenvalue analysis and by comparing the torque coefficients induced by the PSS specified with the specified value.

A. Specifying the DAMP(s)

It was also stated in [99] that “The wash-out and low-pass filter time constant are chosen so that, over the frequency range of interest, DAMP(s) has near constant gain ($D_{\text{PSS}}$) and phase between 0 and -30 degrees (depend on the damping requirements of local- and inter-area modes).”

Typically, DAMP(s) has the following form.

$$DAMP(s) = D_e \cdot B(s)$$  \hspace{1cm} (5-38)

where

$$B(s) = \left(\frac{s T_w}{1 + s T_w}\right) \left(\frac{1}{1 + s T_p}\right)^\nu$$  \hspace{1cm} (5-39)
The frequency response of the DAMP(s) specified in this case example is shown in Figure 5-32, where $D_e$ equals to 20pu on the basis of machine rating and the time constants for the wash out filter and low-pass filter are set to be 3s and 0.05s respectively.

Figure 5-32 Bode plot for DAMP(s) with $D_{PSS}=20$pu on $M_{base}$ 750 MVA, $T_w=3s$ and $T_p=0.05s$.

**B. PVr characteristic and curve fitting for Innamincka Generator 1**

To disable the shaft dynamics of all the machines, the transfer function from the voltage reference input ($V_r$) of Automatic Voltage Regulator (AVR) on Innamincka generator #1 to the torque of the electrical power output ($P$) that $P_{Vr}(s)$ can be easily calculated as shown in Figure 5-33 (solid blue line). For design purpose, the $P_{Vr}(s)$ should be fitted to a lower order plant as given in equation (5-40) below. Its corresponding Bode plot is given in Figure 5-33 (dotted red line).

$$P_{Vr}(s) = \frac{18.6s + 3268}{s^2 + 15.25s + 59.63} = 54.805 \cdot \frac{0.0056916s + 1}{0.01677s^2 + 0.25574s + 1} \quad (5-40)$$

Then converting $P_{Vr}(s)$ from pu on $S_{base}$ (100 MVA) to pu on $M_{base}$ (750 MVA) and specify the DAMP(s) function,

$$P_{Vr - M}(s) = K_{sm} \cdot G(s) = K_{sm} \cdot \frac{1 + 0.0056916s}{0.01677s^2 + 0.25574s + 1} \quad (5-41)$$

Here, $K_{sm} = K_s \cdot S_{base} / M_{base} = 54.805 \cdot 100 / 750 = 7.3073$
5.3. Integrating with the Simplified Australian Grid

Figure 5-33 PVr characteristic and curve fitting for Innamincka generator #1

C. Derivation of the PSS Transfer Function

The transfer function of PSS that $PSS(s)$ and the system PVr characteristics $PVr(s)$ are related in terms of the following equation,

$$PSS(s) \cdot PVr(s) = DAMP(s)$$  \hspace{1cm} (5-42)

Then the PSS transfer function can be easily derived as,

$$PSS(s) = \frac{DAMP(s)}{PVr - M(s)}$$

$$= \frac{D_{PSS}}{K_{in}} \cdot \frac{\frac{3s}{1 + 3s} \cdot \frac{1}{1 + 0.05s}}{0.01677s^2 + 0.25574s + 1}$$  \hspace{1cm} (5-43)

$$= \frac{(0.13685 \cdot D_{PSS})}{1 + 3s} \cdot \frac{1}{1 + 0.05s} \cdot \frac{0.01677s^2 + 0.25574s + 1}{0.0056916s + 1}$$

D. Assessing the PSS Performance

a) Eigenvalue Analysis

Figure 5-34a shows that the damping performance of the system under high loading condition has been enhanced by the designed PSS. However, it can be noted that the compensation added by PSS is not so significant, and it can be further verified by conducting a small step test (0.01 pu) on the voltage reference of Innamincka generator #1 (see Figure 5-35). Figure 5-35 shows that the response of the generator output power is damped slightly by comparing the case with (dashed black curve) and without PSS (solid red line). In addition, the damping performance of the system under the light loading...
condition has not been changed significantly, which can be verified by the eigenvalue map shown in Figure 5-34b. As it can be seen in the figure, the eigenvalues of this operating mode have not been significantly left-shifted. However, it is worth noting that it does not deteriorate the damping performance of the system at least (see Figure 5-35). To further improve the damping performance of the system, the additional damping torque added by introducing supplementary POD controllers will be shown in the next section.

(a) High loading condition

(b) Light loading condition

Figure 5-34 The comparison of the rotor modes of the system with the equivalent damping torque (blue star) and the system fitted with PSS (red dot) under the high loading condition and light loading condition. The damping gain in Innamincka generators are increased from zero (no PSS in service) to 30 pu in 5 pu steps.

Figure 5-35 Comparison on the power output of generator #1 from Innamincka under the condition with and without PSS in service by applying a small disturbance 0.01pu on the reference voltage of Innamincka generator #1
5.3. INTEGRATING WITH THE SIMPLIFIED AUSTRALIAN GRID

b) Comparing the Torque Coefficients

As indicated in [99] ‘To obtain the torque coefficient induced by PSS on the shaft of the machine, the shaft dynamics is disabled and a speed test signal was injected into the PSS’. Figure 5-36a,b show the induced damping torque and synchronous by PSS torque in Innamincka generator #1 (red curve) compared with the specified damping torque coefficient (blue curve). Results in these plots confirm the successful implementation of the PSS.

![Figure 5-36a](image1)  
(a) Damping torque coefficients introduced by the PSS in the Innamincka generator #1 (red curve) compared with the specified damping torque coefficient (blue curve)  
(b) induced synchronizing torque (De equals to be 20 pu on M_base)

5.3.3.2 POD Design and Assessment

The auxiliary device fitted to the FACTS devices for enhancing power system stability are called the power oscillation damping controllers, which is designed to enhance the damping performance of certain inter-area modes. Based on the source of the feedback signals, two types of POD, local POD and wide area POD (WAPOD) are designed systematically based on the ‘residue’ method. Note that the residue analysis gives an indication on the selection of the best suitable feedback signal which is the one with the largest residue, since such signal is defined to be capable of improving the targeting oscillation mode with less efforts [153].

Figure 5-37 shows the general structure of the AC/DC hybrid network with POD damping controllers. The POD controllers are composed of an amplification block, a wash-
out and a low-pass filter and \( m_c \) stages lead-lag blocks. The transfer function \( G(s) \) of the POD controllers can be given by,

\[
G(s) = k \cdot \frac{1}{1+T_{LP}s} \cdot \frac{sT_{w}}{1+T_{lead}s} \cdot \frac{sT_{lag}}{1+T_{lag}s}
\]

(5-44)

where, \( T_{LP} \) denotes the time constant of the low-pass filter; similarly, \( T_{w} \) stands for the time constant of wash-out filter; \( T_{lead} \) and \( T_{lag} \) imply time constants for the lead-lag block; \( m_c \) is the number if compensation stages (usually \( m_c = 2 \)).

Figure 5-37 The schematic diagram of the VSC-HVDC damping system

The theoretical analysis and the systematic design approach are well documented in [98, 100, 153]. Assuming that the excitation mode of the system is the ‘Target mode’ \( \lambda_h \) only, the simplified approximate model of the target system can be given by \( \frac{R_h}{s-\lambda_h} \), where \( R_h \) is the open-loop residue from the selected input to the output of the MIMO system for the particular \( h^{th} \) complex mode. Furthermore, assuming that the POD controller \( G(s) \) is in place, the closed-loop transfer function for the POD loop and the balanced equation for \( \lambda_h \) via the eigenvalue calculation can be obtained. Furthermore, by applying the small signal technique and first order Taylor series expansion, it can be obtained the left-shift of a ‘target mode’ caused by the POD controllers satisfies the below equation,
5.3. Integrating with the Simplified Australian Grid

\[ \Delta \lambda_n \approx k \cdot R_n \cdot G(\lambda_n) \]  

(5-45)

where \( k \) is chosen such that

\[ k \ll 1 \cdot \frac{1}{R_n \cdot \left( \frac{\partial G(s)}{\partial s} \right)_{s=\lambda_n}} \]  

(5-46)

In order to left-shift the target mode horizontally by using a POD controller as in equation (5-44), the parameter selections of \( T_{lead} \) and \( T_{lag} \) must satisfy the following relationship [100],

\[ \phi_{comp} = \arg(G(\lambda_n)) = 180^\circ - \arg(R_n) \]  

(5-47)

where for \( G(s) \),

\[ \alpha_c = \frac{T_{lead}}{T_{lag}} = \frac{1 - \sin(\phi_{comp})}{1 + \sin(\phi_{comp})} \]  

(5-48)

\[ T_{lead} = \frac{1}{\omega \sqrt{\alpha_c}}; T_{lag} = \alpha_c \cdot T_{lag} \]  

(5-49)

A. Residue Analysis

Table 5-4 presented in the following shows the residue analysis for the interconnected system. For the local POD, the power flow in adjacent AC lines \( \Delta P_{L34} \) is selected as the input signal since it has relatively higher residue [98]. For the same reason, the bus voltage angle difference between Brisbane and Innamincka \( \Delta \delta_{BI} \) is chosen as the input signal for the WAPOD.

Note that in Table 5-4, 17 different modes are considered. In this table, two types of stabilizing input signals are considered: (i) local signals such as power flow in adjacent AC lines \( \Delta P_{L12, L34} \) and (ii) wide-area signals such as bus voltage angles at key nodes \( (V_{AB, VAS, VAM, VAA, VAI}) \) in the various regions of the system. For explanations of the symbols, refer to Figure 5-1. In this table, \( \delta \) and \( \omega \) denote the bus voltage angle and frequency respectively, while the subscript B, S, M, A, I denote the 5 areas Brisbane, Sydney, Melbourne, Adelaide and Innamincka respectively.
Table 5-4 Residue analysis of the system

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<tr>
<th>Mode</th>
<th>Local Signal</th>
<th>Rectifier Side Power Reference Input</th>
<th>Wide area signal</th>
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<th>ΔPw</th>
<th>ΔPHx</th>
<th>ΔPHxw</th>
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B. Local POD controller design

It can be seen from Table 5-4 that the residue angle from \( \text{P}_{\text{REF,REC}} \) to \( \Delta \text{P}_{\text{L34}} \) under the least damped mode 17 (at frequency of 1.7033 rad/s) is 89.684°. Using the equations (5-47) to (5-49), \( T_{\text{lead}} \) and \( T_{\text{lag}} \) can be calculated as 1.4229s and 0.24224s respectively. Then the transfer function of the local POD can be given by

\[
POD(s) = K_{\text{SS}} \cdot Q(s) = K_{\text{SS}} \cdot \left( \frac{10s}{1+10s} \right) \cdot \left( \frac{1}{1+0.01s} \right) \cdot \left( \frac{1+1.4229s}{1+0.24224s} \right)^2
\]

(5-50)

Figure 5-38 shows the effectiveness of the designed POD control. The result meets the compensation requirement, since sum of the compensated angle of the POD (92.3°) and the residue angle of the target mode (89.684°) is approximate 180°, which ensures the horizontally left-shift of the mode.

![Bode Diagram](image)

Figure 5-38 Frequency response of lead compensator \( Q(s) \) for the local POD

a) Root Locus Analysis

The root locus analysis has been conducted and the eigenvalue map of the system for different values of the amplification block \( K_{\text{SS}} \) is shown in Figure 5-39. Note that the target inter-area mode I15 is left-shifted from -0.1549 Np/s to -0.3862 Np/s under high loading condition (see Figure 5-39a), which also resulted in shift of the inter-area modes of I40, I35, I25. Although the Mode I20 is shifted to the right but which is still with enough damping ratio. This is also the cause of the first swing appeared in the ‘with local POD
only’ plot of the Figure 5-41. In addition, for the system under light loading condition (see Figure 5-39b), the modes I50, I30 and I25 remain unchanged, except the mode I40 but still within the acceptable limit. Similar to the high loading condition, mode I20 is also shifted to the right but with an adequate damping performance.

![Eigenvalue Analysis of POD in cooperation with PSS](image)

Figure 5-39 The eigenvalue map of system fitted with POD, where the letters represent the gains of the POD and KSS is increased from 3.642-10^-3 to 7.03642-10^-2 with a step size of 0.01.

**b) Eigenvalue Analysis of POD in cooperation with PSS**

By comparing the eigenvalue maps of the system with the coefficient KSS varying from 3.642-10^-3 to 7.03642-10^-2 at a step size of 0.01, and with PSS on and off, it can be concluded that the inclusion of PSS has significantly improved the inter-area mode I40. However, the other three inter-area modes display small improvements including the high loading conditions (see Figure 5-40a). For the system under the light loading condition, the superposed effects of PSS and POD can be observed in Figure 5-40b. Note that no significant impact has been observed by placing these damping controllers in service. Although the mode I40 has been slightly deteriorated, it is still within the acceptable limit.
5.3. Integrating with the Simplified Australian Grid

Figure 5-40 The eigenvalue map of system fitted with POD and PSS. Here the letters are the gains of the POD and KSS is increased from $3.642 \times 10^{-3}$ to $7.03642 \times 10^{-2}$ with a step size of 0.01.

By applying the small-signal disturbance test (0.01 pu on the reference voltage command) to Innamincka generator #1, it can be easily seen in Figure 5-41 that the damping performance of the system is improved by placing the PSS and POD controller. The plot labelled ‘with POD (Local) only’ provides a better damping performance than ‘the PSS only’ controller. However, all these supplementary control schemes can provide satisfactory improvements on damping the system inter-area modes.

Figure 5-41 Power output of Innamincka generator #1 following a 0.01 pu step change on the voltage reference of Innamincka generators.
Figure 5-42 provides the proof of the adequate performance of the VSC controllers cooperating with the supplementary PSS and local POD controllers. A sudden 0.01pu step change of the power reference command at the rectifier side are applied to the system, the top-left rectifier power plot in the figure displays some oscillations at the first 10s as a consequence of the POD controllers taking effects. It can be concluded in this result that all the controllers perform well as expected.

![Figure 5-42](image)

Figure 5-42 The performance evaluation of the VSC controllers with the supplementary controllers in service following a step change of 0.01 pu on power reference of the rectifier side converter.

C. WAPOD Controller Design

As displayed in the residue analysis, Table 5-4, the residue angle from $P_{REF,REC}$ to $\Delta \delta_{Bi}$ of the lightly damped mode 17 is $70.661^\circ$. Similarly, for the WAPOD, the results of the calculated $T_{lead}$ and $T_{lag}$ are 1.8435s and 0.18697s respectively. The transfer function for the WAPOD can be obtained by

$$POD(s) = KSS \cdot Q(s) = KSS \cdot \left( \frac{10s}{1+10s} \right) \cdot \left( \frac{1}{1+0.01s} \right) \left( \frac{1+1.8435s}{1+0.18697s} \right)^2$$

\( (5-51) \)

Figure 5-43 shows the frequency response of the designed lead compensator $Q(s)$ for WAPOD, which meet the design requirements.
5.3. Integrating with the Simplified Australian Grid

Figure 5-43 Frequency response of lead compensator Q(s) of the WAPOD

a) Root Locus Analysis

By increasing the amplification block coefficients KSS from 3.642×10^{-3} to 0.12 with a step size of 0.02, the eigenvalue evolution map was obtained by conducting the root-locus analysis as given in Figure 5-44 and 5-45. The results in Figure 5-44 indicate a significant improvement of the damping performances of the all 4 inter-area modes under high loading condition. To examine the system sensitivity to the employment of WAPOD (designed to improve the damping performance of high loading condition), the damping performance of light loading condition is also tested.

Figure 5-44 The eigenvalue map of system fitted with WAPOD under high loading condition, where the letters represent the gains of the WAPOD, as KSS is increased from 3.642×10^{-3} to 0.12 with a step size of 0.02.
CHAPTER 5: STABILITY OF VSC-HVDC LINKS EMBEDDED WITH THE WEAK AUSTRALIAN GRID

Figure 5-45 The eigenvalue map of system fitted with WAPOD under light loading condition, where the letters represent the gains of the WAPOD, while KSS is increased from $3.642 \times 10^{-4}$ to 0.12 with a step size of 0.02.

The simulation results suggest that the involvement of the WAPOD does not deteriorate the light loading scenario, but not significantly improve it as well (see Figure 5-45).

**b) Eigenvalue Analysis on WAPOD in cooperation with PSS**

Figure 5-46 shows the eigenvalue analysis of the system operating under high loading condition by employing the WAPOD damping controller and the PSS controller. It can be observed from the figure that the damping performance of the system has been improved significantly with employing the PSS only. This is further confirmed by the time response plot shown in Figure 5-47, which demonstrate that the adequate damping performance can be solely obtained by the WAPOD controller in service. In addition, it is shown that the performance of WAPOD together with PSS is better than that of local POD with PSS controller (red curve and magenta curve in Figure 5-47). Figure 5-48 illustrates the performance of the designed VSC-controllers is still satisfactory as they operate well even with the additional WAPOD controller.
5.3. Integrating with the Simplified Australian Grid

Figure 5-46 Eigenvalue analysis of WAPOD with PSS under high loading condition, where KSS is increased from $3.642 \times 10^{-4}$ to 0.12 with a step size of 0.02.

Figure 5-47 Power outputs of Innamincka generator #1 following a step change of 0.01 pu on voltage reference of Innamincka generators.
Figure 5-48 The performance evaluation of the VSC controllers with PSS and WAPOD in service following a step change of 0.01 pu on power reference of the rectifier side converter.

5.4 Conclusion and Discussion

This chapter presented a small-signal rotor-angle stability analysis of a model of the Australian power system with embedded VSC based HVDC links. We examined the adequacy of using a constant admittance matrix to model the AC transmission system for the analysis of the electromechanical modes. In addition, to facilitate this analysis for various rating systems, a flexible scaling technique was introduced. The parameter sensitivity in terms of the length of the DC link was also examined in the chapter, which does not affect the performance of the designed controller, but on the contrary, enhanced the system stability to some extent. Through the back examination of the basement for the controller design against a higher order detailed Australian grid, it is confirmed that the
assumption that designing the control system of VSC-HVDC based on the first order grid model is sufficiently accurate.

Furthermore, for analytical purposes, a simplified model of the Australian power system is used to connect the high capacity, but as yet undeveloped, geothermal resource in the region of Innamincka in northern South Australia via a 1,100 km HVDC link to Armadale in northern New South Wales. By diagnosing the lightly damped inter-area modes of the hybrid AC/DC grid, it is found that the introduction of the new source of geothermal power generation has an adverse impact on the damping performance of the system. Hence, the supplementary damping controllers (i) generator power system stabilizers (PSS) fitted to the synchronous machines which are used to convert geothermal energy to electrical power and (ii) power oscillation damping controllers fitted to the VSC-HVDC link are well designed to provide adequate damping in rotor modes of oscillation. In the design of POD, two types of stabilizing input signals are considered: (i) local signals such as power flow in adjacent AC lines and (ii) wide-area signals such as bus voltage angles at key nodes in the various regions of the system. It was concluded that the small-signal rotor-angle stability of the interconnected AC/DC system was greatly enhanced by employing the designed damping controllers. Lastly, it should be emphasized that the analysis tool utilized in this chapter is MATLAB m-file.
6.1 Summary

Due to the increasing demand on producing energy from renewable resources, VSC-HVDC has become a common and effective solution for the grid integration of such energy resources, which also promoted the ongoing developments in the field. As it is a widely employed and proven VSC-HVDC technique, it can not only increase the transmission capability but also enhance the damping ability and transient ability of the system by employing an additional damping controller.

Significant levels of renewable energy resources (such as wind, solar and geothermal) are available worldwide and economically harvested locally. However, the locations of such resources are usually far from the main load centres and cities. Therefore, utilization of these energies is very challenging. For example, the power grid in Australia is one of the world’s longest interconnected power systems starting from Port Douglas in Queensland and ending in Port Lincoln in South Australia with a total distance more than 4000 kilometres.
The motivation of this research study has been to design and develop a detailed mathematical understanding of the control system of a VSC-HVDC that can be integrated into such a long and weak AC system.

As presented in the thesis, the outer power loop, the inner current loop, synchronization method, and the input-output impedance of a weak AC interconnected VSC-HVDC system have been partially studied in the literature. However, most of these earlier studies typically employed a single-machine infinite-bus test system and did not study a wide range of operating conditions that is likely to be encountered in practice. Therefore, one of the primary aims of this thesis was to design a robust control system with a simple structure and study a wide range of loading conditions that may occur in practice.

To achieve this main aim, this research can be divided into two main sections. The first section (Chapter 2–4) of the research has investigated three potential linear inner current control schemes to determine the most suitable type. Then an analytical model of the DB controlled VSC was developed as the suitable controller. The discussions in the thesis include a set of linearized representation of system components which prepared the ground work. This resulted in the development of a new method for eliminating the modulator/demodulator blocks. Using this new model, the classical frequency response technique was also applied to a set of linear models using a number of operating points to develop a robust outer loop controller.

In the second section of the research (Chapter 5), the impact of an admittance representation of the grid to the controller design in the VSC-HVDC system and a scaling approach were investigated. The investigations of this section also include the integration of the designed VSC-HVDC links into the Extended Simplified South-East Australian power grid, which aimed to form a large AC/DC integrated power system. In addition, extensive eigen-sensitivity studies were performed to determine the characteristics of the interaction and to identify the critical parameters. Finally, the power damping controllers as PSS, local POD and WAPOD were designed to enhance the power system stability.
6.2 Original Contributions and associated Key Results

6.2.1 Original Contributions

In this thesis, the applicability of three types of linear controllers, namely PI, PR and DB, for VSC-HVDC transformation systems was investigated in depth to identify the most suitable current control method.

In addition, a novel small-signal model for the digital DB controlled voltage-controlled oscillator was also developed and systematically verified. To achieve this, the study developed a new methodology to linearize the modulator/demodulator blocks which are used to develop the small signal models for several key components.

The most significant contribution of the thesis is in designing a controller of the VSC-HVDC system capable of working with a weak AC system. I proposed a robust controller design methodology which takes into account a set of operating points covering the converter operating capability (PQ capacity chart) and various grid parameters including X/R ratios. I realized this method by applying the frequency response technique to a set of open loop transfer functions of the target system, and bring up with practical recommendations.

6.2.2 Associated Key Results of the Thesis

1. Three types of linear inner current controllers, PI, PR, and DB, were discussed for a VSC-HVDC transmission system (Chapter 2).

   - A new method for the selection and optimization of the parameters of the PI compensators in the various control loops using a decoupled control strategy was proposed. In this study, the initial value of the PI compensator parameters for input to the optimization algorithm were obtained using the classical frequency response design approach to simplified linear models of the open-loop transfer functions of VSC-HVDC control system. An optimization algorithm based on the simplex method was adopted. The objective was to simultaneously minimize the weighted sum of the “integral of the time absolute-error products” (ITAE) of the active power, the reactive-power, the DC voltage and the inner current controllers of the respective VSCs. It was concluded that if necessary the weightings of the error signals may need to be modified in this stage.
6.2. **Original Contributions and Associated Key Results**

- Four different DB controllers were also studied in the thesis by including one sample delay with the reduced gain and Smith Predictor, two sample delays based on IMC control design and solving feedback transfer function. It was concluded from the simulation results that the solving feedback transfer function method proves to be more superior to the other methods specifically during the large step response with a fast settling time and with an acceptable reactive current overshoot.

2. A new small signal model for the digital DB controlled VSC was developed (Chapter 3).
  - Padé Approximation was employed to transfer the discrete DB controller to continuous domain.
  - Three approximation methods were investigated and compared: the first order Padé Approximation, the third order Padé Approximation and first order lag approximation since it was essential to model the ZOH, the DB control block and the delay block. In this investigation the first-order Padé Approximation was found to be accurate enough to approximate the pure one sample delay.
  - PLL was also investigated in detail. The principle of PLL, and the parameter design were studied and verified using the small signal and the large signal system disturbances.
  - In this part of the study, a new approach to eliminate the modulator and demodulator block is proposed and realized the freely transformation among abc natural, αβ and dq synchronous reference frames. In addition, the limitation of this methodology was also examined in this thesis, based on which it is suggested that the best strategy for controller design is to design in dq synchronous reference frame but implemented in abc natural reference frame.
  - The small signal model for VSC itself adopted here was the average value model (AVM) which was verified in this project. Although it was found that to represent it as an ideal converter is not so accurate due to its non-linearity nature, the deviation of final results contributed by these differences was small once the loops of the whole system are closed.
Every component of the control system was characterized and verified step by step by comparing the small signal and the large signal models. This provided a solid foundation to verify the accuracy of the complete model. Furthermore, the state-space models of the system components were also developed to obtain the model of a large system.

In the development and analysis stages of this research, a block connection method was proposed which was based on modular concept.

3. Controller design of the VSC-HVDC system which is capable of working in a large set of grid impedance specifically in a weak AC system was proposed in this project by considering a wide range of operating scenarios (Chapter 4).

The causes of failures in a weak AC grid interconnected VSC-HVDC system were studied from the viewpoint of low frequency stability, in which the system tends to operate at a lower bandwidth as the SCR of the interconnected system decreasing.

Selected parameter sensitivity effects on the main and cross-coupling inner current loops were discussed which involved the following factors SCRs, X/R ratios of grid reactances’, loading conditions and different power factors.

The limitation imposed by the RHP zero on the bandwidth of the outer loop controllers was also discussed.

A robust controller design methodology was proposed by taking into account a set of operating points covering the converter operating capability (PQ chart) and the various grid conditions in terms of different SCR and X/R ratios of grid reactance. The method was realized by applying the classical frequency response technique to a set of open loop transfer functions of the target systems to be controlled. It was concluded that it is more accurate to design a controller with the previous designed controller in service, since the more detailed the system will result in a more accurate design for the later controller. In addition, such approach also allows the cross-coupling effects to be included.

A self-defined block was developed in PSCAD for facilitating the successive PSCAD simulations for verification purpose.
6.3 Suggestions for Further Research

Although, a number of research topics were indentified as potential continuing works, they are not included in this thesis to avoid diversion from the primary aims. Some of these works are listed below to guide the future researchers:

- Time domain verification for the co-operating performance of the various designed controllers was also provided.
- Finally, the small signal model development for each controller such as PID, PI with low pass filter was presented.

4. To avoid the adverse impacts of the introduction of the new source of geothermal power generation where the power are delivered via VSC-HVDC links fed into a weak AC grid (Australian), three types of damping controllers (PSS, POD and WAPOD) were designed to enhance the small-signal rotor-angle stability of the power system. To achieve this, the following tasks were completed (Chapter 5):
  - A constant admittance matrix to model the AC transmission system was studied, and it was concluded that using such representation is adequate for the analysis of the electro-mechanical modes.
  - A scaling technique was introduced which made the model applicable to the systems with different ratings.
  - The parameter sensitivity, in terms of the length of the DC link, was also examined in the thesis, which did not weaken the performance of the designed controller, but enhanced the system stability to some extent.
  - Back examination of the basement for the controller design against a higher order detailed Australian grid confirmed the accuracy of the assumption that design the control system of VSC-HVDC based on first order grid model.
  - It was observed that the introduction of the new source of geothermal power generation has an adverse impact on the damping the inter-area modes by using the small signal stability analysis.
  - Three types of damping controllers (PSS, POD and WAPOD) were designed and verified systematically to enhance the power system stability.
CHAPTER 6: CONCLUSION

- PSCAD verification of the grid integrated damping controllers can be done to be able to provide more proofs for the credibility of the designed damping controllers.
- The dynamics of the grid frequency $\Delta \omega$ can be introduced for the small signal model of DB controlled VSC, which may offer a better precision for the model.
- The control strategy employed in this thesis can be improved to allow a much weaker system to be studied to increase the operating limits of the conventional DB controlled VSC.
- The control system design is able to be improved by employing a more advanced DB current controller which can be designed by using the augmented model (a higher third-order plant model) proposed in [40]. Such an advanced DB controller can offer better control performance, which is able to facilitate the outer loop controller design.
- Coordination of PSS, POD/WAPOD and control system of VSC.
- The coordinating controllers’ parameters can be tuned according to the input/output impedance criterion as given in [65].
- Finally, the DB current controller can be applied to a grid integrated energy storage system, and the system stability can be studied. Such study can provide in-depth understanding on how the energy storage system can enhance the power system security.
Appendix A: VSC-HVDC System Parameters
### APPENDICES

<table>
<thead>
<tr>
<th>Rated Power</th>
<th>$P_n=75\text{MW}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated ac Voltage</td>
<td></td>
</tr>
<tr>
<td>rec</td>
<td>$V_{n,\text{LL}}(\text{RMS})=13.8\text{kV}$</td>
</tr>
<tr>
<td>inv</td>
<td>$V_{n,\text{LL}}(\text{RMS})=115\text{kV}$</td>
</tr>
<tr>
<td>Rated Frequency</td>
<td>$f_n=50\text{Hz}$</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>$f_{\text{sw}}=1350\text{Hz}$</td>
</tr>
<tr>
<td>Sampling</td>
<td>$f_{\text{samp}}=1350\text{Hz}$</td>
</tr>
<tr>
<td>$T_{\text{samp}}=7.4\cdot10^{-4}$</td>
<td></td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>$f_{\text{sw}}=1350\text{Hz}$</td>
</tr>
<tr>
<td>Sampling</td>
<td>$f_{\text{samp}}=1350\text{Hz}$</td>
</tr>
<tr>
<td>$T_{\text{samp}}=7.4\cdot10^{-4}$</td>
<td></td>
</tr>
<tr>
<td>commuting transformer</td>
<td></td>
</tr>
<tr>
<td>ratio</td>
<td>rec</td>
</tr>
<tr>
<td>inv</td>
<td>62.5 kV / 115 kV</td>
</tr>
<tr>
<td>equivalent inductance</td>
<td></td>
</tr>
<tr>
<td>L(pu)</td>
<td>rec</td>
</tr>
<tr>
<td>inv</td>
<td>0.15 pu</td>
</tr>
<tr>
<td>Equivalent Filter</td>
<td></td>
</tr>
<tr>
<td>R(pu)</td>
<td>rec</td>
</tr>
<tr>
<td>inv</td>
<td></td>
</tr>
<tr>
<td>L(pu)</td>
<td>rec</td>
</tr>
<tr>
<td>inv</td>
<td></td>
</tr>
<tr>
<td>Rated dc Voltage</td>
<td>$130\text{kV}$</td>
</tr>
<tr>
<td>DC-link Capacitor</td>
<td>$C=500\mu\text{F}$</td>
</tr>
<tr>
<td>Per Unit system</td>
<td></td>
</tr>
<tr>
<td>$U_{\text{b(rec)}} = \sqrt{2/3} \cdot U_{n,\text{LL(rec)}}$</td>
<td></td>
</tr>
<tr>
<td>$U_{\text{b(inv)}} = \sqrt{2/3} \cdot U_{n,\text{LL(inv)}}$</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{b(rec)}} = \frac{2}{3} \cdot \frac{S_b}{U_{\text{b(rec)}}}$</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{b(inv)}} = \frac{2}{3} \cdot \frac{S_b}{U_{\text{b(inv)}}}$</td>
<td></td>
</tr>
<tr>
<td>$U_{\text{b(dc)}} = 130\text{kV}$</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{b(dc)}} = \frac{S_b}{U_{\text{b(dc)}}}$</td>
<td></td>
</tr>
<tr>
<td>$C_p = C \cdot U_{\text{jdc}}^2 / S_b$ [116]</td>
<td></td>
</tr>
</tbody>
</table>
Appendix B: Method (II) for Elimination of Modulator/De-modulator System

This method is derived from the rotary factor perspective based on state-space equations.

A. Block Transformation Method Derivation for General Modulator/De-modulator System

The general Modulator/De-modulator system in $\alpha\beta$ reference frame is able to be modelled using a set of differential equations and a set of algebraic equations as given below, where $u, Z, y$ denote the inputs, state variables and outputs of the system quantities in $\alpha\beta$ reference frame.

\[
\begin{align*}
\dot{Z}_{\alpha\beta} & = A_0 Z_{\alpha\beta} + B_0 u_{\alpha\beta} \\
y_{\alpha\beta} & = C_0 Z_{\alpha\beta} + D_0 u_{\alpha\beta} \\
u_{\alpha\beta} & = \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix}; \quad \gamma_{\alpha\beta} = \begin{bmatrix} y_\alpha \\ y_\beta \end{bmatrix} \\
G(s) & = \frac{\gamma_{\alpha\beta}}{u_{\alpha\beta}} = C_0 (sI - A_0)^{-1} B_0 + D_0
\end{align*}
\]
\[
\begin{align*}
\dot{Z}_r &= AZ_r + B_u u_{dq} \\
\dot{y}_{dq} &= CZ_r + D_u u_{dq} \\
\end{align*}
\]  \hspace{1cm} (B.3)

\[
\begin{bmatrix}
\dot{u}_d \\
\dot{u}_q \\
\end{bmatrix} = \begin{bmatrix}
A \\
0 \\
\end{bmatrix} u_d + \begin{bmatrix}
C \\
0 \\
\end{bmatrix} u_q
\]  \hspace{1cm} (B.4)

\[
\begin{align*}
\dot{Z} &= AZ + Be^{j(\alpha_f + \theta)} u_{dq} \\
\dot{y}_{aq} &= CZ + De^{j(\alpha_f + \theta)} u_{dq}
\end{align*}
\]  \hspace{1cm} (B.5)

Set \( R = \begin{bmatrix}
cos(\alpha_f + \theta) & -sin(\alpha_f + \theta) \\
sin(\alpha_f + \theta) & \cos(\alpha_f + \theta)
\end{bmatrix} \Rightarrow \begin{align*}
\dot{Z} &= AZ + BR u_{dq} \\
\dot{y}_{aq} &= CZ + DR u_{dq}
\end{align*} \hspace{1cm} (B.6)

In which,
\[
A = \begin{bmatrix}
A_0 & 0 \\
0 & A_0
\end{bmatrix}; B = \begin{bmatrix}
B_0 & 0 \\
0 & B_0
\end{bmatrix}; C = \begin{bmatrix}
C_0 & 0 \\
0 & C_0
\end{bmatrix}; D = \begin{bmatrix}
D_0 & 0 \\
0 & D_0
\end{bmatrix}
\]

This assumption is valid because system is symmetrical,
\[
\dot{Z} - AZ = BR u_{dq} \hspace{1cm} (B.7)
\]

Multiply \( R^{-1} \) both sides,
\[
R^{-1}(\dot{Z} - AZ) = R^{-1} BR u_{dq} \hspace{1cm} (B.8)
\]

\[
R^{-1} BR = \begin{bmatrix}
cos(\alpha_f + \theta) & \sin(\alpha_f + \theta) \\
-sin(\alpha_f + \theta) & \cos(\alpha_f + \theta)
\end{bmatrix} \begin{bmatrix}
B_0 & 0 \\
0 & B_0
\end{bmatrix} = \begin{bmatrix}
B_0 & 0 \\
0 & B_0
\end{bmatrix}
\]  \hspace{1cm} (B.9)

\[
= \begin{bmatrix}
1 & 0 \\
0 & 1
\end{bmatrix}
\]

\[
R^{-1}(\dot{Z} - AZ) = B_0 u_{dq} \hspace{1cm} (B.10)
\]

\[
R^{-1} \dot{Z} - R^{-1} AZ = B_0 u_{dq}
\]
Appendix B: Method (II) for Elimination of Modulator/De-modulator System

\[ R^{-1} \ddot{Z} + (R^{-1} \cdot Z - (R^{-1}) \cdot Z - R^{-1} AZ = B_0 \mu_{d_q} \]

\[ (R^{-1} \cdot Z) = (R^{-1} \cdot Z + R^{-1} AZ + B_0 \mu_{d_q} \]

\[ \therefore R^{-1} = e^{-j\omega t}; (R^{-1}) = -j \omega_0 e^{-j\omega t} = -j \omega_0 R^{-1} \]

\[ \therefore (R^{-1} \cdot Z) = -j \omega_0 R^{-1} \cdot Z + R^{-1} AZ + B_0 \mu_{d_q} \]

\[ R^{-1}A = \begin{bmatrix} \cos(\omega_0 t + \theta) & \sin(\omega_0 t + \theta) \\ -\sin(\omega_0 t + \theta) & \cos(\omega_0 t + \theta) \end{bmatrix} \begin{bmatrix} A_0 & 0 \\ 0 & A_0 \end{bmatrix} = \begin{bmatrix} \cos(\omega_0 t + \theta)A_0 & \sin(\omega_0 t + \theta)A_0 \\ -\sin(\omega_0 t + \theta)A_0 & \cos(\omega_0 t + \theta)A_0 \end{bmatrix} \]

\[ AR^{-1} = \begin{bmatrix} A_0 & 0 \\ 0 & A_0 \end{bmatrix} \begin{bmatrix} \cos(\omega_0 t + \theta) & \sin(\omega_0 t + \theta) \\ -\sin(\omega_0 t + \theta) & \cos(\omega_0 t + \theta) \end{bmatrix} = \begin{bmatrix} A_0 \cos(\omega_0 t + \theta) & A_0 \sin(\omega_0 t + \theta) \\ -A_0 \sin(\omega_0 t + \theta) & A_0 \cos(\omega_0 t + \theta) \end{bmatrix} \]

\[ \therefore R^{-1}A = AR^{-1} \]

\[ \Rightarrow (R^{-1} \cdot Z) + j \omega_0 (R^{-1} \cdot Z) - A(R^{-1}Z) = B_0 \mu_{d_q} \]

\[ \Rightarrow s(R^{-1} \cdot Z) + j \omega_0 (R^{-1} \cdot Z) - A(R^{-1}Z) = B_0 \mu_{d_q} \]

\[ \Rightarrow \frac{R^{-1} \cdot Z}{\mu_{d_q}} = \frac{B_0}{(s + j \omega - A)} \Rightarrow Z = \frac{R \cdot B_0 \cdot \mu_{d_q}}{(s + j \omega - A)} \]  \hspace{1cm} (B.11)

Substituting (B.4) into (B.5), it can be easily obtained

\[ R_y_{d_q} = CZ + D\mu_{d_q} \Rightarrow y_{d_q} = R^{-1}CZ + R^{-1}D\mu_{d_q} \]  \hspace{1cm} (B.12)

Then substituting (B.11) into (B.12), we can obtain,

\[ \Rightarrow G(s) = \frac{y_{d_q}}{u_{d_q}} = R^{-1}CR[(s + j \omega) - A]^{-1}B_0 + R^{-1}DR \]

\[ Since, R^{-1}CR = C_0; R^{-1}DR = D_0 \]

\[ G(s) = C_0[(s + j \omega) - A]^{-1}B_0 + D_0 \]  \hspace{1cm} (B.13)

Therefore, the transfer function transferred from \( \alpha \beta \) to \( dq \) reference frame can be easily done by replacing Laplace factor \( s \) with \( s+j\omega \) item.

**B. Compute State Space Equations and the Frequency Response Matrix**

The original \( \alpha \beta \) reference frame state space equation is as follows,

\[ \begin{align*}
\dot{Z} &= AZ + B_\alpha \mu_{\alpha} \\
\gamma_{\alpha} &= CZ + D_\alpha \mu_{\alpha}
\end{align*} \hspace{1cm} (B.14) \]

Transfer to \( dq \) reference frame is done by replace \( s \) with \( s+j\omega \)

\[ \begin{align*}
(s + j \omega)Z_{d_q} &= A_{d_q} Z_{d_q} + B_{d_q} \mu_{d_q} \\
\gamma_{d_q} &= C_{d_q} Z_{d_q} + D_{d_q} \mu_{d_q}
\end{align*} \hspace{1cm} (B.15) \]
As the original $\alpha\beta$ reference frame transfer function is

\[
G(s)|_{\alpha\beta} = C(sI - A)^{-1}B + D
\]

\[
G(s)|_{dq} = C[(sI + j\Omega) - A]^{-1}B + D
\]

\[
G(s)|_{dq} = C\frac{1}{(sI + j\Omega) - A}B + D
\]

\[
G(s)|_{dq} = C\frac{1}{(sI - A) + j\Omega}B + D
\]

\[
G(s)|_{dq} = C\frac{(sI - A) - j\Omega}{(sI - A)^2 + \Omega^2}B + D
\]

\[
G(s)|_{dq} = (C\frac{sI - A}{(sI - A)^2 + \Omega^2}B + D) - jC\frac{\Omega}{(sI - A)^2 + \Omega^2}B
\]

\[
Y_d + jY_q = [(C\frac{sI - A}{(sI - A)^2 + \Omega^2}B + D) - jC\frac{\Omega}{(sI - A)^2 + \Omega^2}B](U_d + jU_q)
\]

\[
Y_d = (C\frac{sI - A}{(sI - A)^2 + \Omega^2}B + D)U_d + C\frac{\Omega}{(sI - A)^2 + \Omega^2}BU_q
\]

\[
Y_q = -C\frac{\Omega}{(sI - A)^2 + \Omega^2}BU_d + (C\frac{sI - A}{(sI - A)^2 + \Omega^2}B + D)U_q
\]

\[
\frac{Y_d}{U_d} = C\frac{sI - A}{(sI - A)^2 + \Omega^2}B + D; \quad \frac{Y_d}{U_q} = C\frac{\Omega}{(sI - A)^2 + \Omega^2}B; \quad \frac{Y_q}{U_d} = -C\frac{\Omega}{(sI - A)^2 + \Omega^2}B; \quad \frac{Y_q}{U_q} = C\frac{sI - A}{(sI - A)^2 + \Omega^2}B + D
\]
Appendix C: Method (I) for Elimination of Modulator/Demodulator System

This method is derived from the transfer matrix state space equations point of view avoiding imaginary component during derivation

A. Continued to Equation (3-83)

Substituting \([\dot{X}_\alpha, \dot{X}_\beta]^T\) in equation (3-80) into equation (3-83), substituting \([X_\alpha, X_\beta]^T\) in equation (3-78) into equation (3-83),

\[
\begin{bmatrix}
\cos \theta \ln - \sin \theta \ln \\
\sin \theta \ln \cos \theta \ln
\end{bmatrix}
\frac{d}{dt} \begin{bmatrix} Z_x \\ Z_q \end{bmatrix} = \begin{bmatrix} A & 0 \\ 0 & A \end{bmatrix} \begin{bmatrix} \cos \ln - \sin \ln \\ \sin \ln \cos \ln \end{bmatrix} \begin{bmatrix} Z_x \\ Z_q \end{bmatrix} + \begin{bmatrix} \sin \theta \ln \cos \theta \ln \\ -\cos \theta \ln \sin \theta \ln \end{bmatrix} \frac{d\theta}{dt} \begin{bmatrix} Z_x \\ Z_q \end{bmatrix} + \begin{bmatrix} B & 0 \\ 0 & B \end{bmatrix} \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} u_d \\ u_q \end{bmatrix}
\]

Aside: Compute

\[
\begin{bmatrix}
\cos \theta \ln & -\sin \theta \ln \\
\sin \theta \ln & \cos \theta \ln
\end{bmatrix}^{-1}
\]

According to the Woodbury matrix identity theory, this matrix has the form that

\[
\begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} = \begin{bmatrix} A^{-1} + A^{-1}BPCA^{-1} & -A^{-1}BP \\ -PCA^{-1}P & P \end{bmatrix} = \begin{bmatrix} E & F \\ G & H \end{bmatrix}
\]
where, \( P = (D - CA^{-1}B)^{-1} \)

\[
\begin{align*}
A &= \cos \theta \ln \\
B &= -\sin \theta \ln \\
C &= \sin \theta \ln \\
D &= \cos \theta \ln \\
\end{align*}
\]

(C.4)

\[
A^{-1} = \frac{1}{\cos \theta} \ln
\]

(C.5)

\[
P = [\cos \theta \ln - \sin \theta \ln(\frac{1}{\cos \theta})\ln(-\sin \theta \ln)]^{-1}
\]

(C.6)

\[
E = (A^{-1} + A^{-1}BPCA^{-1}) \text{ from(C.3)}
\]

\[
= \frac{1}{\cos \theta} \ln + (-\frac{1}{\cos \theta} \ln)(-\sin \theta \ln) \cdot (\cos \theta \ln) \cdot (\frac{1}{\cos \theta} \ln)
\]

\[
= \frac{1}{\cos \theta} \ln - \frac{\sin^2 \theta}{\cos \theta} \ln
\]

\[
= (\frac{1}{\cos \theta} \ln)(1 - \sin^2 \theta) \ln
\]

\[
= \cos \theta \ln \ln
\]

\[
F = -A^{-1}BP
\]

\[
= (-\frac{1}{\cos \theta} \ln)(-\sin \theta \ln)(\cos \theta \ln)
\]

\[
F = \sin \theta \ln \text{ from(C.3)}
\]

\[
G = -PCA
\]

\[
= (-\cos \theta \ln)(\sin \theta \ln)(\frac{1}{\cos \theta} \ln)
\]

\[
G = -\sin \theta \ln \text{ from(C.3)}
\]

\[
H = P
\]

\[
H = \cos \theta \ln
\]

Thus, equation (C.2) can be written as equation (C.7) according to equation (C.3).

\[
\begin{bmatrix}
\cos \theta \ln & -\sin \theta \ln \\
\sin \theta \ln & \cos \theta \ln 
\end{bmatrix}^{-1}
\begin{bmatrix}
E & F \\
G & H 
\end{bmatrix}
= \begin{bmatrix}
\cos \theta \ln & \sin \theta \ln \\
-\sin \theta \ln & \cos \theta \ln 
\end{bmatrix}
\]

(C.7)

From equation (C.1), the equation (C.7) can be written as,
Appendix C: Method (I) for Elimination of Modulator/Demodulator System

\[
\begin{bmatrix}
\dot{Z}_d \\
\dot{Z}_q
\end{bmatrix} = \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
A & 0 \\
0 & A
\end{bmatrix}
\begin{bmatrix}
\cos In & -\sin In \\
\sin In & \cos In
\end{bmatrix}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
+ \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
\sin \theta & \cos \theta \\
-\cos \theta & \sin \theta
\end{bmatrix}
\frac{d\theta}{dt}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
+ \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
B & 0 \\
0 & B
\end{bmatrix}
\begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
u_d \\
u_q
\end{bmatrix}
+ \begin{bmatrix}
\cos \theta A & \sin \theta A \\
-\sin \theta A & \cos \theta A
\end{bmatrix}
\begin{bmatrix}
\cos In & -\sin In \\
\sin In & \cos In
\end{bmatrix}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
\end{aligned}
\]

\[
\begin{aligned}
\dot{Z}_d &= \begin{bmatrix}
\cos \theta A & \sin \theta A \\
-\sin \theta A & \cos \theta A
\end{bmatrix}
\begin{bmatrix}
\cos In & -\sin In \\
\sin In & \cos In
\end{bmatrix}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
+ \begin{bmatrix}
\cos \theta B & \sin \theta B \\
-\sin \theta B & \cos \theta B
\end{bmatrix}
\begin{bmatrix}
\cos In & -\sin In \\
\sin In & \cos In
\end{bmatrix}
\begin{bmatrix}
u_d \\
u_q
\end{bmatrix}
+ \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\frac{d\theta}{dt}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
+ \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\frac{d\theta}{dt}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
+ \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\frac{d\theta}{dt}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
= \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\frac{d\theta}{dt}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
\end{aligned}
\]

Now assume that, which is significantly important, \(\frac{d\theta}{dt} = \omega_0\)

\[
\begin{bmatrix}
\dot{X}_d \\
\dot{X}_q
\end{bmatrix} = \begin{bmatrix}
A & In\omega_0 \\
-In\omega_0 & A
\end{bmatrix}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
+ \begin{bmatrix}
B & 0 \\
0 & B
\end{bmatrix}
\begin{bmatrix}
u_d \\
u_q
\end{bmatrix}
\]

(C.8)

Substituting \([X_d, X_q]'\) in equation (3.78) into equation (3.84), substituting \([u_d, u_q]'\) in equation (3.81) (a) into equation(3.85),

\[
\begin{bmatrix}
y_d \\
y_q
\end{bmatrix} = \begin{bmatrix}
C & 0 \\
0 & C
\end{bmatrix}
\begin{bmatrix}
\cos In & -\sin In \\
\sin In & \cos In
\end{bmatrix}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
+ \begin{bmatrix}
D & 0 \\
0 & D
\end{bmatrix}
\begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
u_d \\
u_q
\end{bmatrix}
\]

\[
\begin{bmatrix}
y_d \\
y_q
\end{bmatrix} = \begin{bmatrix}
C & 0 \\
0 & C
\end{bmatrix}
\begin{bmatrix}
\cos In & -\sin In \\
\sin In & \cos In
\end{bmatrix}
\begin{bmatrix}
Z_d \\
Z_q
\end{bmatrix}
+ \begin{bmatrix}
-D & 0 \\
0 & -D
\end{bmatrix}
\begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}
\begin{bmatrix}
u_d \\
u_q
\end{bmatrix}
\]

(C.9)

Finally, rewrite equation(C.8) and(C.9) below; they can be combined in equation
These two equations can be combined as equations (3-86).

**B. Compute the Frequency Response Matrix**

\[
sZ_{dq} = A_{dq}Z_{dq} + B_{dq}u_{dq}
\]

\[
(sI - A_{dq})Z_{dq} = B_{dq}u_{dq}
\]

\[
Z_{dq} = (sI - A_{dq})^{-1}B_{dq}u_{dq}
\]

\[
y_{dq} = (C_{dq}(sI - A_{dq})^{-1}B_{dq} + D_{dq})u_{dq}
\]

\[
G_{dq}(s) = \frac{y_{dq}}{u_{dq}} = C_{dq}(sI - A_{dq})^{-1}B_{dq} + D_{dq}
\]

Consider the term \((sI - A_{dq})^{-1}\) as follows:

\[
(sI - A_{dq})^{-1} = \left( \begin{array}{cc} sI & 0 \\ 0 & sI \end{array} \right)^{-1} = \left( \begin{array}{cc} A_{dq} & \omega_d I \\ -\omega_d I & A_{dq} \end{array} \right)^{-1}
\]

\[
= \left( \begin{array}{cc} (sI - A_{dq}) & -\omega_d I \\ \omega_d I & (sI - A_{dq}) \end{array} \right)^{-1}
\]

Now use equation (C.3) to compute equation (C.12), in the following A, B, C, D in equation (C.3) are replaced by a,b,c,d to avoid confusion with the state-matrix.

\[
a = sI - A_{dq};
\]

\[
b = -\omega_d I;
\]

\[
c = \omega_d I;
\]

\[
d = sI - A_{dq};
\]

\[
P = (d - ca^{-1}b)^{-1}
\]

\[
= (a - ca^{-1}b)^{-1}
\]

\[
= (a - \omega_d Ia^{-1}(-\omega_d I)^{-1})^{-1}
\]

\[
= (a + \omega_d I)^{-1}
\]
Appendix C: Method (I) for Elimination of Modulator/Demodulator System

\[ E = a^{-1} + a^{-1}bpca^{-1} \]
\[ = a^{-1} + a^{-1}b(a + \omega_h^2 a^{-1})^{-1}ca^{-1} \]
\[ = a^{-1} - \omega_h^2 a^{-1}(a + \omega_h^2 a^{-1})^{-1}a^{-1} \]
\[ = a^{-1}(In - \omega_h^2(a + \omega_h^2 a^{-1})^{-1}a^{-1}) \]  \hspace{1cm} (C.15)
\[ = a^{-1}(In - \omega_h^2(a(a + \omega_h^2 a^{-1}))^{-1}) \]
\[ = a^{-1}(In - \omega_h^2(a^2 + \omega_h^2 In)^{-1}) \]
\[ = a(a^2 + \omega_h^2 In)^{-1} \]

\[ F = -a^{-1}bp \]
\[ = a^{-1}\omega_h(a + \omega_h^2 a^{-1})^{-1} \]
\[ = \omega_h a^{-1}(a + \omega_h^2 a^{-1})^{-1} \]  \hspace{1cm} (C.16)
\[ = \omega_h((a + \omega_h^2 a^{-1})a)^{-1} \]
\[ = \omega_h(a^2 + \omega_h^2 In)^{-1} \]

\[ G = -pca^{-1} \]
\[ = -(a + \omega_h^2 a^{-1})^{-1}\omega_h Ina^{-1} \]
\[ = -\omega_h((a + \omega_h^2 a^{-1})^{-1}a^{-1}) \]  \hspace{1cm} (C.17)
\[ = -\omega_h(a(a + \omega_h^2 a^{-1}))^{-1} \]
\[ = -\omega_h(a^2 + \omega_h^2 In)^{-1} \]

\[ H = p \]
\[ = (a + \omega_h^2 a^{-1})^{-1} \]

The Woodbury identity is
\[ (A + CBC^T)^{-1} = A^{-1} - A^{-1}C(B^{-1} + C^TA^{-1}C)C^{-1}TA^{-1} \]

Define \( A = a, C = \omega_h In, C^T = \omega_h In, B = a^{-1} \)

\[ H = (a + \omega_h^2 a^{-1})^{-1} = a^{-1} - a^{-1}\omega_h^2(a + \omega_h^2 a^{-1})^{-1}a^{-1} \]
\[ = a^{-1}(In - \omega_h^2(a + \omega_h^2 a^{-1})^{-1}a^{-1}) \]

Then:
\[ = a^{-1}(In - \omega_h^2(a(a + \omega_h^2 a^{-1}))^{-1}) \]
\[ = a^{-1}(In - \omega_h^2(a^2 + \omega_h^2 In)^{-1}) \]
\[ = a(a^2 + \omega_h^2 In)^{-1} \]

Thus
\[ H = E \]  \hspace{1cm} (C.18)

\[ (sI - A_{\omega_h})^{-1} = \begin{bmatrix} E(s) & F(s) \\ -F(s) & E(s) \end{bmatrix} = \begin{bmatrix} a(a^2 + \omega_h^2 In)^{-1} & \omega_h(a^2 + \omega_h^2 In)^{-1} \\ -\omega_h(a^2 + \omega_h^2 In)^{-1} & a(a^2 + \omega_h^2 In)^{-1} \end{bmatrix} \]  \hspace{1cm} (C.19)
Substitute \( a = s\ln - A_{dq} \) into equation (C.19).

\[
(sI - A_{dq})^{-1} = \begin{bmatrix}
(sI - A)((sI - A)^2 + \omega_0^2)^{-1} & \omega_0((sI - A)^2 + \omega_0^2)^{-1} \\
-\omega_0((sI - A)^2 + \omega_0^2)^{-1} & (sI - A)((sI - A)^2 + \omega_0^2)^{-1}
\end{bmatrix}
\]

(C.20)

\[
E(s) = (sI - A)((sI - A)^2 + \omega_0^2)^{-1}, F(s) = \omega_0((sI - A)^2 + \omega_0^2)^{-1}
\]

(C.21)

\[
G_{dq}(s) = \begin{bmatrix}
C & 0 \\
0 & C
\end{bmatrix}
\begin{bmatrix}
E(s) & F(s) \\
-F(s) & E(s)
\end{bmatrix}
\begin{bmatrix}
B & 0 \\
0 & B
\end{bmatrix}
+ \begin{bmatrix}
D & 0 \\
0 & D
\end{bmatrix}
\]

\[
= \begin{bmatrix}
CE(s) & CF(s) \\
-CF(s) & CE(s)
\end{bmatrix}
\begin{bmatrix}
B & 0 \\
0 & B
\end{bmatrix}
+ \begin{bmatrix}
D & 0 \\
0 & D
\end{bmatrix}
\]

(C.22)

\[
= \begin{bmatrix}
G_{dd}(s) & G_{dq}(s) \\
G_{dq}(s) & G_{qq}(s)
\end{bmatrix}
\]

\[
G_{dd}(s) = CE(s)B + D
\]

\[
= C((sI - A)((sI - A)^2 + \omega_0^2)^{-1}B + D
\]

\[
G_{dq}(s) = CF(s)B
\]

\[
= C\omega_0((sI - A)^2 + \omega_0^2)^{-1}B
\]

(C.23)

\[
G_{qd}(s) = -CF(s)B
\]

\[
= -C\omega_0((sI - A)^2 + \omega_0^2)^{-1}B
\]

\[
= -G_{dq}(s)
\]

\[
G_{qq}(s) = G_{dd}(s)
\]

where, \( G_{dq}(s) \) and \( G_{qd}(s) \) are cross-coupling items between dq axes due to modulation d e-modulation.
Appendix D: Lead-Lag Block

State space equation of lead-lag block

\[
\begin{align*}
\dot{x} \cdot k(1 + T_a s) &= y(1 + T_b s) \\
kx + kx T_a s &= y + y T_b s \\
kx - y &= s(T_b y - KT_a x) \\
\frac{kx}{T_b} - \frac{y}{T_b} &= s(y - k \frac{T_a}{T_b} x)
\end{align*}
\] (D.1)

set \quad y - k \frac{T_a}{T_b} x = z \Rightarrow y = z + k \frac{T_a}{T_b} x \quad \text{(D.2)}

\[
\begin{align*}
sz &= \frac{k}{T_b} x - \frac{1}{T_b} (z + k \frac{T_a}{T_b} x) 
\end{align*}
\] (D.3)

Figure D.1 Block diagram of lead-lag-gain
\begin{equation}
\begin{cases}
s_z = -\frac{1}{T_b} z + \left(\frac{k}{T_b} - \frac{k}{T_b T_b}\right) x \\
y = z + k \frac{T_z}{T_b} x
\end{cases}
\end{equation}

Set $A = -\frac{1}{T_b}$; $B = \frac{k}{T_b} - \frac{k}{T_b T_b}$; $C = 1$; $D = k \frac{T_a}{T_b}$
Appendix E: Regional Boundaries for the National Electricity Market & Committed Developments
Appendix F: Performance Evaluation of all the Power and Voltage Controllers with a New set of DC Link Parameters

A. Rectifier Side Power Controller with Updated DC Link

Figure F-1 Open loop frequency response (a) without and (b) with power controller under the updated DC link condition
Figure F-2 Step response on power reference with updated DC link parameters

B. Rectifier Side AC Controller with Updated DC Link

Figure F-3 Open loop frequency response (a) without and (b) with rectifier side AC voltage controller under the updated DC link condition
Appendix F: Performance Evaluation of all the Power and Voltage Controllers with a New set of DC Link Parameters

Figure F-4 Step response on rectifier side AC voltage reference with updated DC link parameters

C. **Inverter Side DC Voltage Controller with Updated DC Link**

Figure F-5 Open loop frequency response (a) without and (b) with inverter side DC voltage controller under the updated DC link condition
Figure F-6 Step response on inverter side DC voltage reference with updated DC link parameters

D. Inverter Side AC Voltage Controller with Updated DC Link

Figure F-7 Open loop frequency response (a) without and (b) with inverter side DC voltage controller under the updated DC link condition
Appendix F: Performance Evaluation of all the Power and Voltage Controllers with a New set of DC Link Parameters

Figure F-8 Step response on inverter side AC voltage reference with updated DC link parameters

E. Step Tests for System with All Controllers in service under Updated DC Link Condition

a) Step test on rectifier side power controller

(a) Rectifier side Power response

(b) Rectifier side AC voltage response
APPENDICES

b) Step test on rectifier side AC voltage controller

(a) Rectifier side Power response  
(b) Rectifier side AC voltage response

(c) Inverter side DC voltage response  
(d) Inverter side AC voltage response
Appendix F: Performance Evaluation of all the Power and Voltage Controllers with a New set of DC Link Parameters

c) **Step test on inverter side DC voltage controller**

(a) Rectifier side Power response

(b) Rectifier side AC voltage response

(c) Inverter side DC voltage response

(d) Inverter side AC voltage response

d) **Step test on inverter side AC voltage controller**

(a) Rectifier side Power response

(b) Rectifier side AC voltage response
(c) Inverter side DC voltage response

(d) Inverter side AC voltage response
### Appendix G: VSC-HVDC System (II) Parameters

#### Basement for AC system

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_b$</td>
<td>Nominal three-phase power of the ac grid</td>
<td>75MW</td>
</tr>
<tr>
<td>$V_b$</td>
<td>Nominal peak phase voltage at the ac side</td>
<td>$V_b = \frac{V_{L1}(\text{rms})}{\sqrt{3}} \cdot \sqrt{2} \bigg</td>
</tr>
<tr>
<td>$I_b$</td>
<td>Nominal peak phase current</td>
<td>$I_b = \frac{2}{3} \cdot \frac{S_b}{V_b} = 0.9798kA$</td>
</tr>
<tr>
<td>$Z_b$</td>
<td>Nominal impedance</td>
<td>$Z_b = \frac{V_b}{I_b} = 52.082\Omega$</td>
</tr>
<tr>
<td>$R_c$</td>
<td>Converter resistance of reactance</td>
<td>$0.0015pu=0.0015*Z_b = 0.0781\Omega$</td>
</tr>
<tr>
<td>$L_c$</td>
<td>Converter inductance of reactance</td>
<td>$0.15pu=0.15*Z_b/\omega_b=0.0249H$</td>
</tr>
<tr>
<td>$\omega_b$</td>
<td>Base frequency</td>
<td>$2\pi \cdot 50Hz$</td>
</tr>
</tbody>
</table>

*The base for per unit transformation is chosen as to achieve a power invariant transformation, so that the ac and dc side power is the same.*

#### Basement for DC system
<table>
<thead>
<tr>
<th>$V_{dc,b}$</th>
<th>Nominal DC voltage</th>
<th>130kV</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{dc,b}$</td>
<td>Nominal DC current</td>
<td>0.5769kA</td>
</tr>
<tr>
<td>$Z_{dc,b}$</td>
<td>Nominal DC impedance</td>
<td>225.33 Ω</td>
</tr>
<tr>
<td>$\tau_b$</td>
<td>Time constant</td>
<td>$C \cdot \frac{V_{dc,b}^2}{S_b}$</td>
</tr>
</tbody>
</table>
Reference


